國 立 交 通 大 學

電機與控制工程學系

博士論文

新型式單相單級交流轉直流且具有輸入電流修飾的

電源轉換器

Novel Single-Phase Single-Stage AC/DC Converters

with Input Current Shaper

研 究 生: 劉興富

指導教授: 張隆國 博士

中 華 民 國 九十四 年 四 月

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國立交通大學

電機與控制工程學系

博士論文

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In

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Hsingchu, Taiwan, Republic of China

中 華 民 國 九十四 年 四 月

博碩士論文授權書

本授權書所授權之論文為本人在 國立交通 大學(學院) 電機與控制工程 系所 電機電力 組 93 學年度第 2 學期取得 博 士學位之論文。

論文名稱：新型式單相單級交流轉直流且具有輸入電流修飾的電源轉換器

指導教授： 張隆國

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研究生簽名：劉曉富　　學號：8812804

日期：民國　94 年　6　月　1　日

國家圖書館博碩士論文電子檔案上網授權書

本授權書所授權之論文為本人在 國立交通 大學(學院) 電機與控制工程 系所
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研究生簽名：劉曉富　　學號：8812804
（親筆正楷）　　（務必填寫）

日期：民國　94 年　6　月　1　日

---

1. 本授權書請以黑筆撰寫，並列印二份，其中一份影印裝訂於附錄三之一(博碩士論文授權書)之次頁.

推薦函

一、事由：推薦電機與控制工程系博士班研究生劉興富提出論文以參加國立交通大學博士論文口試。

二、說明：本校電機與控制工程系博士班研究生劉興富已完成博士班規定之學科及論文研究訓練。

有關學科部分，劉君已修畢應修學分（請查學籍資料, 學號 8812804），通過資格考試；有關論文方面，劉君已完成“新型式單相單級交流轉直流且具有輸入電流修飾的電源轉換器”初稿。其相關論文已刊登於 IEEE Transactions on Power Electronics, Jan./2005 和 IEEE Transactions on Industrial Electronics, Feb./2005。同時所研發的新技術已獲得發明專利認證另有多篇論文分別發表於重要的國內外研討會（請參閱博士論文著作目錄）。

三、總言之，劉君已具備國立交通大學電機與控制工程系博士班研究生應有之教育及訓練水準，因此推薦劉君參加國立交通大學電機與控制工程系博士論文口試。

此致

國立交通大學電機與控制工程系

電機與控制工程系教授

張隆國

國 立 交 通 大 學

論 文 口 試 委 員 會 審 定 書

本校 電機與控制工程學系 博士班 劉興富 君

所提論文: 新型式單相單級交流轉直流且具有輸入電流修飾的電源轉換器

合於博士資格水準、業經本委員會評審認可。

口試委員：劉添華 李祖添 陳德玉 余松清 蕭曉時 張隆國

指導教授：張隆國

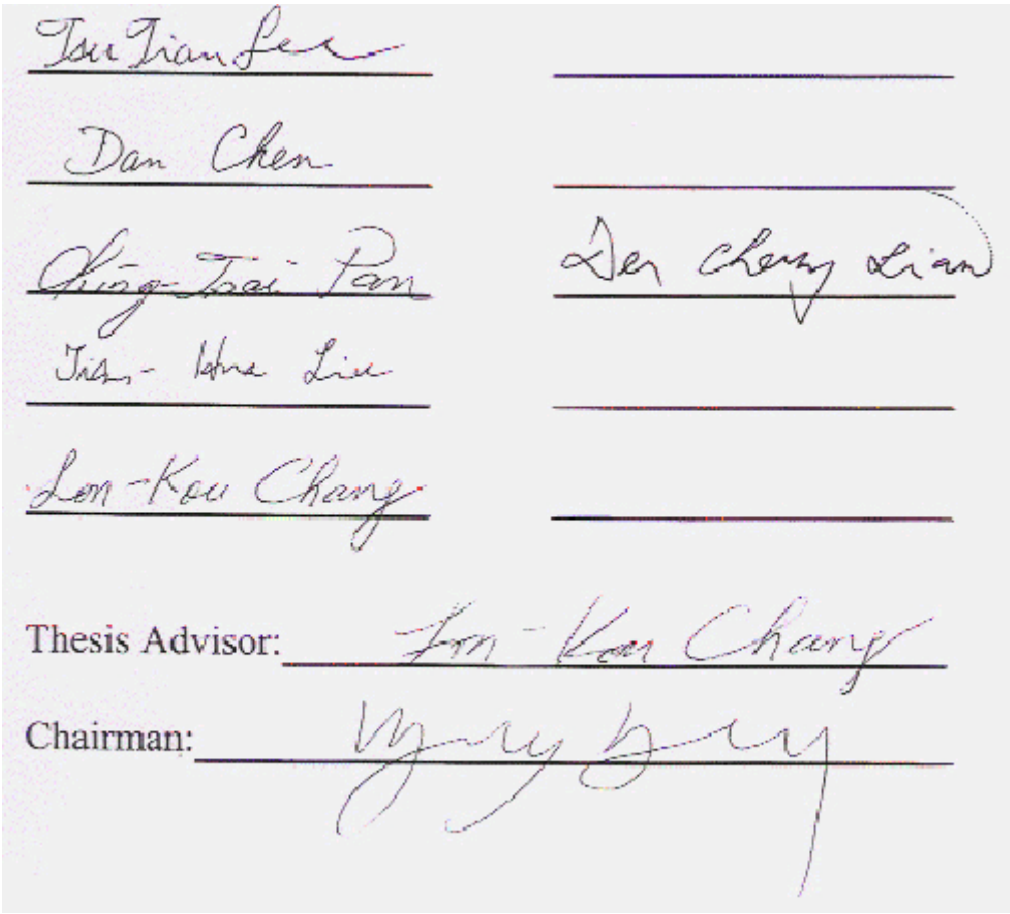
系 主 任：易谷澤

中 華 民 國 九十四 年 四 月二十七 日

Department of Electrical and Control Engineering National Chiao Tung University
Hsinchu, Taiwan R.O.C.

Date: April 27, 2005

We have carefully read the dissertation entitled Novel Single-Phase Single-Stage AC/DC Converters with Input Current Shaper submitted by Hsing-Fu Liu in partial fulfillment of the requirements of the degree of **DOCTOR OF PHILOSOPHY** and recommend its acceptance.



Thesis Advisor:

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新型式單相單級交流轉直流且具有輸入電流修飾的電源轉換器

學生：劉興富　　指導教授：張隆國

國立交通大學電機與控制工程學系（研究所）博士班

摘　　要

本論文研製之新型輸入電流修飾器應用於交流轉直流電源轉換器，此轉換器具有輸入電流諧波校正功能以及輸出電壓快速反應特性。在文中所介紹的輸入電流修飾器應用在兼具電流校正功能的反馳式架構，順向式架構和橋式架構。明顯改善了傳統交流轉直流電源轉換器中輸入電流的諧波電流，若經過適當設計功率因數可高達 90%以上，且只要選用傳統控制器既可完成穩定輸出電壓與電流，是一項精巧而實用的研究成果。所有文中提及的電路都是在穩態情況作分析與考量。所做的分析研究包括操作原理分析、重要參數分析、電路設計步驟最後還有電路模擬或雛型電路實作驗證性能。

這論文研究的交流轉直流電源轉換器中利用變壓器加繞一線圈達到兩個主要優點：(i) 本設計大大減小舊有單級 Boost-型功率因數校正單元中的大電感。 在同樣輸出瓦特數， 舊有單級具功率因數校正轉換器中的 boost 電感有高至 1.7 倍於磁化電感的感值，或是 1.4mH 的感值。在論文中所研

究的電路所使用的電感 L_1 其電感值可低至 0.1 倍於磁化電感或是 30 μH 的電感值。(ii) 另一優點是在輸入端整流用的大電容電壓差可以控制在 450V 以下， 經由調整變壓器線圈的圈數比可以達成即便是在全範圍輸入電壓也適用(90V~265V)。雖然這幾年有不少類似技術文獻的出現，其中有些要用到較複雜的控制電路達到高的功率因數、非固定切換頻率作高功率因數調整或是在電路前段的升壓部分仍具有大體積的電感，過去所提的這些方法固然有其個別優點，可是在競爭激烈的切換式電源市場角度評量，電路架構簡單、高信賴度、以及成本是主要考量因素。

本文中所新提出的轉換器即使在輸入功率高至 600W 應用範圍也能滿足規範 IEC61000-3-2 class D 的要求，且具有輸出電壓快速動態反應的性能。文中所研究的電路具有結構簡單，高信賴度，與低的成本。其中的切換頻率是定頻式，對於變壓器設計和電磁干擾防治可有較好的效果。且論文中研究的電路可以用最普通的控制器 UC3842 或 TL494 來完成應用設計而且電氣性能表現符合電流諧波規範。

Novel Single-Phase Single-Stage AC/DC Converters with Input Current Shaper

Student：Hsing-Fu Liu　　Advisors：Dr. Lon-Kou Chang

Department（Institute）of Electrical and Control Engineering
National Chiao Tung University

ABSTRACT

This dissertation presents a new input current shaper (ICS) for single-phase single-stage AC/DC converters with harmonic current correction and fast output voltage regulation. The proposed ICS are applied in flyback structure, forward structure, and bridge structure with the function of harmonic current correction. All the circuits are analyzed in steady state consideration. The study contains operation principle analysis, critical parameters analysis, design procedure. Finally, simulations and experiment results are shown for verifications.

In the proposed AC/DC converters, an extra winding wound in the transformer provides two key advantages: (i) The size of the bulk inductor used in the conventional boost-based PFC cell can be significantly reduced in the proposed converters. In same output power application, the main transformer should has similar size but the boost inductor in prior single-stage PFC converter will be up to $1.7L_m$ or 1.4mH, and the inductor L_1 in the proposed circuit can be down to $0.1L_m$ or 30 μH. (ii) The voltage across bulk capacitor can be held under 450V by tuning the transformer windings ratio even though the converter operates in a wide range of input voltages (90V~265V/ac). Similar technique has been reported in recent years, but complex control circuit is needed to achieve high power factor or still use a bulk inductor in the boost-cell in the

front stage of the converter. In a competitive market of switching power supply, the main consideration includes a simple, reliable, and cost-effective. Therefore, there is an improved opportunity in those presented solutions.

These new converters comply with IEC 61000-3-2 class D from the load range up to 600W, and can achieve fast output voltage regulation. The proposed circuit has a simple, reliable, and cost-effective structure. The switching frequency is fixed in the proposed converters, which benefits the design of transformer and EMI filter. The proposed solution employs conventional controller, UC3842 or TL494, to implement the circuits and the solution can comply with the agent's standards.

誌　　謝

首先感謝指導老師張隆國博士五年多來在各方面的協助與指導，進博士班很重要的是有位學風自由與術德兼備的指導老師，很榮幸我遇到了。張老師在學術研究上讓我有很大思考空間，所以我很快的確定研究方向，同時每當我在研究上遇到困難時都能適時協助化解疑惑讓我的研究能有所進展。而且指導過程中時常提醒我一個很重要的觀念，學術研究只是人生中的一個小過程，重要的是人生的價值與意義一定要清楚把握，這聲音一值盤旋在我的心裡很久。很榮幸成為張老師門下首位取得博士學位學生。

在論文寫作上除了平日指導老師的教導，非常感謝口試委員李祖添教授，陳德玉教授，潘晴財教授，劉添華教授與廖德誠教授在百忙中提出寶貴的建議與指導讓我的論文更為兼備與完整。

謝謝學弟晏銘協助我平日忙碌中所無法完成的事，還有 815 實驗室學弟妹們，胡致暉，阿信，蔡銘裕，李恆毅，楊如璇，陳鵬宇，洪嘉偉，劉志偉，李奕廷，陳彥廷，黃柏蒼，曹文昇，我感受到大家的關心與祝福，也祝福大家順利完成學業。

在求學中兼顧工作若沒有主管支持很難成就，所以非常謝謝沛亨半導體總經理李明儒先生與昔日主管陳繼健先生；聚積科技總經理楊立昌先生與副總吳仲佑先生，還有我的工作夥伴們吳志鈺，李燕婷，李偉任，許紘薰，孫僅，張育倫，信華，雅燕，謝謝大家工作上體諒與幫忙。

為了兼顧研究與工作會忽略很多家庭生活，很感恩一直陪伴我支持我的父母與妻子，謝謝您們讓我無後顧之憂盡心完成學業，還有一直從旁協助我的姊姊們與哥哥，僅將此小小研究成果獻給我摯愛的家人，和關心我的親戚與朋友，同時讓大家一起分享此時的喜悅與榮耀。

劉 興 富

2005 春天 于 新竹交通大學

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CHAPTER 1

INTRODUCTION

1.1 Motivation

A switching mode AC/DC converter can be designed to have high power transfer efficiency. This characteristic enables AC/DC converters to be used as the primary power supplies in modern electronic products, such as personal computers, computer peripherals and test instruments. Furthermore, to suppress the quantities of harmonic current emissions, the AC/DC converters must embed a function with power factor correction or harmonic current reduction.

Usually, the requirements regarding a practical AC/DC converter are expected to have high reliability and cost-effective. Many power management controllers with power factor correction function were designed in the past, but they always used two power-stages with the IC controllers each of which has at least 8 pins, for instance, LT1509/20pins, UCC38517/20pins, FAN4803/8pins, and L4981/20pins. Therefore, their application circuits are kinds of complex. Moreover, power source is usually a critical and necessary one in electronic products, and high quality power is also required too. In another viewpoint, a simple and reliable circuit structure will gain cost-effective benefit in business consideration. Thus, a simpler and reliable circuit structure appears to be an important requirement.

The requirements above may not satisfy to each other. However, there are at least four main demands when designing the converters in wide input range (90~265 Vrms): (i) the line current harmonics must satisfy agency standards, (ii) the primary side dc bus voltage should be less than 450 V/dc to reduce the size of the dc bus capacitor, (iii) the feedback control band width should cover the line frequency to minimize low frequency output ripples and advanced dynamic response, and (iv) the circuit should be simple and flexible to enhance reliability in practical applications.

1.2 Literature Survey

In recent years, many studies have presented the techniques regarding harmonic current correction in ac/dc converters. These proposed solutions could be categorized into two classes. One class yields sinusoidal input line current [1] while the other yields non-sinusoidal input line current [2], [3]. The class with sinusoidal line current has almost a unity power factor but requires a complex topology or control circuit [1], [3] and [4]. Figure 1.1 schematically shows an ac/dc converter belonging to the sinusoidal input line current class.

This kind of converters uses two power conversion stages. The first stage is used to transfer the AC power to a DC output with near unity power factor. The controllers have designed to fit the input ac current waveform to the ac voltage waveform. Under this control strategy the bandwidth of PFC is under 120Hz so dc output voltage doesn't have good regulation [1]. Thus, an extra dc/dc converter is needed to solve the regulation problem and more cost will be required.

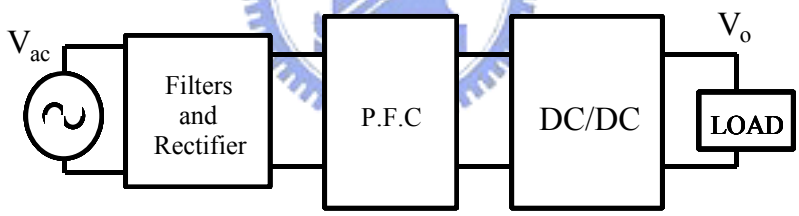


Fig. 1.1 Classical ac/dc converter with PFC function

The other one with non-sinusoidal line current has a simple topology based on a single-stage single-switch. Although they don't provide unity power factor in [5]-[13], they comply with IEC 61000-3-2 class D [6]. A family of such circuits was described in [5]-[13]. The family of circuits often has a common configuration, a boost circuit applied to a dc/dc converter, as shown in Fig. 1.2. This feature successfully simplifies a conventional two-power-stage with power factor corrector into a single-power-stage corrector.

This kind of the converters uses only one switch and one stage circuit. However, their topologies commonly contain two parts; those are the input current shaper [ICS] and the dc/dc

converting circuit. They are driven by one common switch. Through the switch operates the input current shaper, denoted by ICS, pulling in the input power current and the average of the current is determined by the input voltage as long as the ICS conducts. Thus, the power factor will be smaller than one but can be kept to a pretty high value if ICS is designed properly. Simultaneously, the controller in the circuit is only responsible for the dc/dc converter, and the line current is shaped by ICS. Therefore, a conventional controller can be employed in the proposed circuits.

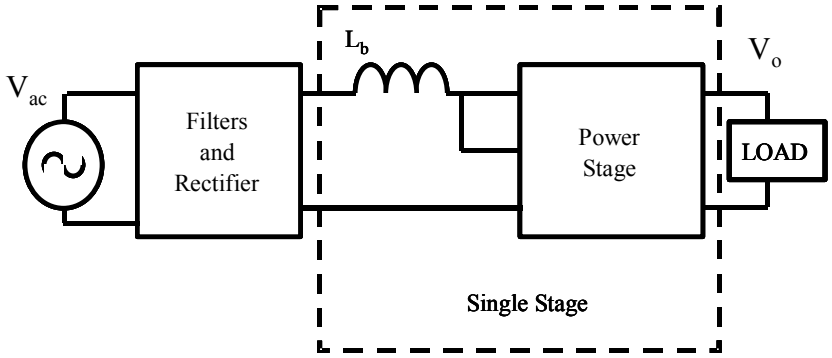


Fig. 1.2 Prior Single Stage ac/dc PFC converter

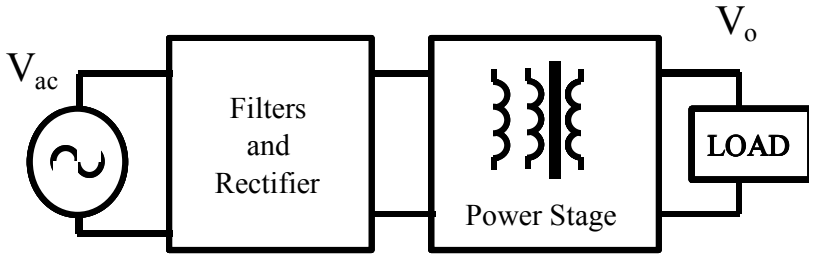


Fig. 1.3 Proposed Single Stage ac/dc converter

Some interested circuits with PFC function are presented in [14]-[16]. In [14], it employs a dither signal to achieve power factor correction and it still needs a bulk inductor in PFC cell. Based on the concept of power-split ratios, reference [15] presents a method to improve

power efficiency with PFC converter but it needs an extra power stage to share a part of power flow. In [16], an auxiliary output of the main converter is used in parallel with the rectified input voltage instead of the series connection and the circuit also has a bulk inductor (~1mH) as the energy transfer component.

There are some papers presented about the single-phase single-stage bridge-type converters with input current shaper. A basic topology for bridge-type converter with input current shaper is presented in [17]-[18]. The circuit suffers from high voltage in dc bus voltage when input voltage is up to 260V in heavy load and low input inductance L_{in}. The circuit presented in [19] is the simplified one from [17]. It also suffers the same issue as [17]. An improved circuit for [19] is presented in [20]. The improved circuit can keep dc bus voltage under 450V in wide line and load range. In [21], it proposes a zero-voltage zero-current-switched full-bridge converter but it still suffers high voltage in dc bus voltage when input voltage is up to 260V in heavy load. A soft-switching mode rectifier (SSMR) consisting of a power factor correction zero-voltage-transition-pulse-width-modulated is presented in [22], the circuit has sinusoidal line current with low harmonics and near unity power factor via special control method. An interested regulator is realized with an asymmetrical PWM control and two coupled inductors, which can achieve ZVS and high power factor in [23]. In [24], an asymmetrical control and synchronous rectification are employed to achieve high power efficiency but a bulk inductor is still in power loop. In [25] and [26], that introduce a lot of topologies which performance can conform to IEC 61000-3-2 class D and still can't avoid to use a bulk inductor in these circuits.

1.3 Contributions of the Dissertation

This study proposes a new converter with the configuration shown in Fig. 1.3. The new converter satisfies the input harmonic current constraints given by IEC 61000-3-2 class D and provides a fast output regulating response. A multi-winding transformer is employed in the proposed converter. This arrangement has three advantages. First, the size of the bulk inductor can be further reduced. Second, the line harmonic currents can be reduced. Third, the phase difference between the fundamental component of the line current and line voltage closely approaches zero. Furthermore, the voltage across the bulk capacitor can be arranged to a reasonable value under 450V/dc by adjusting the turn-ratio of two primary windings. Therefore, this design can adapt to large line voltage variation. Moreover, The switching frequency is fixed in the proposed converters, which benefits the design of transformer and EMI filter. Some valuable and useful EMI considerations are in [27]. The structure and operation principal of a new converter is explained in the following section, and the practical experimental results are shown in sections 3.4 and 4.4.

Based on the proposed concept of input current shaper, the thesis also proposes bridge-type circuits such as full-bridge converter with ICS, asymmetrical half-bridge converter with ICS, and push-pull converter with ICS. These extended circuits have several features described in above section.

1.4 Outline

Chapter 1 introduces the background regarding the study and indicates the practical requirements about ac/dc converter with input current harmonics correction.

Chapter 2 introduces previous studies and explains their features and defects. The survey focus on some selected typical topologies in single-phase ac/dc converter with input current harmonics correction presented in the recent ten years.

Chapter 3 introduces the flyback converter using the proposed input current shaper. The text contains circuit description, operation principle, circuit design procedure, prototype experiment results, and extension circuit in the section.

Chapter 4 depicts the forward converter using the proposed input current shaper. The text also covers several segments same as Chapter 3.

Chapter 5 depicts the full-bridge converter using the proposed input current shaper. The text also covers several segments same as Chapter 3. Besides, half-bridge converter and push-pull converter with input current shaper are simply described in the Chapter.

In Chapter 6, a summary regarding the proposed circuits is described. The purpose of this section is to provide a simple guide to select a suitable circuit in future practical application. A suggested future research about the proposed circuits is coved in this chapter.

CHAPTER 2

A SURVEY OF PREVIOUS SINGLE-STAGE PFC CIRCUITS

2.1 The Familiar Single-Stage Single-Switch PFC Rectifiers

Many papers have been presented about single-stage PFC rectifiers with boost-type ICS in the past ten years. The survey will focus on the topologies of the single-stage PFC rectifiers. Each of them contains a boost ICS and a dc-dc converter in a cascade type. Through the inspection of the locations of the storage capacitors along the energy flow paths in these topologies, two categories were identified [28]. In the first category, the capacitor is in series with transformer. In the other one, the capacitor is in parallel with transformer.

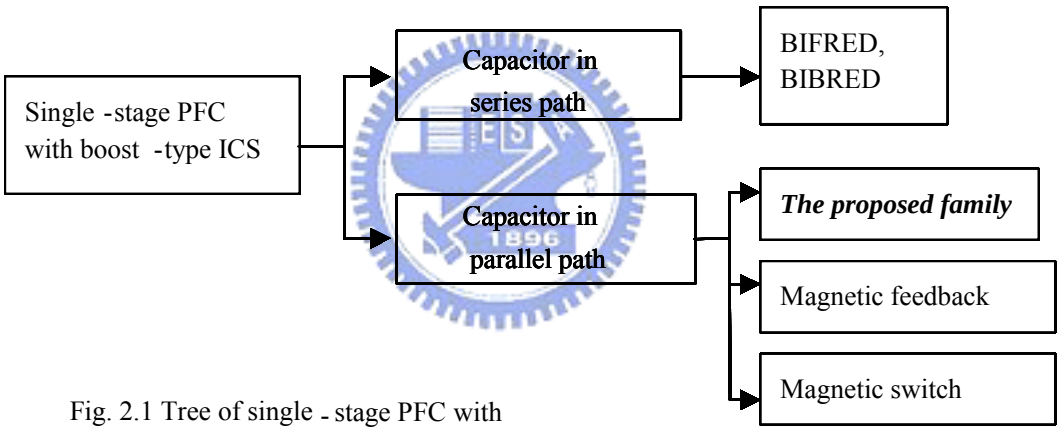


Fig. 2.1 Tree of single - stage PFC with boost - type ICS.

In the topology type of series connection, the bulk capacitor stores and transports energy in series between boost ICS and dc-dc converter. Fig. 2.2 shows the common structure. In this type, [28] proposes BIFRED (Boost Integrated with Flyback Rectifier /Energy Storage/Dc-dc converter) and BIBRED (Boost Integrated with Buck Rectifier /Energy Storage/Dc-dc converter) designs. Both the BIFRED and BIBRED consist of a boost-type ICS cascaded by a flyback converter or a buck converter correspondingly, the two circuits are shown in Fig. 2.3. The ICS in such a circuit is simply implemented by a boost inductor, a diode and switch. The boost cell operates in discontinuous conduction mode (DCM) and the dc/dc cell operates in either DCM or continuous conduction mode (CCM). If the dc/dc converter operates in CCM,

the converter suffers from high voltage stress in the bulk capacitor. Besides, the circuit has a bulk inductor in the boost cell circuit.

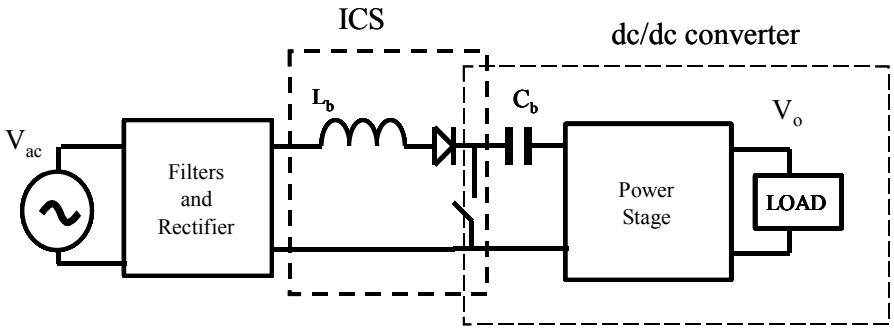
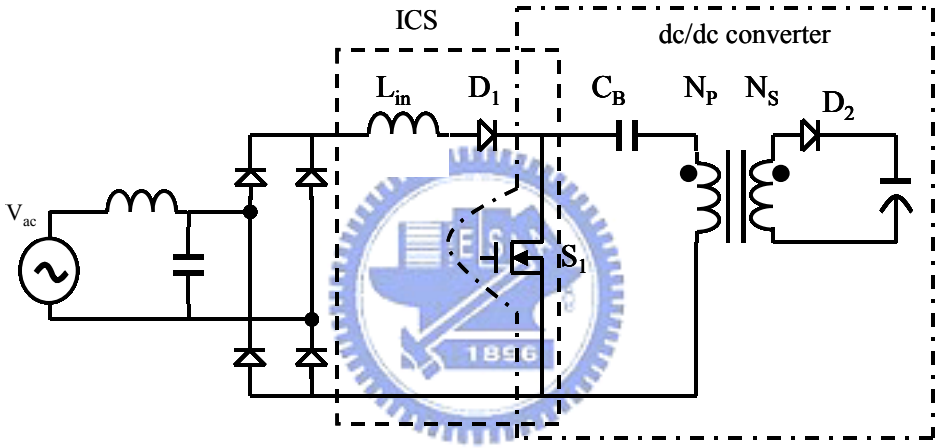
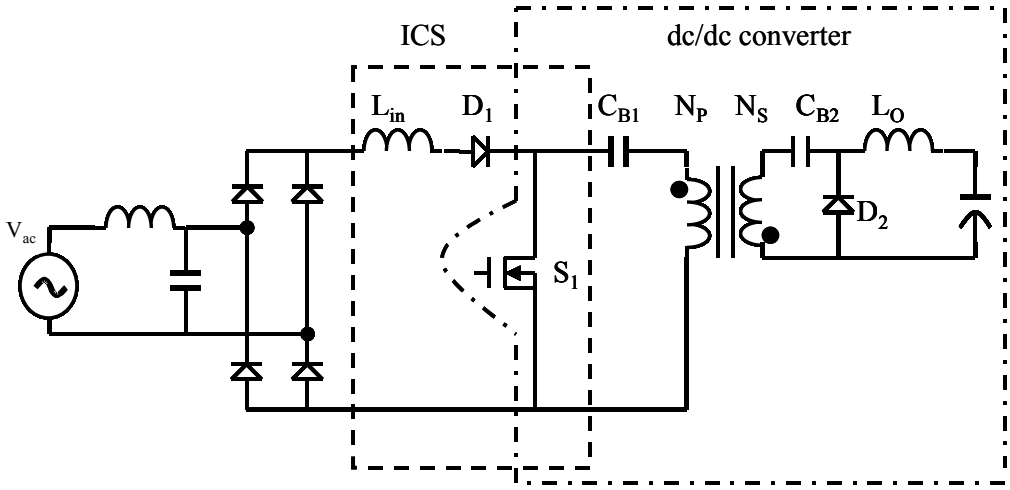


Fig. 2.2 Structure for capacitor in series path.



(a)



(b)

Fig. 2.3 Single-stage PFC characterized by an energy storage capacitor in the series path of the energy flow, (a) BIBRED (b) BIFRED presented in [3].

For the other type, using parallel connection, the bulk capacitance is not in the series path with respect to the transformer in dc-dc converter but in a parallel fashion instead. The corresponding circuit topology has three-terminal structure as shown in Fig. 2.4. The practical circuit shown in Fig. 2.5 (a) is presented by [7]. The boost cell operates in DCM and naturally forms input current shaper and the power factor can achieve 98% when a suitable ratio for L_{in}/L_{N1} is selected. Besides, the dc/dc converter can operate in either DCM or CCM. However, if the dc/dc converter operates in CCM, the voltage across bulk capacitor will vary with the load current. Furthermore, it suffers from high voltage stress under high-line and light-load condition.

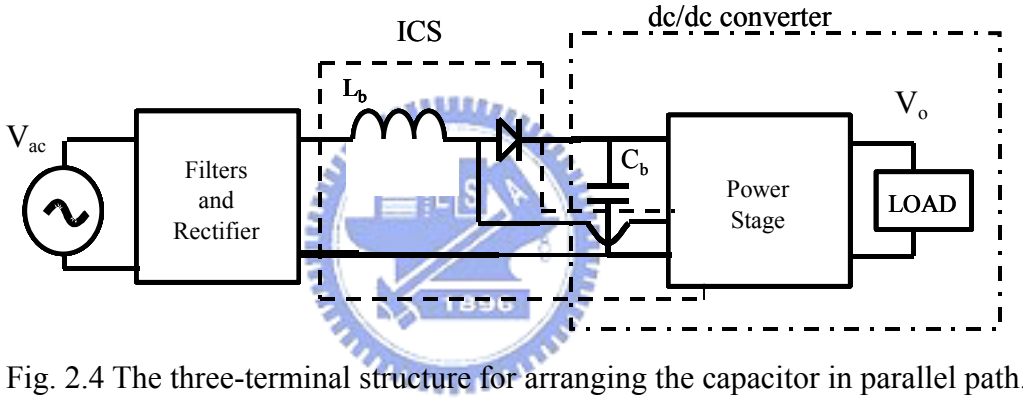
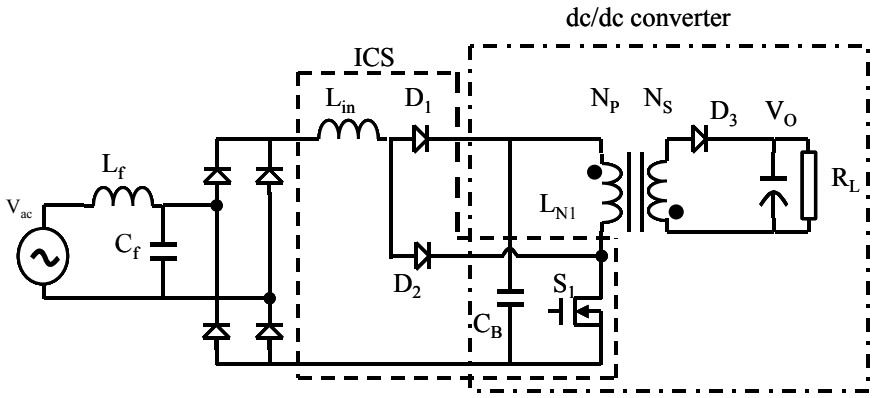
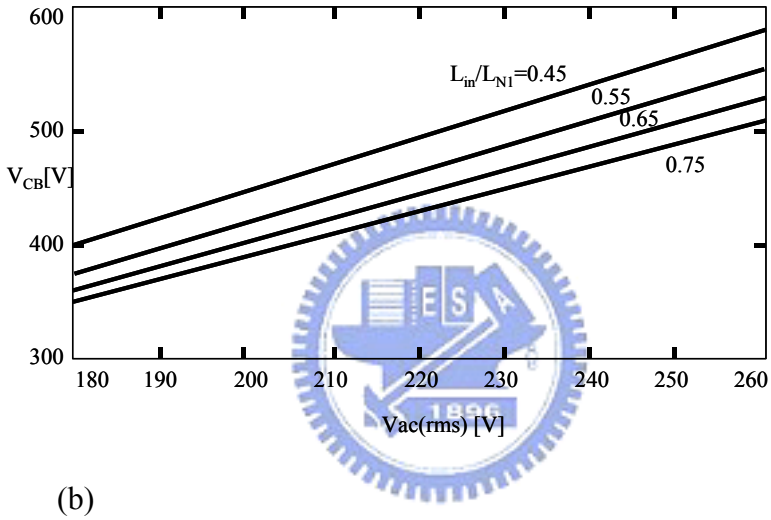


Fig. 2.4 The three-terminal structure for arranging the capacitor in parallel path.



(a)



(b)

Fig. 2.5 The ICS implemented by three-terminal structure [7], (a) circuit, (b) V_{CB} and V_{ac}.

For the circuit shown in Fig. 2.5(a), Fig. 2.5(b) shows that the voltage across bulk capacitor, V_{CB}, will be over 450V/dc when the input voltage approaches 220V/ac and the ratio of L_{in}/L_{N1} is lower than 0.6.

2.2 Circuit Technologies for Reducing the Voltage Stress of Bulk Capacitor

Although the above topologies [7] can achieve high power factor up to 98%, it needs to face the problem of high voltage across bulk capacitor. The high dc-bus voltage presents high stress in bulk capacitor and switching components. A compromising solution was presented in [8], [9], and [29]. A topology using a fashion of negative magnetic feedback is implemented by adding an extra-winding in power transformer, as shown in Figs. 2.6 and 2.7. The winding connecting as a negative magnetic feedback fashion provides another energy flow path. While the bulk capacitance charging the transformer, the ICS also charges the transformer too. Consequently, the voltage of bulk capacitance required to provide the constant output voltage can be reduced. The small trade off is that this solution has smaller power factor. However, it can conform to standard IEC61000-3-2 class D, and the solution can keep the dc bus voltage below 450V.

In [30]-[32], two extra windings in power transformer are added to form magnetic feedback loops and each design consists of a boost cell and a dc-dc converter to operate in CCM as shown in Fig. 2.8. In [33]-[37], a magnetic switch concept is introduced by adding another extra winding in power transformer to further drive boost cell in CCM. The operation in CCM is good for the dc-bus voltage being less affected by the load current The circuits are shown in Figs. 2.9 and 2.10. While the boost cell and dc/dc converter operate in CCM, two gain benefits are presented: lower conduction power loss in switching components and lower switching ripple in input and output sides.

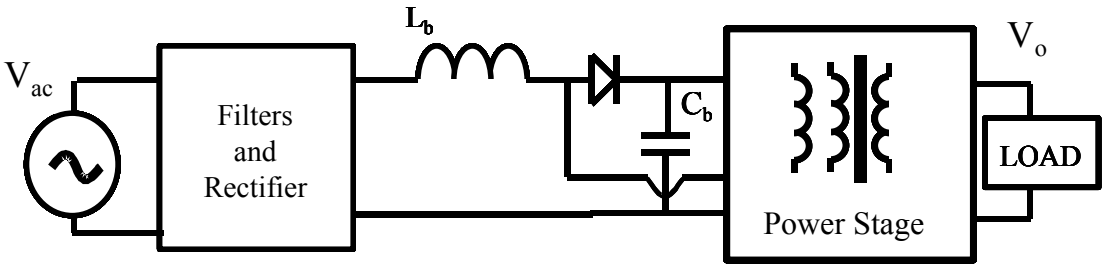


Fig. 2.6 The three-terminal structure for adding an extra winding in power transformer.

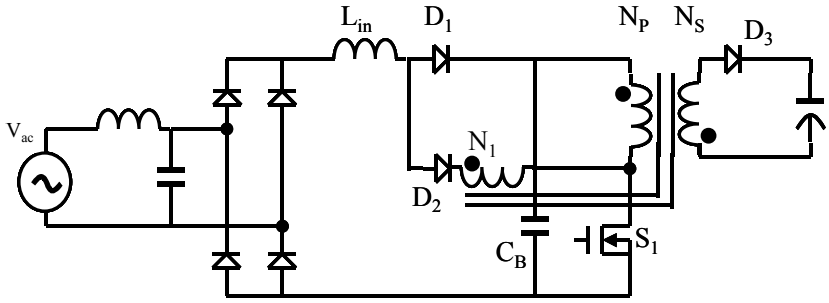


Fig. 2.7 Circuit with an extra winding in transformer [3,10,11].

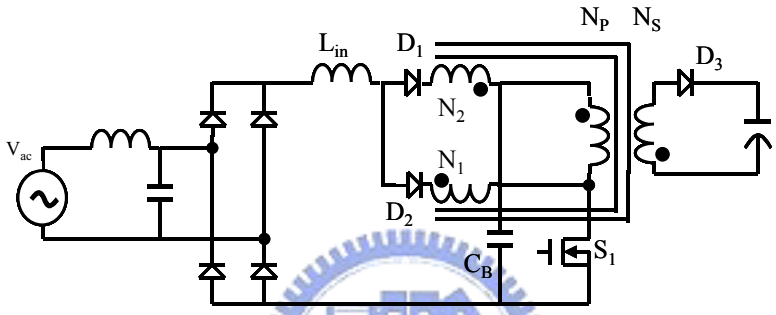


Fig. 2.8 Circuit with two extra windings in transformer [3].

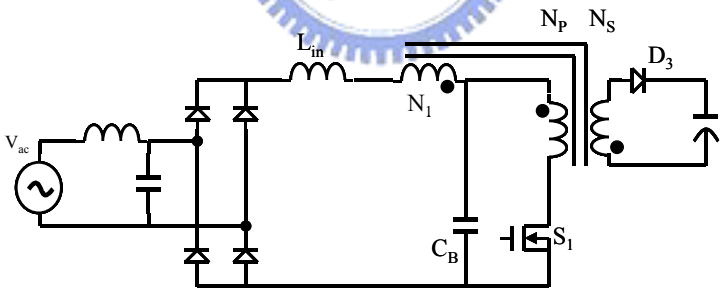


Fig. 2.9 Circuit with magnetic switch winding in transformer [3].

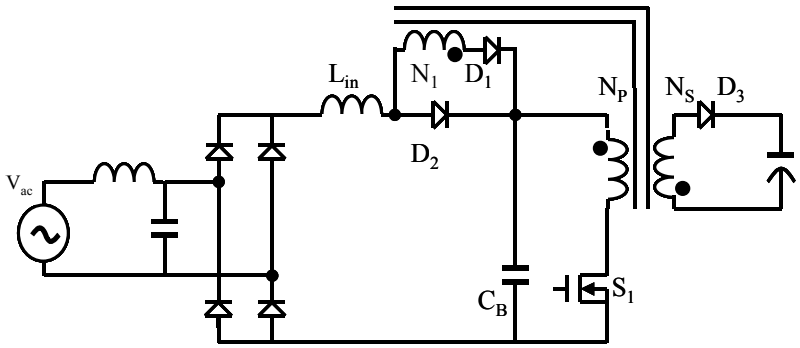


Fig. 2.10 Circuit with magnetic switch winding in transformer [3].

2.3 The Proposed New Design for Reducing the Voltage Stress of Bulk Capacitor

The converters mentioned in last section are related single stage PFC rectifiers with ICS function. They successfully reduce the voltage stress of bulk capacitor by employing one or more windings connected in a fashion of negative magnetic feedback or magnetic switch. Although the negative feedback magnetic winding is added to power transformer, they still need to use bulk inductors L_b (or L_{in}) in boost cell to achieve the ICS function.

The single-stage converter designed with three-terminal parallel structure as shown in Fig. 2.5(a) is a pretty flexible design. Many improved ICS designs are based on this structure. In this structure, two current flow paths are implemented through diodes D_1 and D_2 respectively. The new design proposed in this dissertation is also based on the circuit of Fig. 2.5(a) with a negative magnetic feedback design. The design concept is shown in Fig. 2.11. In the proposed topology, the bulk inductor of boost cell, L_{in} shown in Fig. 2.11, is replaced by adding an extra winding N_1. The extra winding is implemented in the power transformer and connected in a negative magnetic feedback structure so that the goal for reducing the dc bus voltage can be reached. To complete the ICS function a small inductor L_1 sketched by a dotted line in Fig. 2.11 is added. Since the inductance of L_1 is smaller than one-tenths of L_{N1} in the proposed design, it can be implemented by the leakage inductance of the winding N_1 in low power application. Therefore, the total volume of magnetic material can be reduced via the new design.

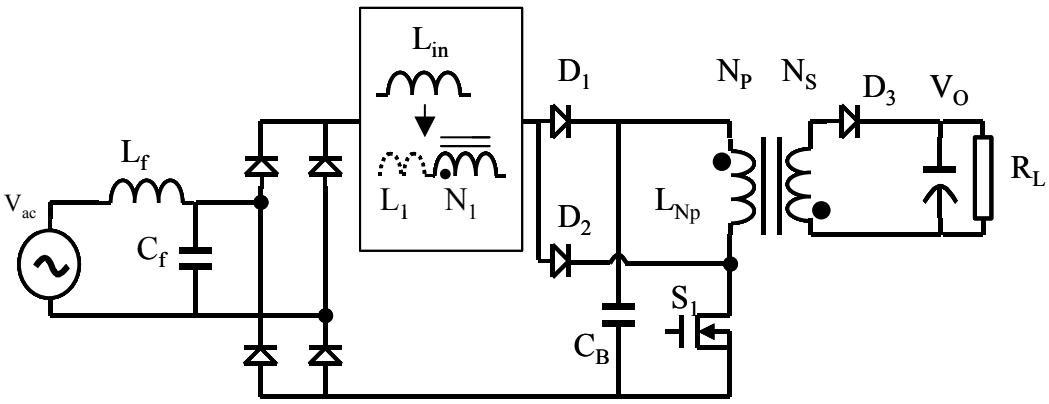


Fig. 2.11 The schematic to obtain the proposed design.

In the new design, the winding number N_1 is greater than that in the circuit like Fig. 2.7 so that the power input loop is in reverse bias within the switch on duration instead of using the switch on operation in the those converters mentioned above. By this design L_{in} can be removed. Winding N_1 operates as a magnetic switch in the switch off duration and provides a power-in loop. However, a small L_1 is needed to obtain controllable and satisfying ICS function and also guarantee the reduction of the voltage of the bulk capacitance. Another function of inductor L_1 is that L_1 can provide soft-switching-on for diode D_1 and soft-switching-off for diode D_2.

The alternative sketch of the proposed circuit is shown in Fig. 2.12. Although it looks like the ICS shown in Fig. 2.7, the location of winding N_1 and the operation theorem are different. In Fig. 2.7 the bulk inductance L_{in} is magnetized in the switch on duration and demagnetized in the switched off duration. In the proposed design, the timing is converse. In Fig. 2.7 the ratio N_1/N_P has to be smaller than that in the proposed one in order to achieve a better power factor. In the proposed design, a larger ratio N_1/N_P is used to achieve higher power factor. Therefore, a better voltage reduction of V_{CB} can be achieved in the proposed circuit. Furthermore, the inductor L_{in} of Fig. 2.7 can not be substituted by leakage inductor of winding N_1 in low power application because the inductor L_{in} and winding N_1 are not in series.

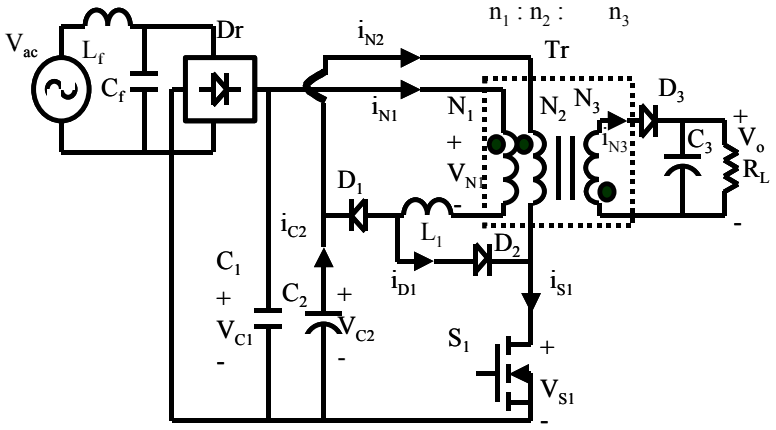


Fig. 2.12 Proposed simple flyback AC/DC converter

The design considerations of the proposed circuit are trying to conform to the four main demands indicated in page 1 of chapter 1. The additional winding N_1, which can functionally

replace the bulk inductor, has successfully simplified the circuit of Fig. 2.5 into Fig. 2.12.

The input current shaper consists of winding N_1, inductor L_1, diodes D_1, D_2 and switch S_1 in Fig. 2.12. The average current of i_{N1} will automatically track the rectified input voltage V_{C1} at the time period when the voltage, $V_{C1}+V_o(n_1/n_3)$, is greater than V_{C2}. The automatically shaping feature of the line current can save a current shaping controller. In the proposed circuit needs only one controller to regulate the output voltage of dc/dc cell as that in the conventional dc/dc converter. Therefore, the feedback control bandwidth is designed to cover two times of the line frequency to minimize the line frequency output ripple and simultaneously enhance the output dynamic response.

Through the charging operation for capacitance C_2, the voltage of V_{C2} will be smaller than the voltage, $V_m+V_o(n_1/n_3)$, when dc/dc cell operates in CCM. Actually while the line voltage arises from zero, the current i_{N1} will keep zero until the line voltage arises to a level so that $V_{C1}+V_o(n_1/n_3)$ approaches V_{C2}. The nonzero i_{N1} will charge the capacitance C_2 and produce a high voltage V_{C2}. It is worthy to mention that the proposed extra winding N_1 is also good for reducing the voltage V_{C2} especially in light load. When the load changes from a heavy one to a light one, the output current will reduce to zero earlier and consequently the charging time and charging current will be reduced too. Therefore, the voltage V_{C2} will not increase as much as what happens in the conventional BIFRED converters. Through using a suitable ratio n_1/n_3 V_{C2} can be controlled lower than 450V in wide range input voltage. A detailed description is depicted in the following chapters.

2.4 The Design consideration for choosing DCM and/or CCM Operations

The operation mode has a significant effect for single-stage PFC rectifiers. It can manipulate the voltage and current stress of the storage and switching components, the PF value, and even the power loss along the energy flow paths. Basically, a single stage PFC

rectifier consists of boost cell and dc/dc converter as described in last sections. The boost cell may operate in DCM shown in Fig 2.13 or CCM shown in Fig 2.14, and so does dc/dc cell. The choice of mode operation is determined by the strategies of the designer. Lowering the power dissipation is often one of the considerations.

Typically, two kinds of power losses may present in the circuits such as, conduction loss and switching loss. In ac/dc converter, the input port is always high voltage and small current. Thus, the main power loss is switching loss rather than conduction loss in the boost cell. Therefore, the boost cell in DCM is preferable because the switching loss of main switch can be reduced through soft switching design. Furthermore, the line current can naturally trace line voltage and forms a quasi-sine waveform simultaneously. The power loss of the $R_{ds,on}$ of main switches is usually to be less than 5W while MOSFET's $R_{ds,on}$ resistor is smaller than 1 Ohm in the application condition below 500W output power. That means the major power loss of MOSFET (main switch) is switching loss rather than conduction loss when application is below 500W output. Furthermore, the L-C filter in AC input port can filter switching ripple existed from the line current in real application as boost cell does in DCM. To the dc/dc cell, CCM operation is preferable due to the consideration of output voltage ripple. Because the dc/dc output voltage connects to digital or analog control circuits in general application, these control circuits are sensitive to switching noise.

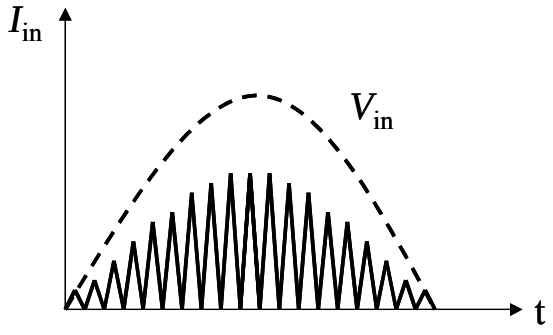


Fig. 2.13 Line current in DCM waveform

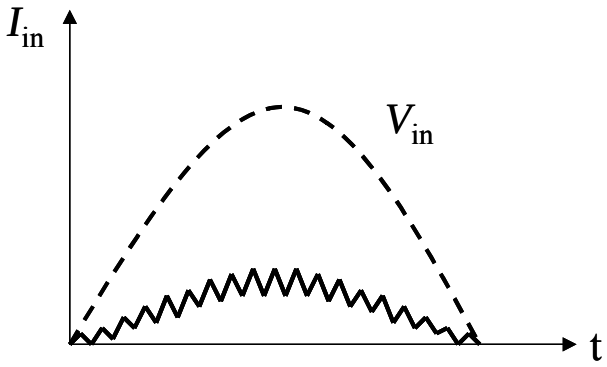


Fig. 2.14 Line current in CCM waveform

In [5] and [25], the boost cell and dc/dc cell are arranged to operate in DCM. Otherwise, the voltage of bulk capacitor (or dc bus voltage) may be arisen higher than 500V when dc/dc cell operates in CCM and in wide range input application. Under the CCM operation the dc-bus voltage will vary with the load current. In the steady state, the switch's duty cycle is constant in CCM when the energy stored in bulk capacitor via AC voltage source is equal to the energy transferring to output load in a half-cycle of the ac-line voltage. The dc-bus voltage will increase when load current decreases and results in the reduction of the switching duty cycle and inequality quantity of energy transferred between line-to-bulk-capacitance and bulk-capacitance-to-load. Consequently, the new balance dc-bus voltage becomes higher.

2.5 International Standard IEC 61000-3-2 Class D

While a power sets are design, the power quality must be controlled. Thus, in the international society, some standards for measuring the power quality are published. One of the important standards is the International Standard IEC 61000-3-2. The outline of it is briefly mentioned as follows.

For the purpose of harmonic current limitation, equipment is classified as follows:

Class A: - Balanced three-phase equipment;

- Household appliances, excluding equipment identified as class D;
- Tools, excluding portable tools;
- Dimmers for incandescent lamps;
- Audio equipment.

Class B: Portable tools, arc welding equipment, including dimming device.

Class C: Lighting equipment, including dimming device.

Class D: Equipment having a specified power according to 6.2.2 (the item shown in IEC 61000-3-2) less than or equal to 600 W of the following types:

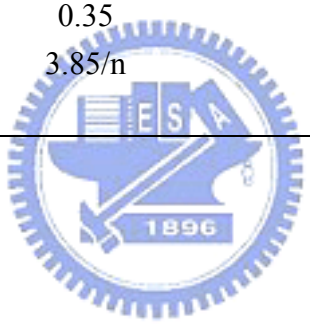
- Personal computers and personal computer monitors;

- Television receivers.

The converters proposed in this thesis shall be of the power sets applied in modern electronic products, such as personal computers, computer peripherals, and television receivers. All these electronic products' input power is less than 600W. Therefore, the experimental results will be criticized by employing the standard class D, which gives the current limits for eleven major harmonics as shown in Table 2.1.

Table 2.1 Limits for class D equipment

Harmonic order n	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13 ≦ n ≦ 39(odd harmonics only)	3.85/n	0.21, 15/n when n≧15



CHAPTER 3

THE FLYBACK CONVERTER USING THE PROPOSED INPUT CURRENT SHAPER

Figure 3.1 shows the proposed new flyback ac/dc converter with harmonic current correction function and tight output regulation. The circuit is a single-stage single-switch ac/dc converter, which comprises single switch S_1, an input filter L_f, C_f and C_1, a bulk capacitor C_2, a soft-switching inductor L_1 and a transformer with two primary windings N_1 and N_2. The winding N_1, inductor L_1, diode D_1 and D_2 form an input current shaper cell. Besides, the winding N_1, inductor L_1, diode D_1 and D_2, switch S_1, and bulk capacitor C_2 comprise a boost circuit. The winding N_2 and N_3, bulk capacitor C_2, switch S_1, diode D_3 and output capacitor C_3 form a flyback converter.

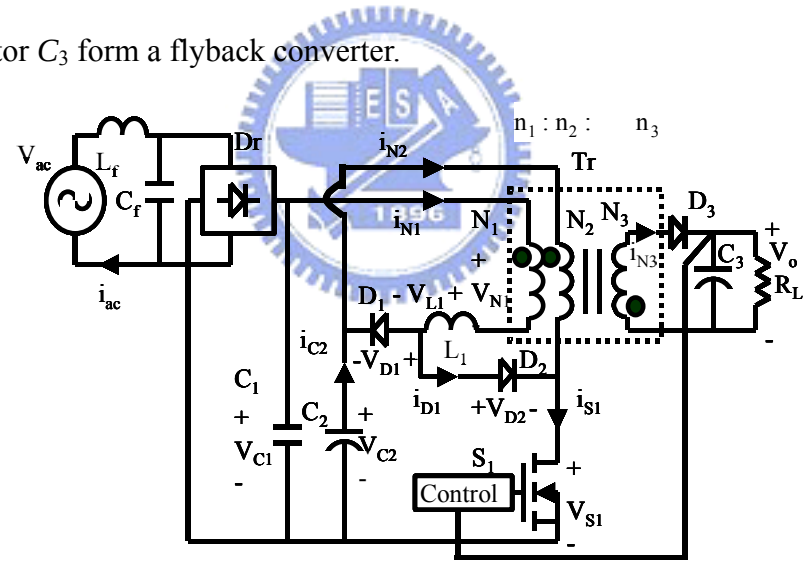


Fig. 3.1 Proposed flyback AC/DC converter with ICS

The function of inductor L_1 in the proposed circuit is different from that of the boost inductor presented in the converters of [2]-[10]. Actually, L_1 provides partial soft switching functions for diodes D_1 and D_2, to suppress the harmonic current by increasing the conduction time for i_{ac} from time t_1 to t_5 in Fig. 3.2, and to reduce the voltage V_{C2} across the bulk capacitor.

The inductor L_1 has a soft-switching function on D_1 and D_2, as mentioned in [12]. Figure 3.3 shows that when S_1 turns off, D_2 changes to reverse bias and proceed soft off since the current i_{N1} has gradually reduced to zero at the reverse bias time $t_{1,M3}$ or $t_{1,M2}$. Therefore, to overcome the problem of the reverse recovery effect of D_2, a suitable inductance of L_1 must be selected. Contrarily, D_1 softly turns on when the current i_{N1} gradually increases from zero at time $t_{2,M2}/t_{2,M3}$.

The winding N_1 provides the voltage-boost function for bulk capacitor C_2 during the period from t_1 to t_5, as illustrated in Fig. 3.2. During this period, when S_1 turns off, D_1 turns on and the charge current flows from the power line source to C_2 through N_1, L_1, and D_1. At this moment, the residue magnetic energy stored in the transformer will also induce current i_{N3} as a falling ramp waveform, as illustrated in Fig. 3.3. Furthermore, the increasing current i_{N1} keeps storing the magnetic energy in L_1. The magnetic energy stored in L_1 passes to winding N_2 through winding N_1, and induces a portion of current i_{N2} when S_1 is turned on.

The turns-ratio, n_1/n_2, of the transformer can determine not only the starting conduction angle of the line current but also the voltage across a bulk capacitor C_2. Furthermore, the inductance and volume of L_1 are significantly smaller than the primary windings N_1 or N_2 of the transformer.

The control circuit can be designed by using a fixed-frequency simple voltage-mode control or a conventional peak-current control. The experiment results have demonstrated that even using a simple control method, the line current of the proposed AC/DC converter can comply with the standard IEC 61000-3-2, and the converter also provides fast load dynamic response.

3.1 Basic Operation Theories

The fundamental operating principle of the proposed converter is to store the magnetic energy in windings N_2 when switch S_1 turns on, and then to deliver it to bulk capacitor C_2 and secondary winding N_3 when switch S_1 turns off. The entire operation principle of the circuit can be explained in three operation modes. Figure 3.2 shows six operation modes in a line cycle. Only three modes are left after combining the similar modes, namely M_1/M_6, M_2/M_5 and M_3/M_4. Figure 3.3 shows the main current and voltage waveforms in every mode.

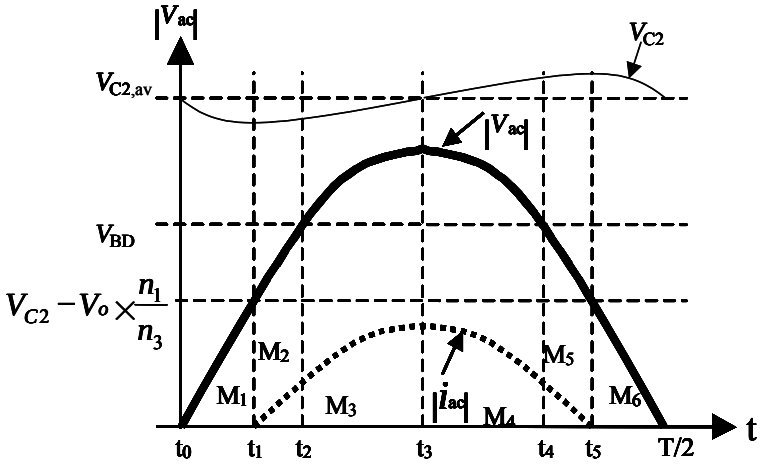


Fig. 3.2 Operation modes in proposed flyback converter

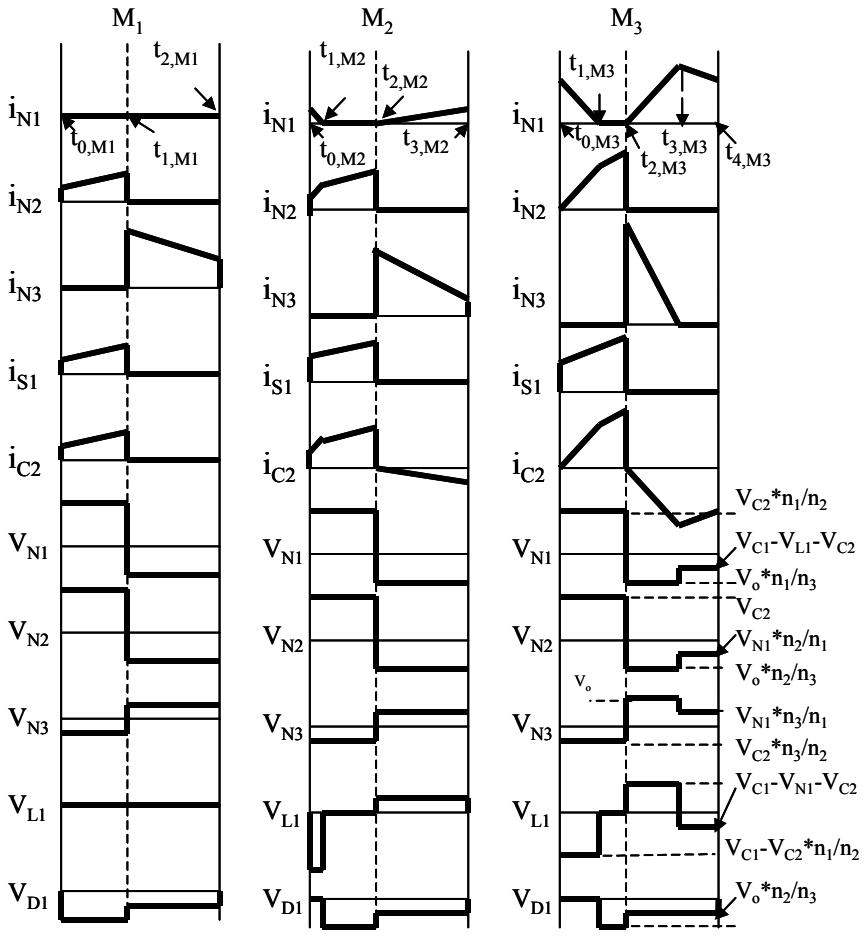


Fig. 3.3 Current and voltage waveforms in a switching cycle in *M*1~*M*3.

3.1.1 Operation Modes M_1 (t_0 ,t_1) and M_6 (t_5, T/2)

This mode holds when $0<|V_{ac}|<V_{c2}-V_o\times(n_1/n_3)$. Currents $|i_{ac}|$ and i_{N1} have not yet been induced. The converter operates as a conventional flyback converter. Figure 3.4 shows the current conducting path in mode M_1/M_6 with S_1 turned on and off. Figure 3.4 shows that the transformer does not sink the current from the power line. Rather, the converter sinks the current from the bulk capacitor C_2. V_{C2} shows the voltage across on C_2 and is approximated to a constant value during a line cycle in the steady state and can be obtained as follows:

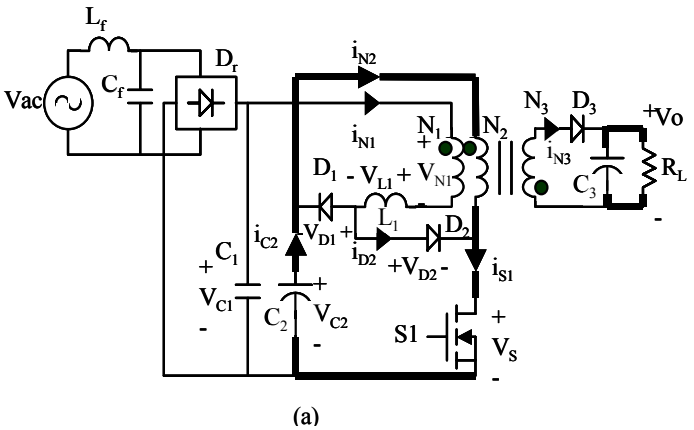
$$V_{C2} \le |V_m| + \frac{V_o\ n_1}{n_3}, \tag{3.1}$$

where $|V_{ac}|=V_m|\sin(\omega t)|$.

The voltage-second balance criterion is applied to the flyback transformer, and thus the total voltage-second should be zero in one time period in steady state. Additionally, another required assumption is that the flyback transformer operates in the CCM mode such that

$$V_{C2} = \frac{n_2 V_o (1-D)}{n_3 D} \quad \text{Or} \quad D = \frac{V_o\ n_2}{V_o\ n_2 + V_{C2}\ n_3}, \tag{3.2}$$

where n_1, n_2 and n_3, are the number of turns used in winding N_1, N_2, and N_3.



(a)

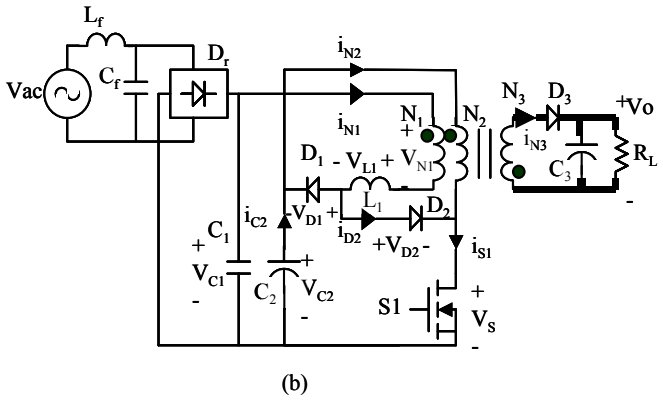


Fig 3.4 Current loop in mode M_1: (a) $t_{0,M1} \le t < t_{1,M1}$, S_1 turns on (b) $t_{1,M1} \le t < t_{2,M1}S_1$, turns off

From equation (3.1) and (3.2) the boundary time of M_1 can be obtained by

$$\omega t_1 = \sin^{-1}\left[\frac{V_o}{V_m} \cdot \frac{n_2}{n_3}\left(\frac{1-D}{D} - \frac{n_1}{n_2}\right) \right] \tag{3.3}$$

Let

$$k = i_{N3}(t_{2,M1}) / i_{N3}(t_{1,M1}) \tag{3.4}$$

Then k is in the range, $0< k< 1$.

Integrating the winding inductor voltages of V_{N2} and V_{N3} over the duty on and off periods yields

$$i_{N2} = \begin{cases} i_{N2}(t_{0,M1}) + (t - t_{0,M1})\dfrac{V_{C2}}{L_{N2}}, & t_{0,M1} < t \le t_{1,M1} \\ 0, & t_{1,M1} < t \le t_{2,M1} \end{cases} \tag{3.5}$$

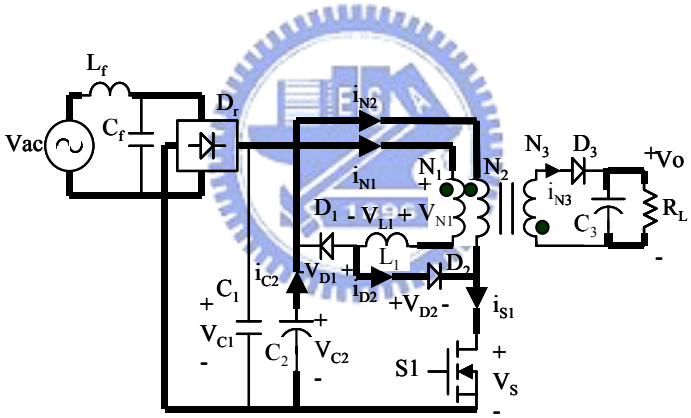
$$i_{N3} = \begin{cases} 0, & t_{0,M1} < t \le t_{1,M1} \\ i_{N2}(t_{1,M1})\dfrac{n_2}{n_3} - (t - t_{1,M1})\dfrac{Vo}{L_{N3}}, & t_{1,M1} < t \le t_{2,M1} \end{cases} \tag{3.6}$$

3.1.2 Operation Modes $M_2(t_1, t_2)$ and $M_5(t_4, t_5)$

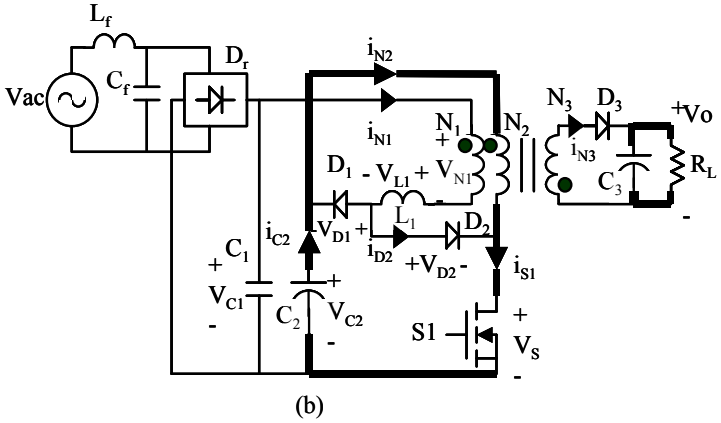
This mode holds when $V_{c2} - V_o \times (n_1/n_3) < |V_{ac}| < V_{BD}$. In the duty on period, D_2 turns on and current i_{N1} flows through the winding N_1, L_1, D_2 and S_1. Simultaneously, C_2 discharges via

winding N_2 and S_1. The conducting paths are as shown in Figs. 3.5(a) and (b) since the induced voltage V_{N1} exceeding $|V_{ac}|$, i_{N1} is none zero current initially, as displayed in Fig. 3.5(a) and reduces to zero linearly and then continues to be zero, as shown in Fig. 3.5(b).

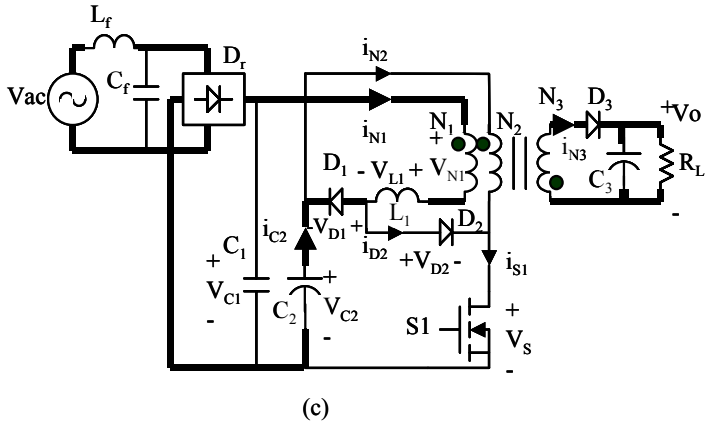
When S_1 turns off, V_{N1} causes i_{N1} to flow via winding N_1, L_1 and D_1 and to charge the bulk capacitor C_2. Simultaneously, D_3 turns to on state and delivers the magnetic power to the output circuit, as shown in Fig. 3.5(c). The conduction of D_3 causes the output capacitor connected to two terminals of winding N_3. Therefore, the output current i_{N3} linearly reduces during the duty off period. In this operation, i_{N3} is nonzero even at the end of the duty-off period. Consequently, in mode M_2 the current i_{N3} of winding N_3 operates in the continuous current mode, denoted by CCM. Based on the CCM of i_{N3} and voltage-second balance, the duty ratio D is the same as that in mode M_1/M_6.



(a)



(b)



(c)

Fig 3.5 Current loop in mode M_2:(a) $t_{0,M2} \le t < t_{1,M2}$, S1 turns on (b) $t_{1,M2} \le t < t_{2,M2}$, S1 turns on (c) $t_{2,M2} \le t < t_{3,M2}$, S1 turns off.

Integrating the voltages of the winding inductors of V_{N1}, V_{N2}, and V_{N3} yields the following winding currents:

$$i_{N1} = \begin{cases} i_{N1}(t_{0,M2}) + (t - t_{0,M2}) \cdot \dfrac{V_{C1} - V_{N1}}{L_1}, & t_{0,M2} < t \le t_{1,M2}. \\ 0, & t_{1,M2} < t \le t_{2,M2}. \\ (t - t_{2,M2}) \cdot \dfrac{V_{C1} + \dfrac{n_1}{n_3} \cdot V_o - V_{C2}}{L_1}, & t_{2,M2} < t \le t_{3,M2}. \end{cases} \tag{3.7}$$

$$i_{N2} = \begin{cases} i_{N2,M2}(t), & t_{0,M2} < t \le t_{1,M2} \\ i_{N2,M2}(t_{1,M2}) + (t - t_{1,M2}) \cdot \dfrac{V_{C2}}{L_{N2}}, & t_{1,M2} < t \le t_{2,M2} \\ 0, & t_{2,M2} < t \le t_{3,M2} \end{cases}, \tag{3.8}$$

where $i_{N2,M2}(t_{1,M2})$, the magnetic current appearing in winding N_2, comes from three sources, $(n_3 / n_2) \times i_{N3}(t_{3,M2})$ provided from winding N_3, $(V_{C2}/L_{N2})\Delta t$ generated in winding N_2 during the duty on period, and $[(V_{N1}\text{-}V_{C1})\Delta t]/L_1$ generated in winding N_1 and determined by L_1 during the duty on period. The resulting formula is obtained as

$$i_{N2,M2}(t) = (t - t_{0,M2}) \cdot \left[\frac{V_{N1} - V_{C1}}{L_1} \cdot \frac{n_1}{n_2} + \frac{V_{C2}}{L_{N2}} \right] + \frac{n_3}{n_2} \cdot i_{N3}(t_{3,M2})$$

$$i_{N3} = \begin{cases} 0 & t_{0,M2} < t \le t_{2,M2} \\ i_{N3,M2}(t) & t_{2,M2} < t \le t_{3,M2} \end{cases}, \tag{3.9}$$

and $i_{N3,M2}(t) = i_{N2}(t_{2,M2}) \cdot \frac{n_2}{n_3} - (t - t_{2,M2}) \cdot \frac{V_o}{L_{N3}} - i_{N1} \cdot \frac{n_1}{n_3}$.

3.1.3 Boundary condition between CCM and DCM

The boundary between CCM and DCM occurs just as i_{N3} reaches zero at the end of the switching period. Since the capacitance of C_2 is large, the value of the voltage V_{C2} is almost kept constant. Throughout the M_2 period, when S_1 is in the off period, the N_1 current generated by the line power increases, and accelerates the decrease of i_{N3} according to Ampere's law. If the duty ratio remains unchanged in Mode M_2, then the current $i_{N1}(t_{3,M2})$ at the end of M_2 equals the current $i_{N3}(t_{2,M1}) \times (n_3/n_1)$ at the end of mode M_1. This approximation yields

$$\begin{aligned} i_{N1}(t_{3,M2}) &= T_s(1-D) \cdot \frac{V_{BD} + \frac{n_1}{n_3} \cdot V_o - V_{C2}}{L_1} \\ &= i_{N3}(t_{2,M1}) \cdot \frac{n_3}{n_1} \\ &= I_{pk} \cdot k \cdot \frac{n_3}{n_1} \\ &= I_o \cdot \frac{2}{1-D} \cdot \frac{k}{1+k} \cdot \frac{n_3}{n_1} \end{aligned}, \tag{3.10}$$

where I_{pk} is actually $i_{N3}(t_{1,M1})$, I_o is the load current, which can be obtained from averaging $i_{N3,M2}(t)$.

$$I_o = (1-D)\left[I_{pk} \frac{(1+k)}{2} \right]$$

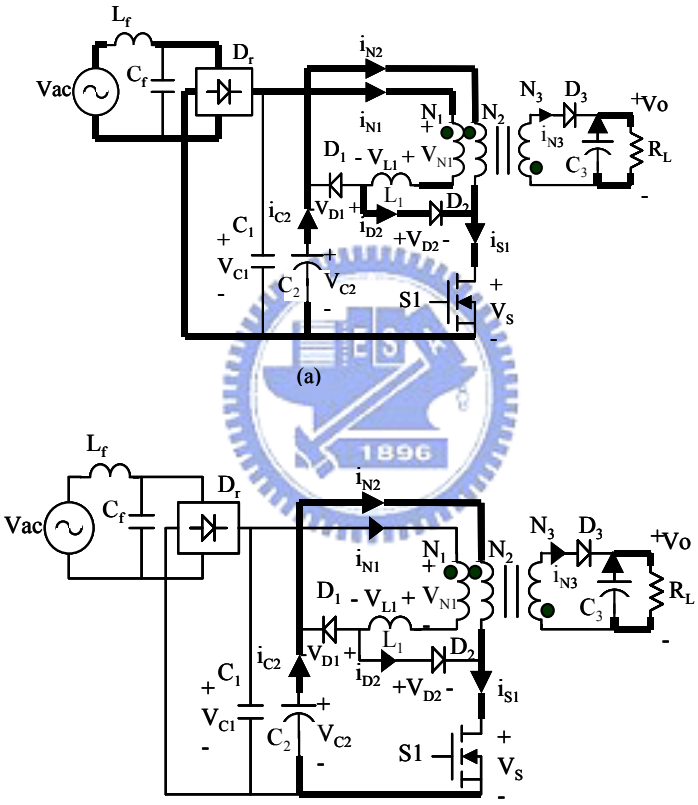
At the boundary, $|V_{ac}|$ is denoted by V_{BD}, which can be obtained by

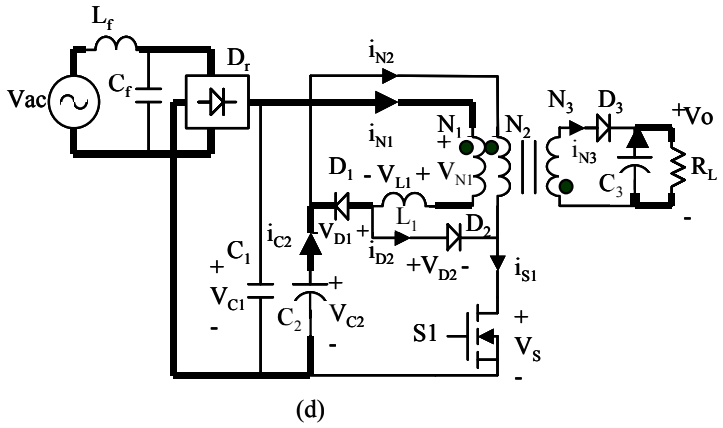
$$\begin{aligned} V_{BD} &= V_m \sin(\omega t_2) \\ &= V_{C2} - V_o \cdot \frac{n_1}{n_3} + I_o \cdot \frac{2kL_1 n_3}{T_s(1-D)^2(1+k)n_1} \end{aligned}, \tag{3.11}$$

where $k = i_{N3}(t_{2,M1}) / i_{N3}(t_{1,M1})$ then k is in the range $0 < k < 1$.

3.1.4 Operation modes $M_3(t_2, t_3)$ and $M_4(t_3, t_4)$

This mode holds when $V_{BD} < |V_{ac}| < V_m$. The large current i_{N1} increases the rate of decay of i_{N3}. The current i_{N3} falls to discontinuous current mode (DCM) in this operational mode. Figure 3.6 shows four different current flow paths in a switching cycle. The energy stored in winding N_2 during the duty on period of S_1 are distributed to the winding N_1 and winding N_3 in the duty off time period. During a switching cycle, i_{N1} and i_{N2} are ruled as in mode M_2/M_5. However, i_{N3} reduces to zero before the end of the duty off period of S_1.





(d)

Fig. 3.6 Current loops in mode M_3: (a) $t_{0,M3} \le t < t_{1,M3}$, S_1 turns on (b) $t_{1,M3} \le t < t_{2,M3}$, S_1 turns on (c) $t_{2,M3} \le t < t_{3,M3}$, S_1 turns off (d) $t_{3,M3} \le t < t_{4,M3}$, S_1 turns off

The winding currents and voltages of inductor L_1 and transformer are given as follows:

$$i_{N1} = \begin{cases} i_{N1}(t_{0,M3}) + t \cdot \dfrac{V_{C1} - V_{N1}}{L_1}, & t_{0,M3} < t < t_{1,M3} \\ 0, & t_{1,M3} < t < t_{2,M3} \\ (t - t_{2,M3}) \cdot \dfrac{V_{C1} + \dfrac{n_1}{n_3} \cdot V_o - V_{C2}}{L_1}, & t_{2,M3} < t < t_{3,M3} \\ i_{N1}(t_{3,M3}) + (t - t_{3,M3}) \cdot \dfrac{V_{L1}}{L_1}, & t_{3,M3} < t \le t_{4,M3} \end{cases} \tag{3.12}$$

$$i_{N2} = \begin{cases} i_{N2,M3}(t), & t_{0,M3} < t \le t_{1,M3} \\ i_{N2}(t_{1,M3}) + \left(t - t_{1,M3}\right) \cdot \dfrac{V_{C2}}{L_{N2}}, & t_{1,M3} < t \le t_{2,M3} \\ 0, & \textit{othwise} \end{cases}, \tag{3.13}$$

where

$$i_{N2,M3}(t) = (t - t_{0,M3}) \cdot \frac{V_{N1} - V_{C1}}{L_1} \cdot \frac{n_1}{n_2} + (t - t_{0,M3}) \cdot \frac{V_{C2}}{L_{N2}} \cdot$$

$$i_{N3} = \begin{cases} i_{N2}(t_{2,M3}) \cdot \dfrac{n_2}{n_3} - i_{N1}(t) \cdot \dfrac{n_1}{n_3} - (t - t_2) \cdot \dfrac{V_o}{L_{N3}}, & t_{2,M3} < t \le t_{3,M3} \\ 0, & \text{otherwise} \end{cases} \tag{3.14}$$

$$V_{N1}=\begin{cases} V_{C2}\cdot\dfrac{n_1}{n_2}, & t_{0,M3}<t\le t_{2,M3} \\ -V_O\cdot\dfrac{n_1}{n_3}, & t_{2,M3}<t\le t_{3,M3} \\ V_{C1}-V_{L1}-V_{C2}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{3.15}$$

$$V_{N2}=\begin{cases} V_{C2}, & t_{0,M3}<t\le t_{2,M3} \\ -V_O\cdot\dfrac{n_2}{n_3}, & t_{2,M3}<t\le t_{3,M3} \\ V_{N1}\cdot\dfrac{n_2}{n_1}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{3.16}$$

$$V_{N3}=\begin{cases} -V_{C2}\cdot\dfrac{n_3}{n_2}, & t_{0,M3}<t\le t_{2,M3} \\ V_o, & t_{2,M3}<t\le t_{3,M3} \\ -V_{N1}\cdot\dfrac{n_3}{n_1}, & t_{3,M3}<t\le t_{4,M3} \end{cases} \tag{3.17}$$

$$V_{L1}=\begin{cases} V_{C1}-V_{N1}, & t_{0,M3}<t\le t_{1,M3} \\ 0, & t_{1,M3}<t\le t_{2,M3} \\ V_{C1}-V_{N1}-V_{C2}, & t_{2,M3}<t\le t_{3,M3} \\ \dfrac{V_{L1,3-4}}{(1-D-\widetilde{F})}, & t_{3,M3}<t<t_{4,M3} \end{cases}, \tag{3.18}$$

$$(h\text{int}:\widetilde{F}=\frac{t_{3,M3}-t_{2,M3}}{Ts})$$

where V_{L1} is calculated via the law of the conservation of voltage-second for L_1 in a switching cycle.

$$V_{L1}(1-D-\widetilde{F})=[V_{C2}\frac{n_1}{n_2}-V_{C1}]\widetilde{D}-[V_{C1}+V_o\frac{n_1}{n_3}-V_{C2}]\widetilde{F}$$

$$\Rightarrow V_{L1,3-4}=[V_{C2}\frac{n_1}{n_2}-V_{C1}]\widetilde{D}-[V_{C1}+V_o\frac{n_1}{n_3}-V_{C2}]\widetilde{F}$$

Employing equations (3.15)-(3.18) with the voltage-second balance theorem to winding N_2 in mode M_3 in steady stat gives the following equations.

$$V_{C2}\cdot D=\frac{n_2}{n_3}V_o\cdot\widetilde{F}+V_{N1}\cdot\frac{n_2}{n_1}(1-D-\widetilde{F}),$$

where $V_{N1}=V_{C1}-V_{L1}-V_{C2}$ during $t_{3,M3}<t\ \leqq\ t_{4,M3}$, and $V_{L1}=V_{L1,3\text{-}4}/(1-D-\widetilde{F})$.

$$V_{C2}\cdot D=\frac{n_2}{n_3}V_o\cdot\widetilde{F}-\frac{n_2}{n_1}(V_{C1}-V_{C2})\cdot(1-D-\widetilde{F})+\frac{n_2}{n_1}(\frac{n_1}{n_2}V_{C2}-V_{C1})\widetilde{D}-\frac{n_2}{n_1}(V_{C1}+\frac{n_1}{n_3}V_o-V_{C2})\widetilde{F}\ .$$

Simplifying the above equation, the duty ratio D can be obtained by,

$$D=\frac{\widetilde{D}(\frac{n_2}{n_1}V_{C1}-V_{C2})+\frac{n_2}{n_1}(V_{C1}-V_{C2})}{\frac{n_2}{n_1}V_{C1}-V_{C2}(1+\frac{n_2}{n_1})}, \tag{3.19}$$

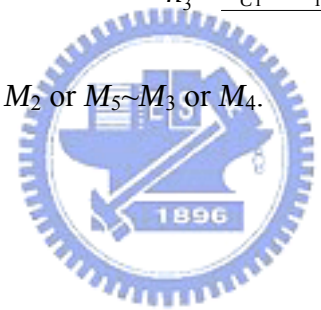
where $$\widetilde{D}=\frac{t_{1,M3}-t_{0,M3}}{Ts}$$

$$\widetilde{F}=\frac{t_{3,M3}-t_{2,M3}}{Ts}$$

$$t_{1,M3}-t_{0,M3}=i_{N1}(t_{0,M3})\cdot\frac{L_1}{V_{N1}-V_{C1}}$$

$$t_{3,M3}-t_{2,M2}=i_{N2}(t_{2,M3})\cdot\frac{n_2}{n_3}\cdot\frac{1}{\frac{V_{C1}+n_1V_o/n_3-V_{C2}}{L_1}+\frac{V_o}{L_{N3}}},$$

and $V_{C1}=|V_{ac}|=|V_m\sin(\omega t)|$ in M_2 or M_5~M_3 or M_4.



3.2 Analysis of Converter Operation

3.2.1 Primary current i_{N1} and Duty ratio D

In the converter circuit the filter capacitance C_1 is designed as a low pass filter to bypass the switching signal to ground and to pass the line power signal to the converter. Consequently, the primary component of $|i_{ac}|$ approximates to the primary component of i_{N1}. From equations (3.7) and (3.12), i_{N1} and V_{C1} display a linear relation when the angle of the line power signal exceeds the conduction angle. Therefore, i_{ac} can be controlled to linearly vary with V_{ac} during the conduction periods.

The secondary winding N_3 of the transformer operates in CCM during modes M_1 and M_2 and in DCM during mode M_3. The calculation of duty ratio can be simply obtained from equation (3.2), when winding N_3 operates in modes M_1 and M_2. However, the duty ratio becomes more complicate as given in equation (3.19) for mode M_3, since the current i_{N3} enters DCM. The value of duty ratio in mode M_3 is smaller than in modes M_1 and M_2. Furthermore, the duty ratio will be smallest when the peak V_{ac} presents, since $\widetilde{D}$ increases and $\widetilde{F}$ decreases when $|V_{ac}|$ increases from zero to the peak value.

3.2.2 Starting conduction angle

The value $\omega(t_1 - t_0)$ is called a starting conduction angle (SCA), as shown in Fig. 3.7. A smaller SCA leads to higher power factor and lower THD. Equation (3.3) shows that the SCA increases with increasing product of V_o/V_m and n_2/n_3. This phenomenon implies that power factor or THD decreases with increasing V_o/V_m or n_2/n_3. Figure 3.8 shows the relationship between V_o/V_m and SCA under various duty ratios D and two different winding ratios of n_1/n_2.

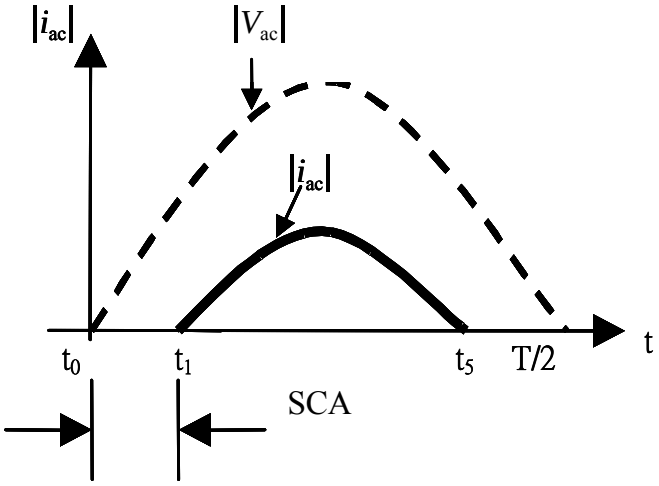


Fig. 3.7 Starting conduction angle

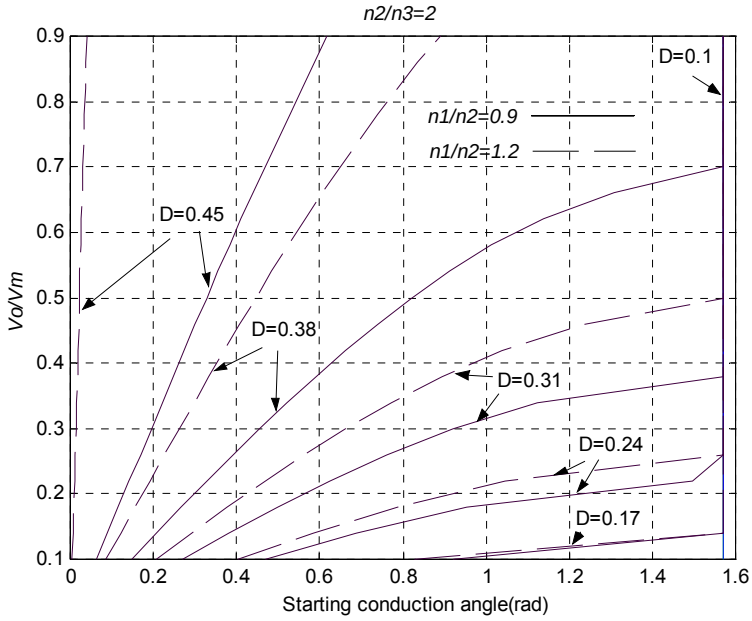


Fig. 3.8 Curve of starting conduction angle, V_o/V_m, D and N_1/N_2 at N_2/N_3=2.

3.2.3 Voltage across bulk capacitor

Equation (3.1) shows that the voltage across bulk capacitor, V_{C2}, varies with V_m, SCA, V_o, and n_1/n_3 but does not vary with the output load. In most applications, all the design calculations are always based on the given values of V_m and V_o. Thus, the voltage V_{C2} can be determined by selecting the preferred n_1/n_3, SCA, or n_2/n_3. In practical applications, the

voltage V_{C2} is kept under 450v for commercial considerations. Figure 3.9 provides designers with a convenient graphical design aid for obtaining the eclectic selections of n_1/n_3, SCA, and V_{C2} for certain line voltage ranges.

According to Fig. 3.2, the current i_{N1} is zero in the mode M_1 because the sum of V_{C1} and V_{N1} is smaller than V_{C2} when S_1 is in the off state. The diode D_1 continues off until the sum of V_{C1} and V_{N1} exceeds V_{C2}. Therefore, SCA decreases with decreasing V_{C2}. Two methods can be used to reduce V_{C2}. One method uses a smaller number of winding turns for n_1, and the other uses a larger inductance in L_1. The larger inductance L_1 can resist i_{N1} to charge V_{C2}, thus achieving lower V_{C2}.

According to equation (3.2), n_2/n_3 is the dominant parameter to influence the value of V_{C2}. L_1 and n_1 are the dominant parameters to influence the harmonic current and line current waveform. The turn number n_1 can be larger than n_2 or smaller than n_2. If n_1 is smaller than n_2, it will not gain any benefit and the harmonics current will become a poor value. Figure 3.11 and 3.12 show the simulation results in different turn ration n_1/n_2, and the lower value of n_1/n_2 will get higher harmonics current. Figure 3.13 also display the harmonics current in different turn rations.

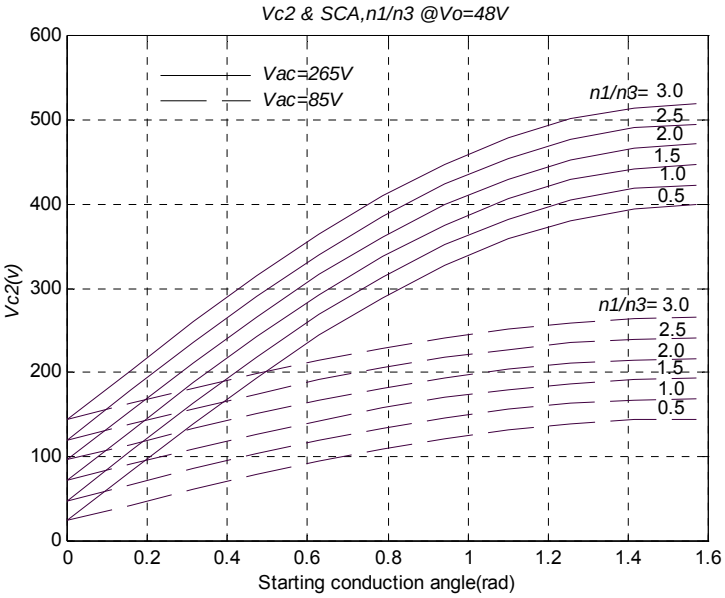


Fig. 3.9 Curve of starting conduction angle,V_{C2}, and n_1/n_3 at V_o=48v.

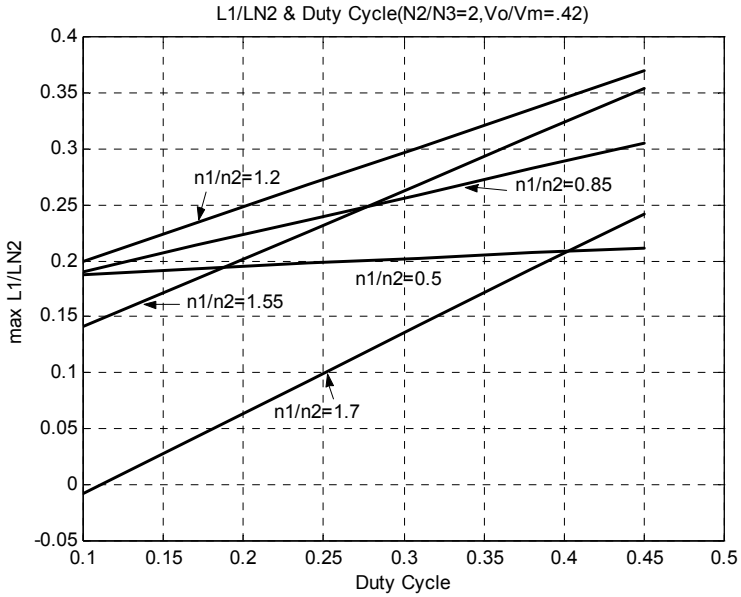


Fig. 3.10 Max L_1/L_{N2} and Duty cycle

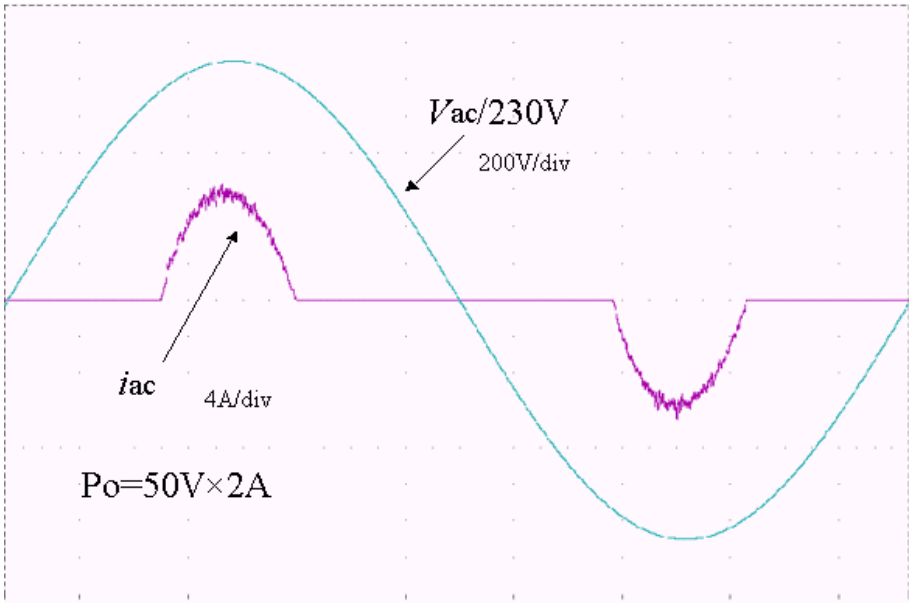


Fig. 3.11 Waveforms of i_{ac}&V_{ac} at n_1:n_2:n_3=1.2:1:0.5, L_1=33uH

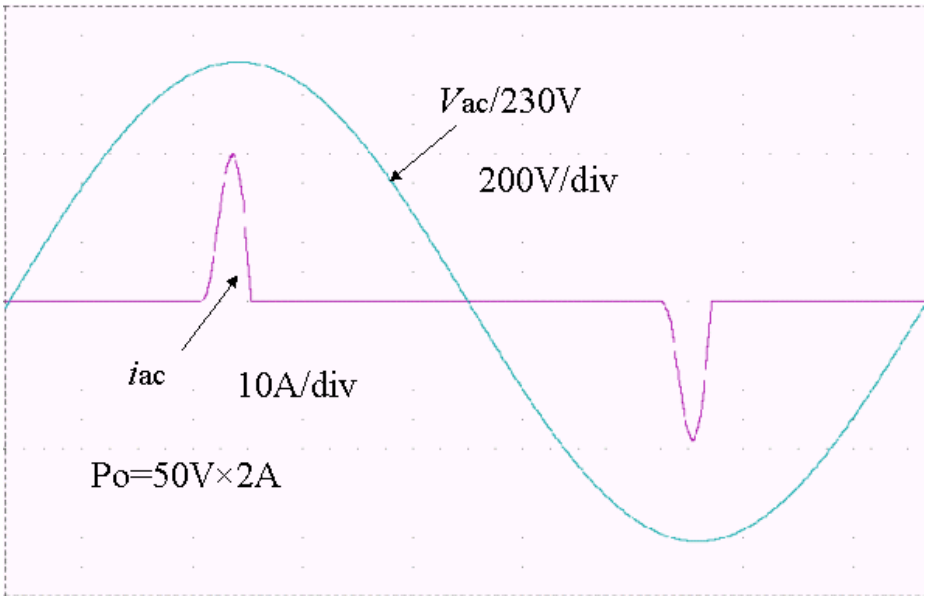


Fig. 3. 12 Waveforms of i_{ac}&V_{ac} at n_1:n_2:n_3=0.8:1:0.5, L_1=33uH

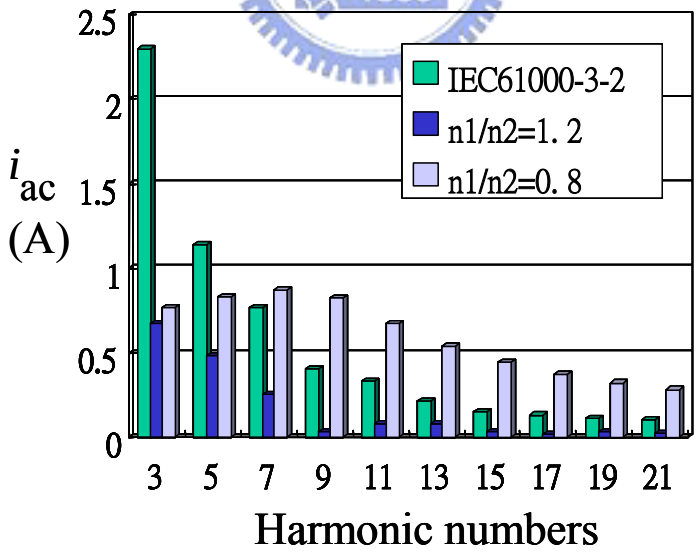


Fig. 3.13 Harmonic current at n_1/n_2=1.2 or n_1/n_2=0.8

3.2.4 Inductor L_1

The inductor L_1 is designed to provide the partially soft-switching function for diodes D_1 and D_2. When the current i_{N1} decreases, inductor L_1 causes the current i_{N1} to linearly decrease to zero, and the diode D_2 turns off without any switching-loss. Furthermore, the inductor L_1 causes i_{N1} to increase linearly from zero, and the diode D_1 turns on without switching-loss. To guarantee the partial soft switching, functions above, current i_{N1} must reduce to zero before switch S_1 turns off.

Employing the voltage-second balance theorem in L_1 for one switching cycle, equations (3.15)-(3.18) in mode M_3 yields

$$(V_{N1}-V_{C1})(t_{1,M3}-t_{0,M3})+V_{L1,3-4}=(V_{C2}+V_{N1}-V_{C1})(t_{3,M3}-t_{2,M3}), \tag{3.20}$$

where $t_{1,M3}$ - $t_{0,M3}=DT_s$, T_s is the switching period, and $V_{C1}=V_m$.

Substitution of equation (3.20) gives the maximum L_1 to guarantee the partial soft switching. Thus, L_1 can be obtained from

$$L_1 \le L_{N2}\cdot\frac{n_3}{n_2}\cdot\frac{V_m+\frac{n_1}{n_3}\cdot V_o-V_{C2}}{2V_o}\left[\frac{V_m}{V_{C2}}\cdot\left(D\cdot\frac{n_2}{n_1}+D\cdot\frac{n_3}{n_1}-\frac{n_3}{n_1}\right)+D\cdot\frac{n_3}{n_2}+\frac{n_3}{n_2}+1-\frac{n_2}{n_1}\right]-\frac{n_1}{n_2}\cdot\frac{\frac{n_1}{n_3}\cdot V_o-V_m}{V_{C2}} \tag{3.21}$$

Fig. 3.10 provides the designer a selection aid of L_1 to guarantee the partially soft-switching function working to D_1 and D_2.

3.3 Design Procedures

The method for designing the circuit of control loop and determining the voltage stresses of components voltage for the proposed converter is similar to that for designing the conventional flyback converter. However, the transformer design needs more calculations and considerations. The design method for transformer is shown as following.

1) Windings turns ratio $n_1/n_2/n_3$: The turn ratio n_2/n_3 can be obtained from equations

(3.1)-(3.3) by the substitutions of the given $V_{m,min}$, $V_{m,max}$, V_o, D_{max}, and $\omega t_{1,min}$, where $V_{m,min}$ and $V_{m,max}$ is the amplitude of minimum line voltage and maximum line voltage respectively, V_o is typical output voltage, D_{max} is the maximum duty ratio, and $0.4 \leqq D_{max} \leqq 0.45$. The corner angle $\omega t_{1,min}$, $0 < \omega t_{1,min} \leq \frac{\pi}{4}$, can be obtained as long as $V_{m,min}$ is chosen. The detailed steps for obtaining the turn ratio n_2/n_3 is depicted as follows:

(i) Let V_{C2} be limited under 420V at V_{in}=265V.

(ii) Assume that V_{C2} is proportional to V_{in}. Then $V_{C2} \fallingdotseq 85\times(420/265)=134.7$V at V_{in}=85V.

(iii) Let V_o=48V, D_{max}=0.4. Then substitution to equation (3.2) gives

$$48=134.7\times(n_3/n_2)\times[0.4/(1-0.4)],\ n_3/n_2 \fallingdotseq 0.5,$$

(iv) Substituting n_3/n_2=0.5 to equation (3.1) yields $0.9 \leqq n_1/n_3$.

(v) Let $\omega t_{1,min}$=0.24, $V_{m,min} \fallingdotseq 120$V, V_o=48V, D_{max}=0.4, and n_2/n_3=2/1. Then the substitutions of all the data to equation (3.3) gives $n_1/n_2 \fallingdotseq 1.2$.

2) Inductance L_{N2}, L_{N3}: The output ripple voltage varies with the inductance value of L_m. Therefore, it is suggested to count the output ripple voltage to calculate L_m. The ripple current of output port is shown as following,

$$\Delta i = V \cdot \Delta t / L\ .$$

Consider the steady state situation. The average output current is

$$\begin{aligned} I_o &= \tfrac{1}{2}[i_{N3}(t_{1,M1}) + i_{N3}(t_{2,M1})](1-D) \\ &= \tfrac{1}{2} i_{N3}(t_{1,M1})(1+k)(1-D) \end{aligned}$$

and the output ripple current is

$$\begin{aligned} \Delta i &= i_{N3}(t_{1,M1}) - i_{N3}(t_{2,M1}) \\ &= i_{N3}(t_{1,M1})(1-k) \\ &= \frac{2I_0(1-k)}{(1+k)(1-D)} \end{aligned} \quad ,$$

where $k = i_{N3}(t_{2,M1}) / i_{N3}(t_{1,M1})$.

Now, let $V = V_o$, $\Delta t = T_s \times (1-D)$ and $L = L_{N3}$. Solving the equations above gives

$$L_{N3} = V_O \times T_s(1-D)^2 \times \frac{(1+k)}{2I_O(1-k)}.$$

and

$$L_{N2} = L_{N3} \times (\frac{n_2}{n_3})^2$$

3) Series inductance L_1: The inductance L_1 can be yielded by putting above parameters in equation (3.21).

4) To confirm $dB<B_{max}$: The maximum change value of magnetic flux density has to limit under maximum magnetic flux density for the selected magnetic material.

Given $L_{N2} \cdot di_{N2} = N_2 \cdot dB \cdot Ae$ or $dB = \frac{L_{N2} \cdot di_{N2}}{N_2 \cdot Ae}$, where di_{N2} can be calculated by substituting DTs for $(t\text{-}t_{0,M3})$ in equation (3.13), Ae is the effective area of the selected magnetic core.

$$di_{N2} \equiv i_{N2,\max} = DTs[\frac{(V_{N1}-V_m)n_1}{L_1 n_2} + \frac{V_{C2}}{L_{N2}}]; \quad \frac{L_{N2} \cdot di_{N2}}{N_2 \cdot Ae} < B_{\max}.$$

3.4 Experimental Results

An experimental prototype has been established to demonstrate the circuit operation and the analysis results presented above. The experimental circuit can operate in 85V~265V/ac input voltage range and generate an output voltage of 48v/dc and an output power of 96W. The turn ratio of $n_1/n_2/n_3$ is 2.38/2/1 and the inductance ratio of L_1/L_{N1} is 0.17, where L_1=30 μ H and transformer core PQ32/20 is used. The transformer core employed in previous similar converter should be EER35 in [6]-[7]. Although some previous similar converters have similar transformer core size to the proposed converter for similar output power and switching frequency, the values of the boost inductors, 58 μ H~240 μ H in [6] or 1.4mH in [7], are several times greater than the value of L_1 in the proposed converter. The sizes of the boost inductors employed in [6]-[7] thus are several times greater than that of L_1 when flowing through a similar line current. The converters in [8] or [9] use similar smaller boost inductor 30 μ H, but the line current harmonic distribution is higher than that produced by the proposed converter. Table 3.1 shows that the detailed harmonic distributions of the experimental circuit using 230V line voltages are significantly below the levels required by class D.

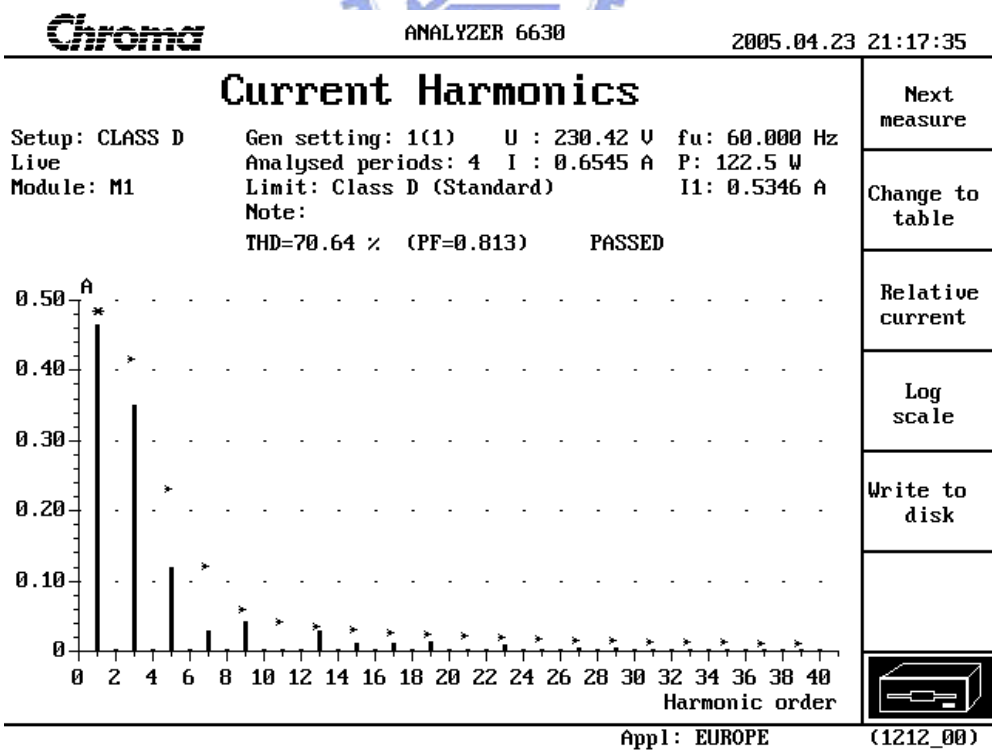


Table 3.1 The major harmonic components of the line current, P_o=48V/2A, in proposed flyback converter

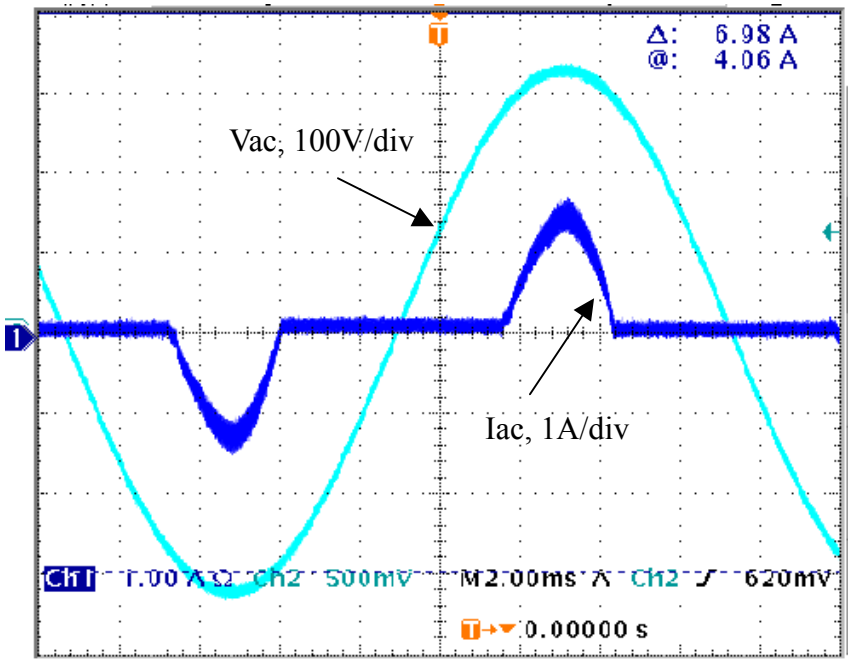


Fig. 3.14 Line current and line voltage waveforms, V_{ac}=230V, Output=48v/2A.

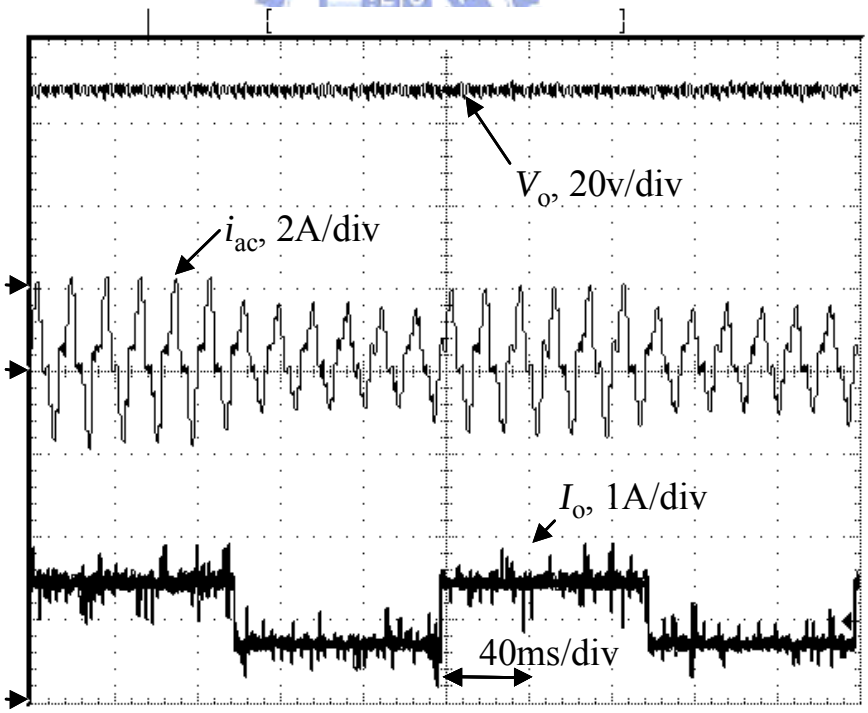


Fig. 3.15 Dynamic response waveforms for output voltage V_o, line current i_{ac} , output current I_o. Ch1->V_o, Ch2-> i_{ac}, Ch3-> I_o=0.75A/1.5A.

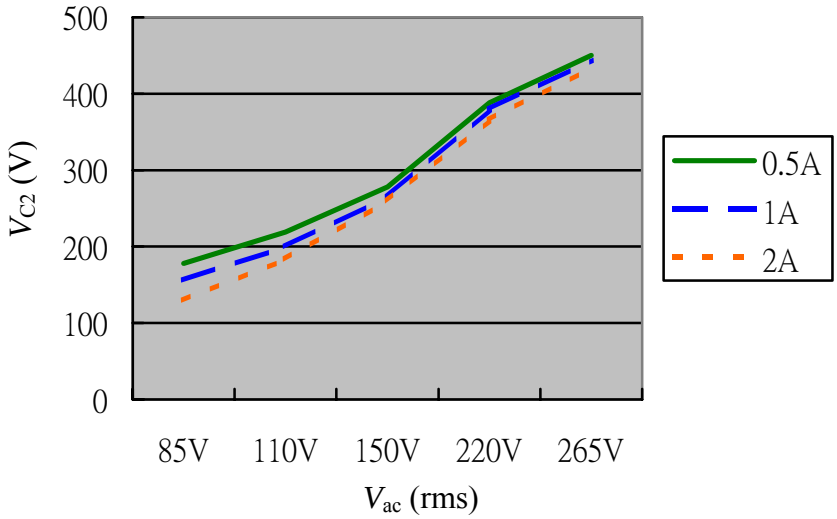


Fig. 3.16 Voltage rating of bulk capacitor and line voltage

Figure 3.14 shows the line current in a line-cycle, revealing that its harmonic distribution complies with a standard of IEC 61000-3-2. Figure 3.15 shows the dynamic response from a 3/8 to 3/4 full load in 110v/ac input voltage. The output voltage of prototype shows a fast response and stable regulation. Figure 3.16 shows the voltages across bulk capacitor for different loads from 85V to 265V line voltage. The experimental results demonstrate that the bulk capacitor voltage was ranged between 60~70% higher than the line voltage. Furthermore, a lower percentage can be achieved by carefully selecting the winding ratio. The voltage of the bulk capacitor is shown to depend on both V_{ac} and turn ratio n_2/n_3, but irrelative to load current.

Figures 3.17 and 3.18 show the test system and prototype of proposed converter respectively. The test system contains Power Analyzer/Chroma 6630, AC power source, Electronic Load and oscilloscope.

Fig. 3.17 Test system picture

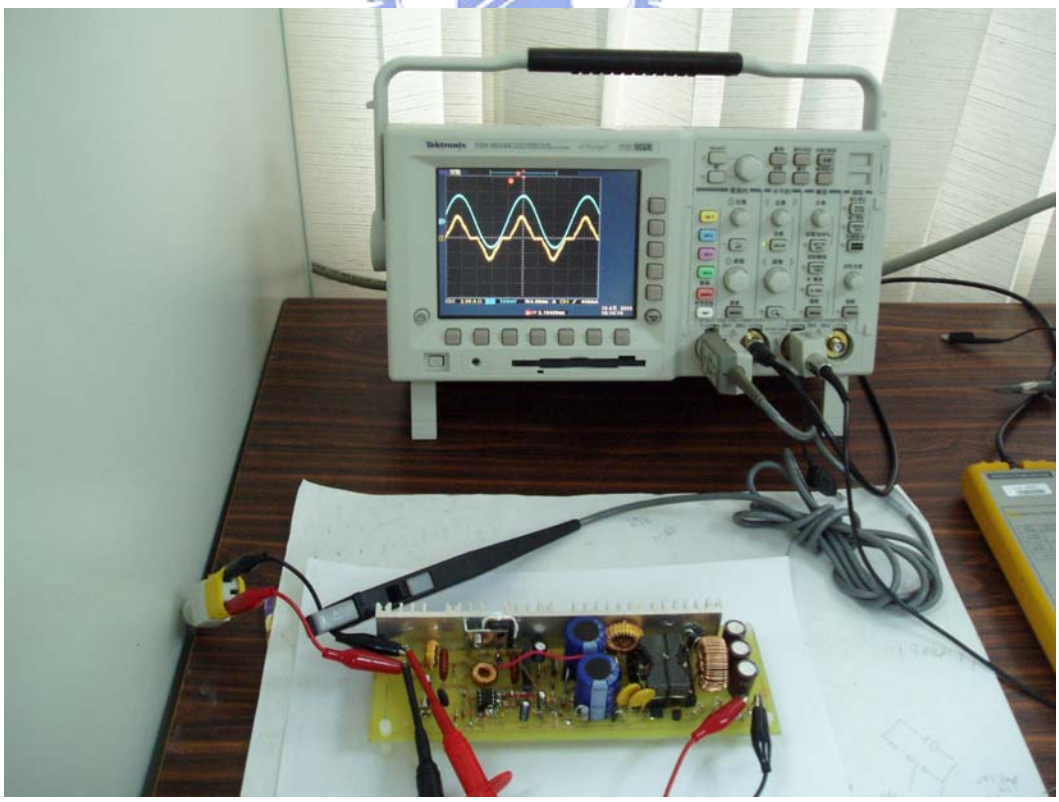


Fig. 3.18 The prototype of the proposed converter and test results at Vac=110V and 48V/2A output.

3.5 Extension Circuit

The voltage stress across main switch in primary side will be over 500V when the proposed flyback converter is applied in wide range input voltage up to 265V. The high voltage stress will cause two drawbacks, expensive cost in MOSFET and high switching loss in the same MOSFET. Therefore, this section will introduce an extension circuit to prevent the switch from the high voltage stress.

The voltage stress on main switch can be expressed as

$$V_{ds} = V_{C2} + V_o \cdot \frac{n_2}{n_3} \tag{3.22}$$

Based on the prototype's data, the maximum voltage stress V_{ds} is 536V where V_{C2}=440V, V_o=48V, and n_2/n_3=2.

Figure 3.19 is the extension circuit, twin-transistors type flyback converter, based on the proposed flyback circuit. The circuit adds a switch S_2 and the switching operation is synchronous to S_1. Except the additional switch, there is no difference in comparing to the proposed flyback converter. The additional transistor can share a half voltage-stress in the single transistor flyback converter. Therefore, the high voltage stress issue can be solved via the proposed twin-transistors flyback converter.

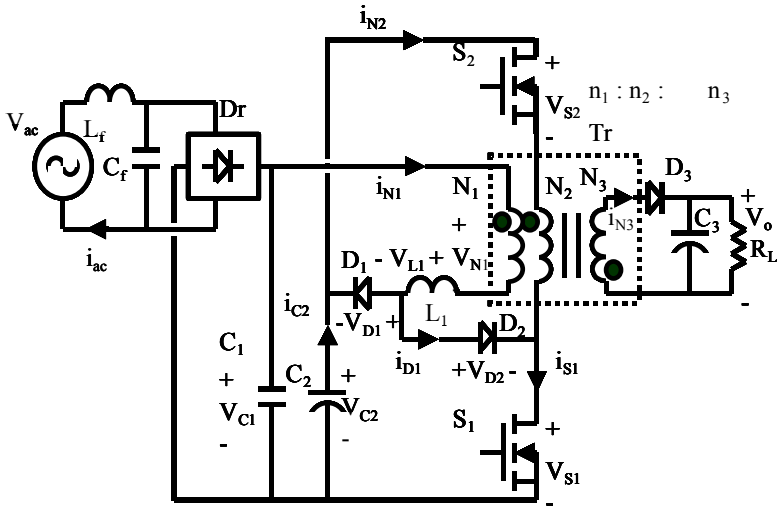


Fig. 3.19 The proposed twin-transistors flyback converter

CHAPTER 4

THE FORWARD CONVERTER USING THE PROPOSED INPUT CURRENT SHAPER

Figure 4.1 illustrates the proposed forward AC/DC converter with input current shaper and fast output regulation. The proposed circuit is a single-switch single-stage AC/DC converter, which comprises a single switch S_1, an input filter C_1, bulk capacitor C_2, soft-switching inductor L_1, and a transformer with two primary windings N_1&N_2. The winding N_1, inductor L_1 and diode D_1&D_2 form an input current shaper. The winding N_1, inductor L_1, diode D_1&D_2, switch S_1, and bulk capacitor C_2 form a boost circuit. Moreover, the windings N_2&N_3, a bulk capacitor C_2, switch S_1, diode D_3, D_4, inductor L_2, and output capacitor C_3 form a forward converter. The circuit connection of the reset winding N_1 differs from that in the classical forward converter. In the proposed design, the reset winding N_1 has two functions, to recycle the magnetic current generated by the winding N_2, and also to form a magnetic feedback for shaping line current. Besides,

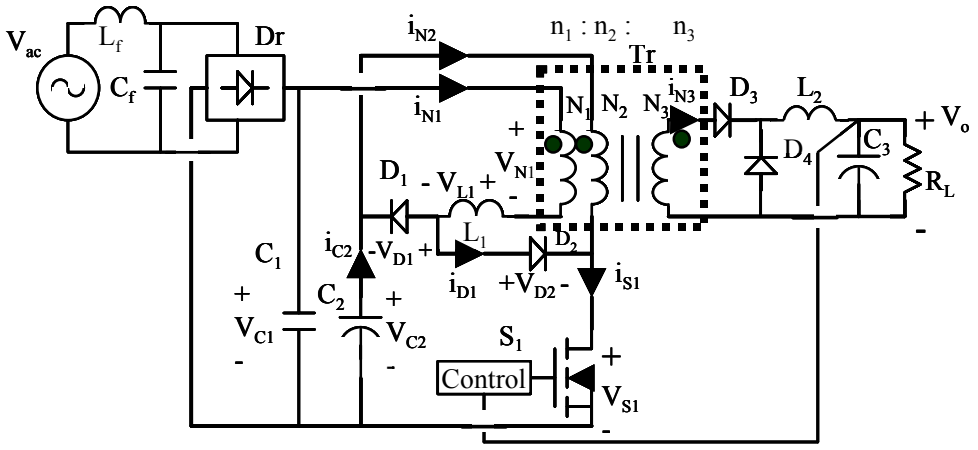


Fig. 4.1 Proposed forward AC/DC converter with ICS

A turn ratio of n_1/n_2 can determine not only the corner angle of the line current, but also the voltage across a bulk capacitor C_2. More detailed effects of turn ratio of n_1/n_2 are discussed in the following section. The inductor L_1 provides a soft-switching function for diodes D_1 and D_2. When the current i_{N1} of L_1 linearly reduces to zero illustrated in Fig. 6, D_1 (in mode M_1) or D_2 (in mode M_2) turn off switching loss. Additionally, the inductance and volume of L_1 are significant, and are smaller than the primary windings N_1 or N_2 of the transformer.

The control circuit can be designed using either a simple fixed-frequency voltage mode control or a conventional peak-current mode control. The experimental results have demonstrated that even if a simple control method is used, the line current of the proposed AC/DC converter can comply with the standard IEC 61000-3-2 and the converter also can exhibit a fast dynamic response to the load.

4.1 Basic Operation Theories

The operating principle of the proposed converter resembles the boost-based AC/DC single-switch single-stage isolated power-factor-correction power supply (S^4IP^2). The energy, stored in winding N_2 while switch S_1 turns on, is delivered to bulk capacitor C_2 via N_1 when switch S_1 turns off. The energy stored in winding N_2 comes from the magnetizing current when switch S_1 turns on. Furthermore, winding N_2 and N_3 are based on the same operating principle as the conventional forward converter. The current i_{N1} gives more magnetizing current to charge C_2 and causes V_{C2} to increase during (t_1, t_3), as illustrated in Fig. 4.2. Furthermore, a lower magnetizing current of i_{N1} causes V_{C2} to decrease during both periods (t_3, $T_l/2$) and (t_0, t_1) in Fig. 4.2. In this converter the capacitance of C_2 is designed to have the same value used in conventional AC/DC forward converter to maintain V_{C2} almost constant in a line cycle. Since the capacitance of C_2 is large, V_{C2} remains almost constant during the whole line period. Furthermore, the inductance of the regulation inductor L_2 in secondary side is set sufficiently large to keep L_2 working in the continuous conduction mode, and also to keep the duty cycle D almost constant during these two operation modes.

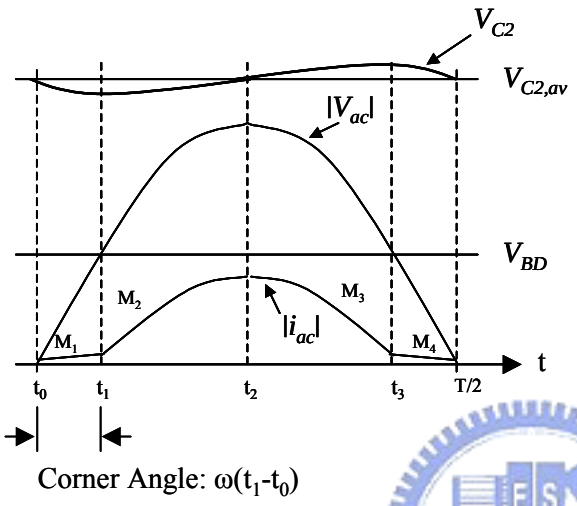


Fig. 4.2 Operation modes in half of line cycle

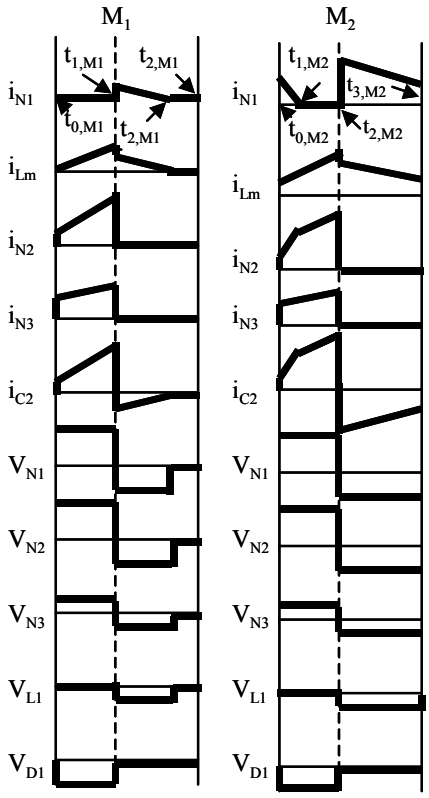


Fig. 4.3 Voltage and current waveforms in two modes

Figure 4.2 shows that the proposed circuit has two operation modes, M_1-M_4 and M_2-M_3, where M_4 and M_3 are mirror-symmetric to M_1 and M_2. Figure 4.3 illustrates the relative voltage and current waveforms in a single switching cycle in two operation modes.

4.1.1 Operation Modes M_1 or M_4 (during t_0~t_1 or t_3~$T_l/2$):

Within this mode, the converter operates as the conventional forward converter does. However, the magnetizing current i_{Lm} generated by winding N_2 is transferred to winding N_1 and the capacitor C_2 is charged when S_1 is switched off. The current i_{N1} linearly reduces to zero when S_1 is turned off. V_{C2} denotes the voltage across the bulk capacitor C_2. If C_2 is

sufficiently large, then V_{C2} can approximate a constant during a line cycle in the steady state, and can be calculated as follows:

$$V_{C2} \cdot \frac{n_3}{n_2} \cdot D = V_o . \tag{4.1}$$

When the boundary time t_1 is met as shown in Fig. 4.2, the magnetic flux will just decreased to zero at the end of duty off time. It implies that after the boundary time of M_1&M_2, i_{N1} will not decreases to zero at the end of duty off time. Therefore, the average of i_{N1} becomes large and causes V_{C2} starting to increase. In other words, $t_{2,M1}$ = $t_{3,M1}$ at t = t_1. Using the boundary conditions t_1 can be obtained by the following calculations.

While time is in the duration of $t_{1,M1} - t_{t2,M1}$, the current i_{N1} is given by

$$i_{N1}(t) = \frac{V_{C2} \cdot T_s D \cdot n_2 \cdot L_{N1}}{L_m \cdot n_1 \cdot (L_{N1} + L_1)} - \frac{V_{C2} - V_{in}}{L_{N1} + L_1} \cdot (t - t_{1,M1})$$

Since at time t_1, $i_{N1}(t_{2,M1}) = i_{N1}(t_{3,M1}) = 0$ and $t_{3,M1}$-$t_{1,M1}$=T_s(1-D), substitution to the equation above gives

$$\frac{V_{C2} \cdot T_s D \cdot n_2 \cdot L_{N1}}{L_m \cdot n_1 \cdot (L_{N1} + L_1)} - \frac{V_{C2} - V_{in}}{L_{N1} + L_1} \cdot (1 - D) T_s = 0 ,$$

where $V_{in} = V_m \sin \omega t_1$. Solving the equation above gives

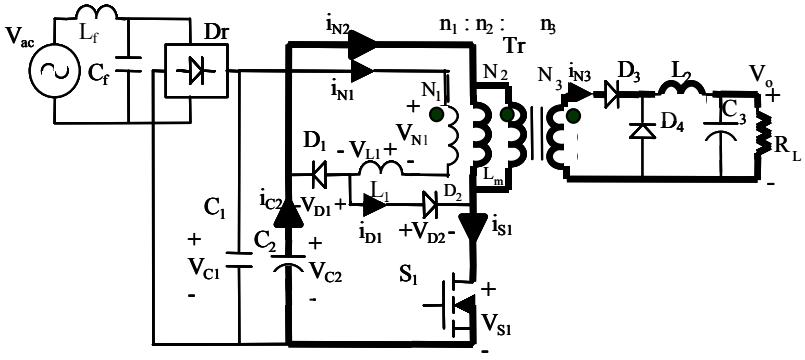
$$t_1 = \frac{1}{\omega} \times \sin^{-1}\left[\frac{V_{C2}}{V_m} - \frac{V_{C2} \cdot D \cdot n_2 \cdot L_{N1}}{V_m \cdot (1 - D) \cdot n_1 \cdot L_m} \right] \tag{4.2}$$

or

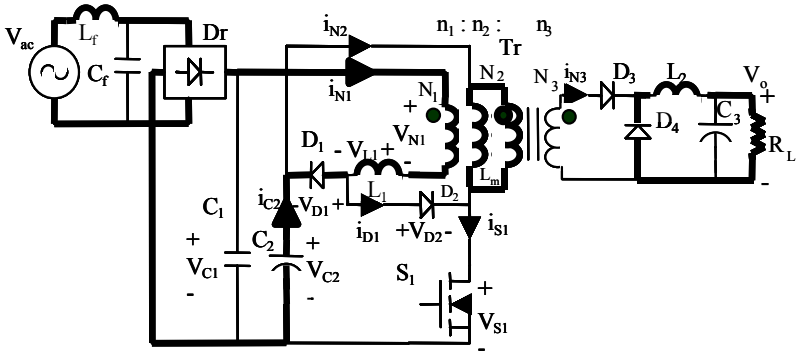
$$\omega t_1 = \sin^{-1}\left[\frac{V_o}{V_m} \cdot \frac{n_2}{n_3} \left(\frac{1}{D} - \frac{n_1}{(1 - D) n_2} \right) \right], \tag{4.3}$$

where $V_m \left| \sin(\omega t) \right|$ is a rectified power source, $|V_{ac}|$.

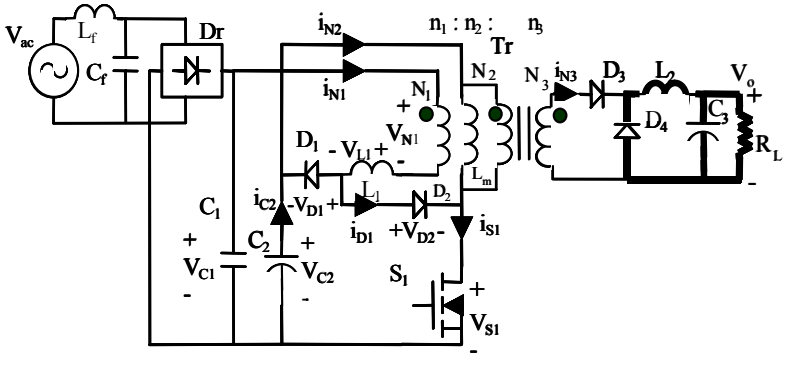
Figure 4.4 illustrates the current loop in three intervals in mode M_1 or M_4.



(a) $t_{0,M1} \leq t < t_{1,M1}$



(b) $t_{1,M1} \leq t < t_{2,M1}$



(c) $t_{2,M1} \leq t < t_{3,M1}$

Fig. 4.4 Current loops during S_1 (a) turns on ($t_{0,M1} \leq t < t_{1,M1}$), (b) turns off($t_{1,M1} \leq t < t_{2,M1}$), (c) turns off($t_{2,M1} \leq t < t_{3,M1}$) in mode M_1/M_4

The winding currents and voltages are calculated as follows:

$$i_{N1}=\begin{cases}0, & t_{0,M1}\le t<t_{1,M1}\\ \dfrac{V_{C2}\cdot T_s D\cdot n_2\cdot L_{N1}}{L_m\cdot n_1\cdot(L_{N1}+L_1)}-\dfrac{V_{C2}-V_{in}}{L_{N1}+L_1}\cdot t, & t_{1,M1}\le t<t_{2,M1}\end{cases}, \tag{4.4}$$

$$i_{N2}=\begin{cases}i_{Lm}+i_{N3}\cdot\dfrac{n_3}{n_2}, & t_{0,M1}\le t<t_{1,M1}\\ 0, & t_{1,M1}\le t<t_{3,M1}\end{cases}, \tag{4.5}$$

where $i_{Lm}=\dfrac{V_{C2}}{L_m}\cdot t$,

$$i_{N3}=\begin{cases}(I_O-\dfrac{\Delta I_O}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_O}{L_2}\cdot t, & t_{0,M1}\le t<t_{1,M1}\\ 0, & t_{1,M1}\le t<t_{3,M1}\end{cases}, \tag{4.6}$$

where $I_O=\overline{V}_O/R_L$ and ΔI_O is a load ripple current and $\Delta I_O=\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_O}{L_2}\cdot DT_S$.

$$V_{N1}=\begin{cases}V_{C2}\cdot\dfrac{n_1}{n_2}, & t_{0,M1}\le t<t_{1,M1}\\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}, & t_{1,M1}\le t<t_{2,M1}\\ 0, & t_{2,M1}\le t<t_{3,M1}\end{cases}, \tag{4.7}$$

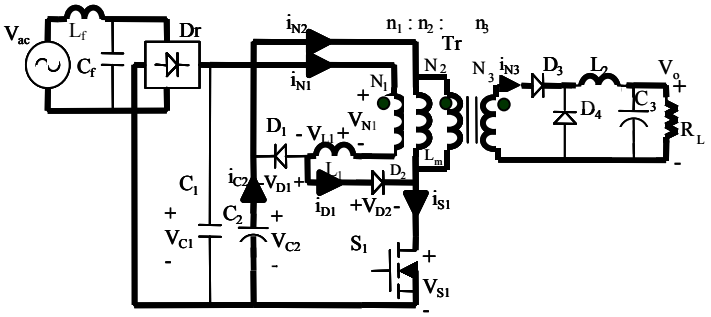
$$V_{N2}=\begin{cases}V_{C2}, & t_{0,M1}\le t<t_{1,M1}\\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}\cdot\dfrac{n_2}{n_1}, & t_{1,M1}\le t<t_{2,M1}\\ 0, & t_{2,M1}\le t<t_{3,M1}\end{cases}, \tag{4.8}$$

$$V_{N3}=\begin{cases}V_{C2}\cdot\dfrac{n_3}{n_2}, & t_{0,M1}\le t<t_{1,M1}\\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}\cdot\dfrac{n_3}{n_1}, & t_{1,M1}\le t<t_{2,M1}\\ 0, & t_{2,M1}\le t<t_{3,M1}\end{cases}, \tag{4.9}$$

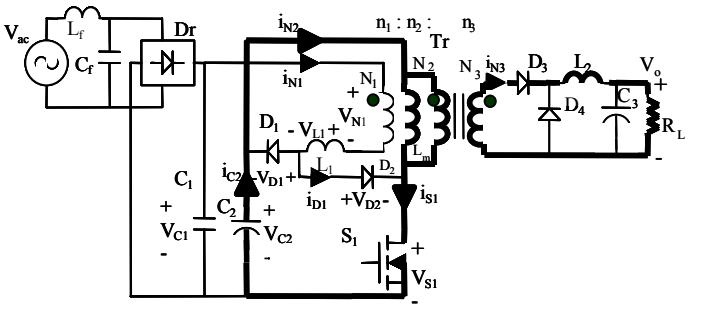
$$V_{L1}=\begin{cases}0, & t_{0,M1}\le t<t_{1,M1}\\ -(V_{C2}-V_{in})\cdot\dfrac{L_1}{L_{N1}+L_1}, & t_{1,M1}\le t<t_{2,M1}\\ 0, & t_{2,M1}\le t<t_{3,M1}\end{cases} \tag{4.10}$$

4.1.2 Operation Modes M_2 or M_3 (during t_1~t_2 or t_2~t_3):

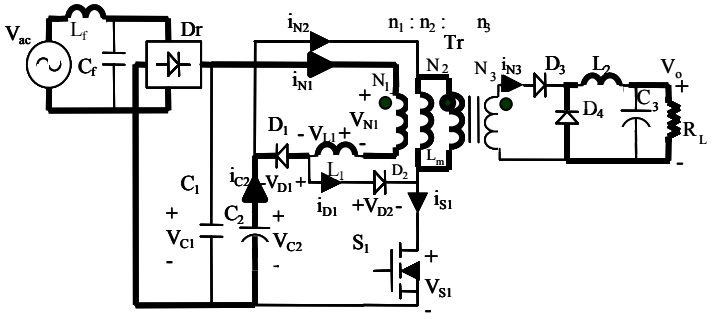
In this mode, i_{N1} doesn't decrease to zero while S_1 turning off in last switching cycle so i_{N1} will continue to decrease when S_1 is turned on again. Current i_{N1} flows through the winding N_1, L_1, D_2, and S_1. Moreover, the induced voltage across winding N_1 forces i_{N1} to speed up decreasing to zero. The capacitor C_2 supplies current i_{N2} which flows through winding N_2 and S_1. Simultaneously, D_3 turns on and the transformer delivers the power to the output circuit. When S_1 turns off, the magnetizing current i_{Lm} induces i_{N1} and charges capacitor C_2 via winding N_1, L_1, and D_1. The induced current i_{N1} linearly decreases to $i_{N1}(t_{3,M2})$ at the end of the duty off period of switch S_1, where $i_{N1}(t_{3,M2})$ or $i_{N1}(t_{3,M3})$ is nonzero in this mode. Figure 4.5 shows the current loops for three operating stages in M_2/M_3.



(a) $t_{0,M2} \leqq t < t_{1,M2}$



(b) $t_{1,M2} \leqq t < t_{2,M2}$



(c) $t_{2,M2} \leqq t < t_{3,M2}$

Fig. 4.5 Current loops during S_1 (a) turns on ($t_{0,M2} \leq t < t_{1,M2}$), (b) turns on($t_{1,M2} \leq t < t_{2,M2}$), (c) turns off($t_{2,M2} \leq t < t_{3,M2}$) in mode M_2/M_3

The corresponding currents and voltages are obtained as follows:

$$i_{N1} = \begin{cases} i_{N1}(t_{0,M2}) - \dfrac{V_{C2} \cdot \dfrac{n_1}{n_2} - V_{in}}{L_1} \cdot (t - t_{0,M2}), & t_{0,M2} \leq t < t_{1,M2} \\ i_{N1}(t_{2,M2}) - \dfrac{V_{C2} - V_{in}}{L_{N1} + L_1} \cdot (t - t_{2,M2}), & t_{2,M2} \leq t < t_{3,M2} \end{cases} . \quad (4.11)$$

Since L_1 is employed, i_{N1} will be continuous at the time $t_{3,M2}$; that is $i_{N1}(t_{3,M2}) \fallingdotseq i_{N1}(t_{0,M2})$. Since proper L_2 is used, the current i_{N3} is almost constant. Consider the magnetic flux generated and applied between winding N_1 and N_2 we can yield

$$i_{N1}(t_{2,M2}) = i_{Lm}(t^{-}_{2,M2}) \cdot \frac{n_2 \cdot L_{N1}}{n_1 \cdot (L_{N1} + L_1)} . \quad (4.12)$$

$$i_{N2}=\begin{cases} i_{Lm}+\dfrac{n_1}{n_2}\cdot\dfrac{V_{C2}\cdot\dfrac{n_1}{n_2}-V_{in}}{L_1}(t-t_{0,M2})+i_{N3}\cdot\dfrac{n_3}{n_2}, & t_{0,M2}\le t<t_{1,M2} \\ i_{Lm}+\dfrac{n_1}{n_2}\cdot\dfrac{V_{C2}\cdot\dfrac{n_1}{n_2}-V_{in}}{L_1}\cdot(t_{1,M2}-t_{0,M2})+i_{N3}\cdot\dfrac{n_3}{n_2}, & t_{1,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.13}$$

where

$$i_{Lm}=\begin{cases} i_{N1}(t_{0,M2})\cdot\dfrac{n_1}{n_2}+\dfrac{V_{C2}}{L_m}(t-t_{0,M2}), & t_{0,M2}\le t<t_{2,M2} \\ i_{N1}\cdot\dfrac{n_1}{n_2}, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.14}$$

Substituting equations (4.12) and (4.14) into (4.11) yields $i_{N1}(t_{3,M2})$, or $i_{N1}(t_{0,M2})$. For the other winding currents, the following equations are obtained.

$$\begin{aligned} & i_{N1}(t_{2,M2})-\frac{V_{C2}-V_{in}}{L_{N1}+L_1}(1-D)T_s=i_{N1}(t_{3,M2})\approx i_{N1}(t_{0,M2}) \\ & \Rightarrow i_{Lm}(t^{-}{}_{2,M2})=i_{N1}(t_{0,M2})\cdot\frac{n_1}{n_2}+\frac{V_{C2}}{L_m}\cdot DT_s \\ & [i_{N1}(t_{0,M2})\cdot\frac{n_1}{n_2}+\frac{V_{C2}}{L_m}\cdot DT_s]\cdot\frac{n_2L_{N1}}{n_1(L_{N1}+L_1)}-\frac{V_{C2}-V_{in}}{L_{N1}+L_1}(1-D)T_s\approx i_{N1}(t_{0,M2}) \\ & i_{N1}(t_{0,M2})\approx\frac{T_s}{2L_{N1}+L_1}[(V_{C2}-V_{in})(1-D)-\frac{n_2V_{C2}L_{N1}}{n_1L_m}\cdot D] \end{aligned}, \tag{4.15}$$

$$i_{N3}=\begin{cases} (Io-\dfrac{\Delta Io}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_o}{L_2}\cdot t, & t_{0,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.16}$$

$$V_{N1}=\begin{cases} V_{C2}\cdot\dfrac{n_1}{n_2}, & t_{0,M2}\le t<t_{2,M2} \\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.17}$$

$$V_{N2}=\begin{cases} V_{C2}, & t_{0,M2}\le t<t_{2,M2} \\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}\cdot\dfrac{n_2}{n_1}, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.18}$$

$$V_{N3}=\begin{cases} V_{C2}\cdot\dfrac{n_3}{n_2}, & t_{0,M2}\le t<t_{2,M2} \\ -(V_{C2}-V_{in})\cdot\dfrac{L_{N1}}{L_{N1}+L_1}\cdot\dfrac{n_3}{n_1}, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.19}$$

$$V_{L1}=\begin{cases} -(V_{C2}\cdot\dfrac{n_1}{n_2}-V_{in}), & t_{0,M2}\le t<t_{1,M2} \\ 0, & t_{1,M2}\le t<t_{2,M2} \\ -(V_{C2}-V_{in})\cdot\dfrac{L_1}{L_{N1}+L_1}, & t_{2,M2}\le t<t_{3,M2} \end{cases}, \tag{4.20}$$

4.2. Analysis of Converter Operation

4.2.1 Line Current and Duty Ratio

The line current i_{ac} is a low frequency component of i_{N1} flowing through the low pass filter L_r-C_r. Mathematically the line current i_{ac} is the average current of i_{N1} within a switching cycle. Equation (4.4) demonstrates that the average current i_{N1}, namely, i_{ac}, varies slightly with V_{in} in both modes M_1 and M_4. Moreover, equation (4.11) demonstrates that the line current i_{ac} varies markedly with the line voltage V_{in} in both modes M_2 and M_3. Accordingly, the none-zero current $i_{N1}(t_{3,M2})$, that equals to $i_{N1}(t_{0,M2})$, also varies with V_{in}. Therefore, the resultant line current is produced, as illustrated in Fig. 4.2. Moreover, the current i_{N1} is discontinuous in mode M_1 and M_2 according to Fig. 4.3. Therefore, the proposed converter operates the current i_{N1} in DCM.

Since the capacitance C_2 is assigned large, V_{C2} is assumed constant. Thus, for fixed load the duty ratio D can be assumed approximate to a constant. Under the assumptions the relation of V_{C2} and duty ratio D can be found through employing equation (4.1). Additionally, i_{L2} is intentionally designed to operate in CCM since this kind of design is useful to stabilize the duty ratio D and improve the output regulation.

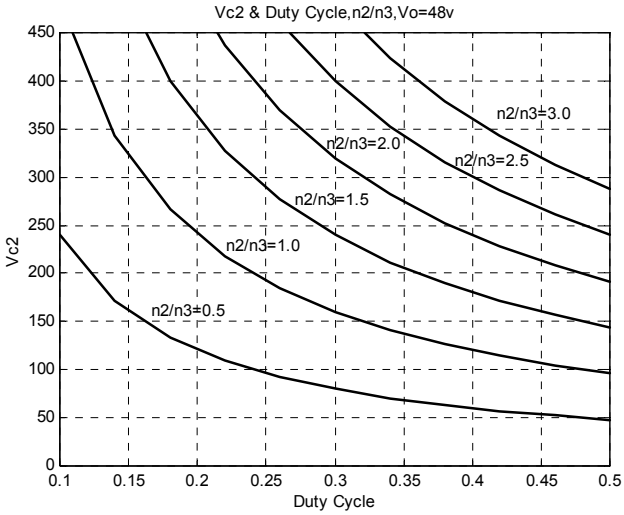


Fig. 4.6 V_{C2} & Duty cycle, n_2/n_3 at V_o=48v

4.2.2 Corner Angle of Line Current

Line current corner angle (CA) is defined as $\omega(t_1\text{-}t_o)$, it can refer to fig. 4.2. Equation (4.3) demonstrates the relation between CA and parameters, duty ratio D, n_1/n_2, n_2/n_3, and V_o/V_m. Moreover, equations (4.1)-(4.3) demonstrate the relation of CA and V_o/V_m in different n_1/n_3 and duty ratio D. CA is larger in the high line voltage than the low line voltage with same given constant output power P_o. Furthermore, greater CA degrades the power factor more and lower CA has higher power factor. Figure 4.7 shows the relationship in curve between corner angle and V_o/V_m, D, and n_1/n_3.

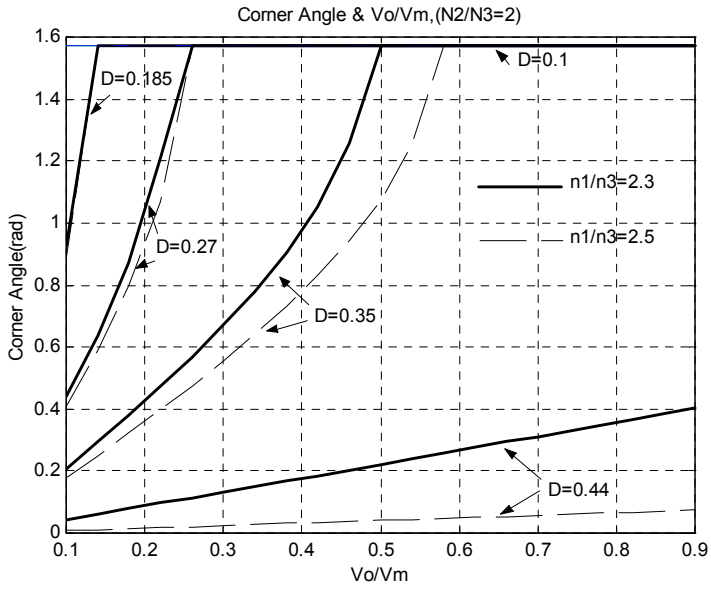


Fig. 4.7 Corner angle and V_o/V_m

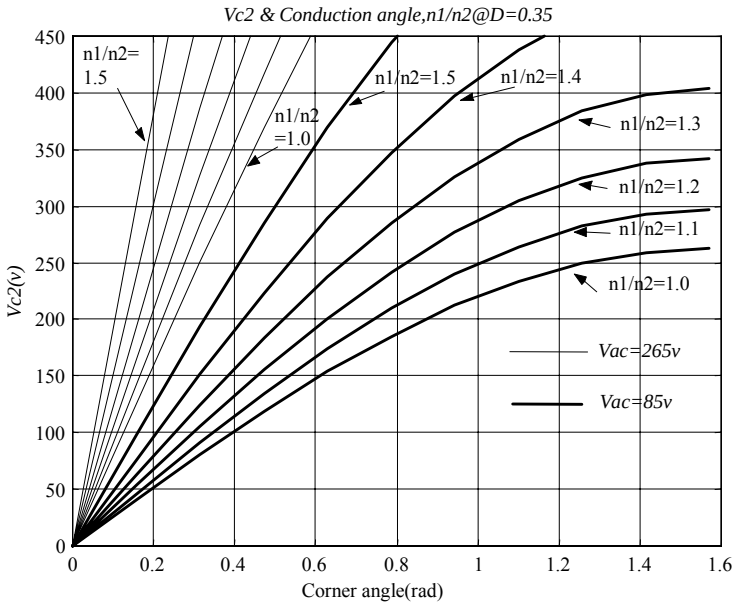


Fig. 4.8 V_{C2}, Corner angle and n_1/n_2

4.2.3 Voltage Across Bulk Capacitor

V_{C2} denotes the voltage across bulk capacitor C_2. The voltage V_{C2} are determined by n_1/n_2, duty ratio D, corner angle CA, input voltage V_{in} and output voltage V_o. Equation (4.21) is the formula to obtain CA. It shows that the greater line voltage or smaller V_{C2} produces smaller

CA. Smaller CA produces higher power factor and lower THD. Furthermore, in practical applications V_{C2} should be below 450V/dc with wide range input, 90V~265V/ac, and parameters, $n_1/n_2/n_3$ and D, also must meet the requirement (V_{C2} below 450V/dc) to produce a given output V_o.

$$\omega t_1 = Sin^{-1}[\frac{V_{C2}}{V_m}(1-\frac{V_o \cdot n_1}{V_{C2} \cdot n_3 - V_o \cdot n_2})] \tag{4.21}$$

Now using equations (4.1) and (4.2) the values of V_{C2}, t_1, n_1/n_2, and n_3/n_2 can be determined under some compromise considerations.

Furthermore, equations (4.4) and (4.11) show that the current i_{N1} is inversely proportion to (L_1+L_{N1}).

$$i_{D1} = \begin{cases} i_{N_1}, & t_{1,M1} < t < t_{2,M1} \\ i_{N_1}, & t_{2,M2} < t < t_{3,M2} \\ 0, & \text{else} \end{cases} . \tag{4.22}$$

Since i_{D1} is the charge current of C_2, V_{C2} will be affected by i_{N1} slightly. Therefore, V_{C2} will be slightly inversely affected by (L_1+L_{N1}).

4.2.4 Inductor L_1

Two reasons exist for using inductor L_1. The first reason is to reduce the high frequency harmonics of i_{N1}, while the second is to reduce the voltage across capacitor C_2. Figure 4.2 demonstrates that the slope of V_{C2} is zero at time t_1. The total charge charged by i_{N1} during the duty on period thus equals the total charge discharged by i_{N2}. Thus equating the integration of equations (4.4) and (4.5) gives

$$\int_{t_{1,M1}}^{t_{3,M1}} i_{N1}(\tau)d\tau = \int_{t_{0,M1}}^{t_{1,M1}} i_{N2}(\tau)d\tau \tag{4.23}$$

The equation above can give the ratio of L_1/L_{N1},

$$\frac{L_1}{L_{N1}} = \frac{(V_{c2} \cdot n_3 - V_o \cdot n_2)(n_2 \cdot T_s)}{L_m n_1 n_3 (\frac{n_3}{n_2} \cdot 2I_o + T_s \cdot \frac{n_2 \cdot V_o}{n_3 L_m})} - 1 \tag{4.24}$$

or

$$L_1 = \frac{V_{c2} T_s (1 - \frac{V_o n_2}{V_{c2} n_3})^2 \cdot (V_{c2} - V_m Sin\omega t_1)}{2I_o V_o + V_o^{\,2} \cdot \frac{n_2^{\,2} \cdot T_s}{n_3^{\,2} \cdot L_m}} - L_{N1} \tag{4.25}$$

4.3 Design Procedures

The method for designing the circuit of control loop and determining the voltage stresses of components voltage for the proposed converter is similar to that for designing the conventional forward converter. However, the transformer design needs more calculations and considerations since three windings are designed in this converter. The design method for transformer is shown as following.

1) Windings turns ratio $n_1/n_2/n_3$: The turn ratio n_2/n_3 can be obtained from equations (4.1)-(4.2) by using the substitutions of the given $V_{m,min}$, $V_{m,max}$, V_o, D_{max}, and $\omega t_{1,min}$, where $V_{m,min}$ and $V_{m,max}$ is the amplitude of minimum line voltage and maximum line voltage respectively, V_o is typical output voltage, D_{max} is the maximum duty ratio, and $0.4 \leqq D_{max} \leqq 0.45$. The corner angle $\omega t_{1,min}$, $0 < \omega t_{1,min} \leq \frac{\pi}{4}$, can be obtained as long as $V_{m,min}$ is chosen. The detailed steps for obtaining the turn ratio n_2/n_3 is depicted as follows:

   (i) Let V_{C2} be chosen lower than 420V at V_{in}=265V.

   (ii) Assume that V_{C2} is proportional to V_{in}. Then $V_{C2} \fallingdotseq 85 \times (420/265) = 134.7$V at V_{in}=85V.

   (iii) Let V_o=48V, D_{max}=0.4 then $48 = 134.7 \times (n_3/n_2) \times 0.4$, $n_3/n_2 \fallingdotseq 0.8$.

   (iv) Let $\omega t_{1,min}$=0.24, $V_{m,min} \fallingdotseq 120$V, V_o=48V, D_{max}=0.4, and n_2/n_3=1.2. Then the substitutions of all the data to equation (4.3) gives $n_1/n_2 \fallingdotseq 1.0$.

2) Magnetic inductance L_m and L_{N1}: Magnetizing current i_{Lm} stores energy to charge bulk

capacitor, so it is recommended to 20 percent of the primary load current.

$$L_m = \frac{V_{C2} \cdot D_{\max} T_s}{\Delta i_{Lm}}, \tag{4.26}$$

where $\Delta i_{Lm} \approx i_{N2}(t_{1,M1}) \cdot 20\%$.

The inductance L_{N1} can be yielded in equation (4.27)

$$L_{N1} / L_m = (\frac{n_1}{n_2})^2, \tag{4.27}$$

where n_2 can be obtained by solving Faraday's law,

$$n_2 = (V_{C2} \cdot D_{\max} T_s) / (A_e dB). \tag{4.28}$$

A_e is effective area of core and dB is flux density change in transformer core.

3) Series inductance L_1: The inductance L_1 can be yielded by putting above parameters in equation (4.25).

4) To confirm $dB<B_{\max}$: The maximum change value of magnetic flux density has to limit under maximum magnetic flux density for the selected magnetic material.

Given $L_m \cdot di_{Lm} = N_2 \cdot dB \cdot Ae$ or $dB = \frac{L_m \cdot di_{Lm}}{N_2 \cdot Ae}$, where di_{Lm} can be calculated by substituting DTs for $(t\text{-}t_{0,M2})$ in equation (4.14), Ae is the effective area of the selected magnetic core.

$$di_{Lm} = [i_{N1}(t_{0,M2}) + \frac{V_{C2}}{L_m} DTs]; \qquad \frac{L_m \cdot di_m}{N_2 \cdot Ae} < B_{\max}.$$

4.4 Experimental Results

The proposed structure has been tested under the specifications of 85V~265V/ac input voltage range, 50V/dc output voltage, and 100w output power. The turn ratio of $n_1/n_2/n_3$ is 27/23/12 and the inductance $L_1 << L_{N1}$, where L_1=30uH and transformer core PQ32/20 is used. The transformer core employed in previous similar converter should be EER35 in [4] and [7]. Although numerous previous similar converters have the transformer core size similar to that of the proposed converter in similar given output power and switching frequency, the boost

inductors sizes, 58uH-240uH in [4], 1.4mH in [7] or 1.7 times the magnetic inductance [28], are several times the L_1 in the proposed converter. The sizes of the boost inductors employed in [4] and [7] are still several times of L_1 when flowing a similar line current in the proposed converter. Figure 4.9 illustrates the line current in a full line cycle. Experiments have verified that the harmonic distribution complies with a standard of IEC 61000-3-2. Table 4.1 demonstrates that the detailed harmonic distribution of the prototype design meets the requirements of class D.

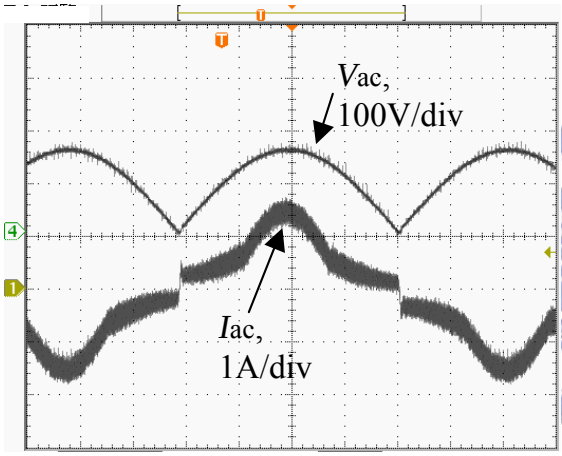


Fig. 4.9 i_{ac} & V_{ac} waveform at V_{ac}=110v ,Io=1.5A

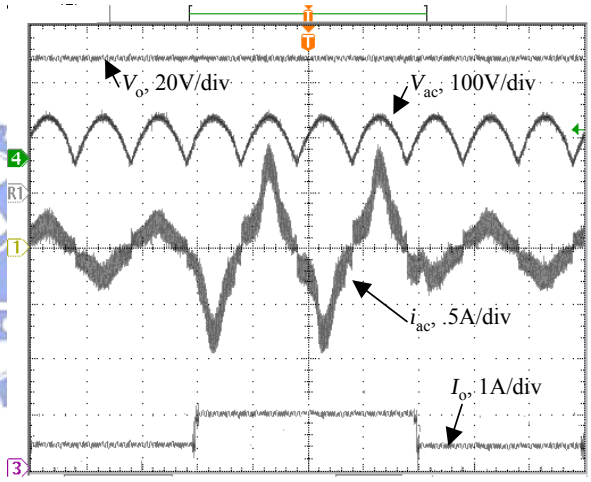


Fig. 4.10 Dynamic response waveforms for V_{ac}, i_{ac}, V_o and I_o when V_{ac}=110V, V_o=50V and I_o=0.5A/1A

Figure 4.10 illustrates dynamic response switching between a half and a full load under 110V/ac input voltage. The output voltage of the prototype displays a fast response and stable regulation. Moreover, Fig. 4.11 illustrates the voltages across the bulk capacitor for different input voltages under a full load. The voltage of the bulk capacitor depends on V_{ac} and turn-ratio n_1/n_3 but it is almost independent of load current. The maximum voltage can be held below 450V/dc, a popular commercial voltage in the market for electrolytic capacitors, by adjusting turn-ratio n_1/n_3.

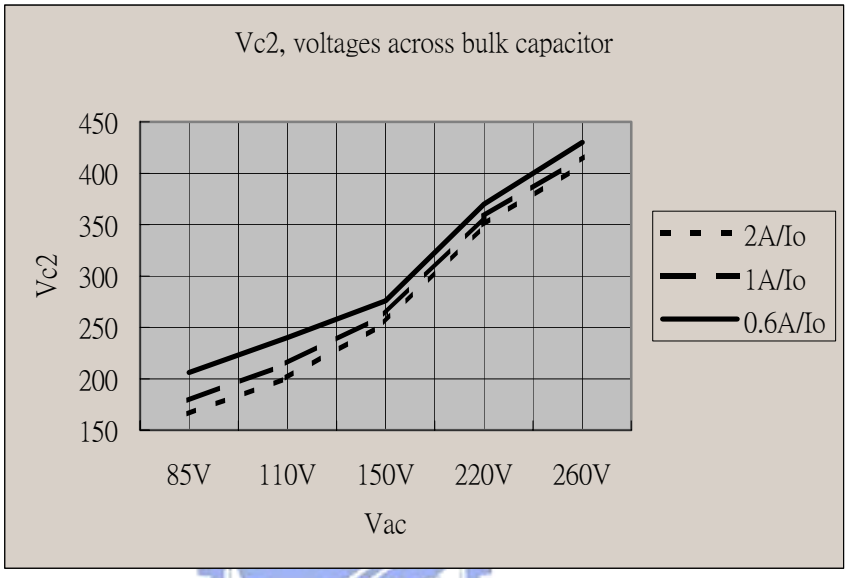


Fig. 4.11 Voltage stress of bulk capacitor V_{C2} and line voltage V_{ac}

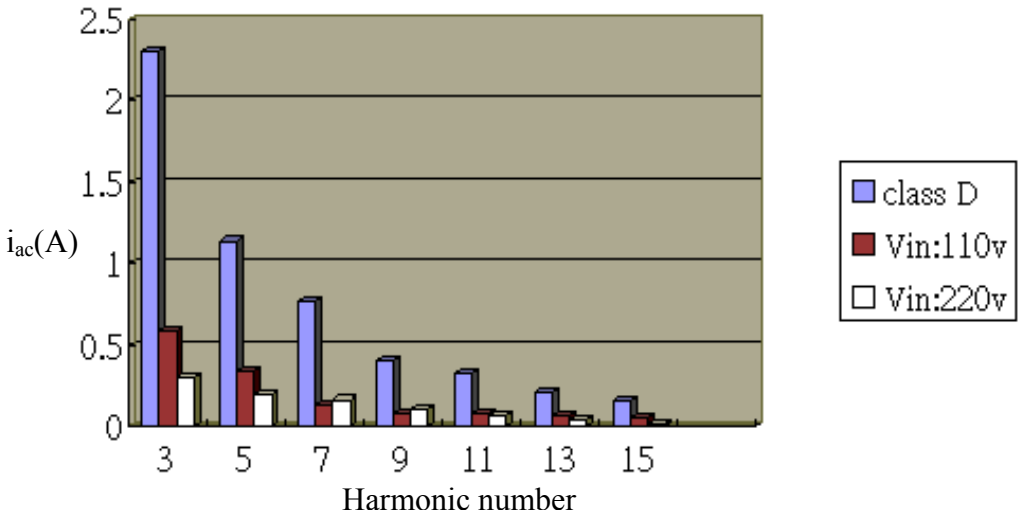


Table 4.1 The major harmonic components of the line current

Table 4.2 Voltage stress of S_1, Voltage across bulk capacitor C_2 and efficiency η.

V_{in} [V]	V_{S1} [V]	V_B [V]	η [%]
90	315	221	72
110	326	241	74
130	332	258	75.4
220	431	371	76
230	452	389	76.5
260	482	425	76.1

Table 4.2 illustrates the voltage stress in S_1, voltage across bulk capacitor C_2 and efficiency η. The voltage stress in S_1 is over 450V when input voltage V_{in} is over 260V. Therefore, an extended type with two switches forward converter can be adopted if user wants to reduce the voltage stress in S_1. The efficiency is penalized due to part of the power being processed twice. Moreover, that the converter operates in DCM at the current i_{N1} also causes the efficiency being slightly decreased.

4.5 Extension Circuit

The voltage stress across main switch in primary side will be over 500V when the proposed Forward converter is applied in wide range input voltage up to 265V. The high voltage stress will cause two drawbacks, expensive cost in MOSFET and high switching loss in the MOSFET. Therefore, an extension circuit is introduced to prevent the switch from the high voltage stress.

The extreme voltage stress on main switch can be obtained from equation (4.17).

$$V_{ds} = V_{C2} + (V_{C2} - V_{in}) \cdot \frac{n_2 L_{N1}}{n_1 (L_{N1} + L_1)} < 2V_{C2}, \tag{4.29}$$

Based on the data of prototype, the maximum voltage stress V_{ds} is no more than 860V where V_{C2} is 430V at input voltage 265V.

Figure 4.12 is the extension circuit, a twin-transistors type Forward converter, based on the proposed Forward circuit. The circuit adds a switch S_2 and the switch's operation is synchronous in S_1. Except the additional switch, there is no difference in comparing to the proposed Forward converter. The additional transistor can share a half voltage-stress in the single transistor Forward converter. Therefore, the high voltage stress issue can be released via the proposed twin-transistors Forward converter.

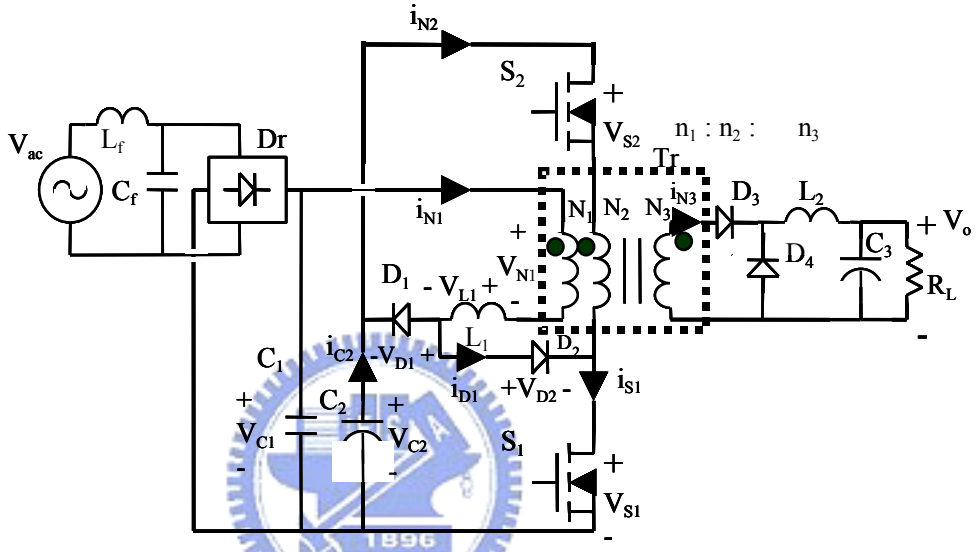


Fig. 4.12 The proposed twin transistors forward converter.

CHAPTER 5

THE FULL-BRIDGE CONVERTER USING THE PROPOSED INPUT CURRENT SHAPER

A Full-bridge AC/DC converter, with the functions of harmonic current elimination and fast output transient response, is proposed as shown in Figure 5.1. The circuit is a single-stage AC/DC converter consisting of 4 switches S_1-S_4, an input filter C_1, a bulk capacitor C_2, an inductor L_1 and a transformer with two primary windings N_1&N_2, where N_1 plays a role of magnetic feedback winding. The winding N_1, inductor $L_1$and diode D_5&D_6 form an input current shaper. The winding N_1, inductor L_1, diode D_6&D_3 (or D_5&D_1), switch S_2 (or S_4) and bulk capacitor C_2 forms a boost circuit. The winding N_2&N_3, a bulk capacitor C_2, switches S_1-S_4, diodes D_7, D_8, inductor L_2 and output capacitor C_3 forms a full-bridge converter. The switches S_1~S_4 are always MOSFETs so D_1~D_4 are the body diode in switches S_1~S_4.

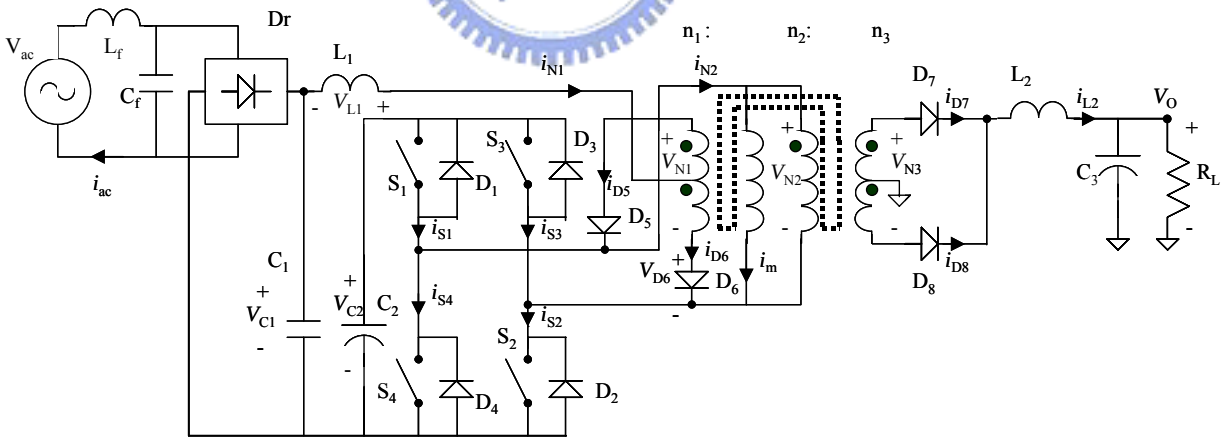


Fig. 5.1 Proposed Full-bridge AC/DC converter

The control method adopts a conventional fixed-frequency voltage mode control. The experimental results have shown that even using a popular fixed-frequency controller TL494, the line current of the proposed ac/dc converter can comply with the standard IEC 61000-3-2 and the converter also can have fast load dynamic response.

5.1 Basic Operation Theories

The operation principle of the proposed converter is somewhat similar to the boost-based forward AC/DC single-stage isolated power-factor-corrected power supply in the Chapter 4. Magnetic energy is stored in inductor L_1, used as an energy-flow switch, when switch S_1&S_2 are on. Electric energy will be delivered to bulk capacitor C_2 through L_1 when switch S_1&S_2 turn off. Windings N_2 and N_3 provide the energy storing and transferring components of the full-bridge stage. Winding N_1 provides a path to charge L_1 and also transfers the line energy to output loads in the duty on duration. In the duty off duration while L_1 still conducts, winding N_1 also induce current $i_{N1}\times(n_1/n_3)$ to secondary side. However, when the line voltage is greater then the winding voltage $V_{N1}/2$ in the duty on duration, the power line can more strongly charges C_2 through L_1 and winding N_1. In the charging duration of C_2, the line current $|i_{ac}|$ is greater than zero and grows fast as the waveform shown in time duration t_1-t_3 of Fig. 5.2. Thus, the slope of V_{C2} is positive during t_1-t_3 and negative in other duration in each half line cycle. The resulting waveform of V_{C2} is sketched in Fig. 5.2. In this circuit the capacitor C_2 is arranged with a capacitance similar to that used in conventional AC/DC full-bridge converters. Since C_2 is large so that V_{C2} can approximate to its average voltage, $V_{C2,av}$. The proposed circuit has two operation modes. Figure 5.2 shows these two operation modes that appear mirror-symmetrically in each quarter of a line cycle. Figure 5.3 shows the relative voltage and current waveforms in one switching cycle in two operation modes.

In this circuit, L_2 is designed in the operation of continuous conduction mode. Since V_{C2} is almost invariant, the duty ratio D can be approximate to constant one in the whole line cycle for fixed load. The circuit analysis will be presented in the following sections. Therefore, a duty cycle D will be assumed constant in these two operation modes and the analysis of L_2 will be taken according to the theorem of voltage-second balance in steady state design consideration.

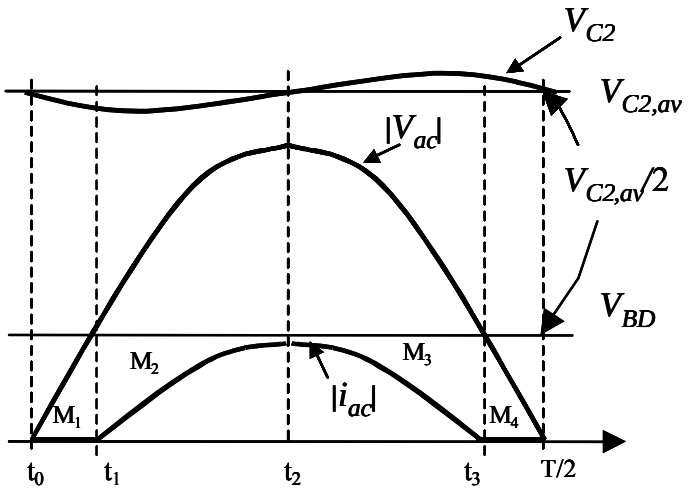


Fig. 5.2 Operation modes in one half of line cycle

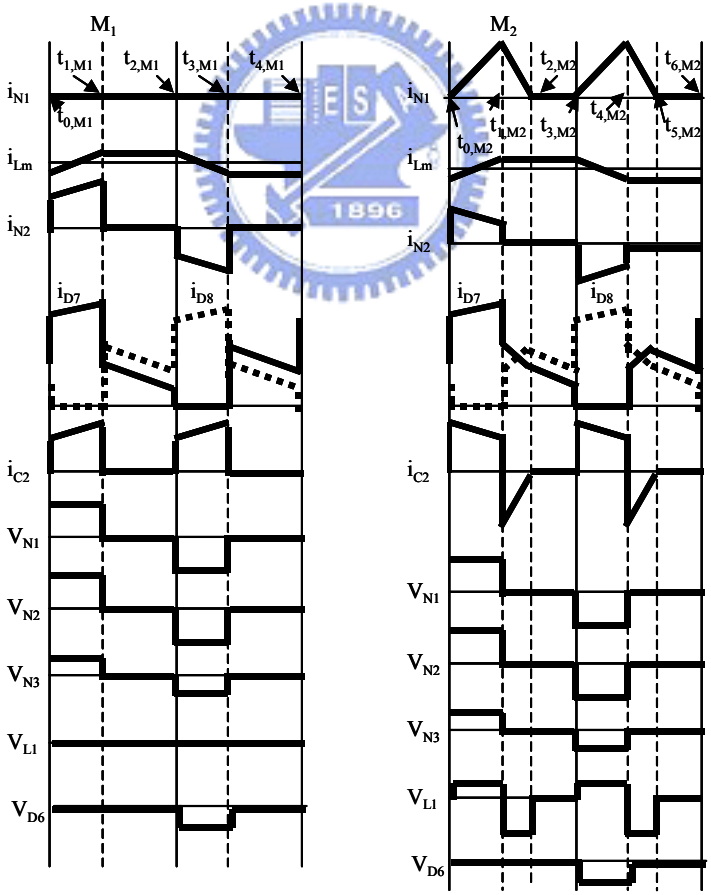


Fig. 5.3 Voltage and current waveforms in a switching cycle in the two modes

5.1.1 Operation Modes M_1 or M_4 (during t_0-t_1 or t_3-Tl /2)

Within this mode, the line current $|i_{ac}|$ and i_{N1} are zeros. The operation principle of the converter is the same as that working in the conventional full-bridge converter. Since C_2 is large enough, V_{C2} can approximate to a constant value during a line cycle. The output conductance L_2 and capacitance C_3 provide a good low pass. Thus the output voltage can be regarded to a constant value and can be obtained as

$$V_o = V_{C2} \cdot \frac{n_3}{2n_2} \cdot D\,, \tag{5.1}$$

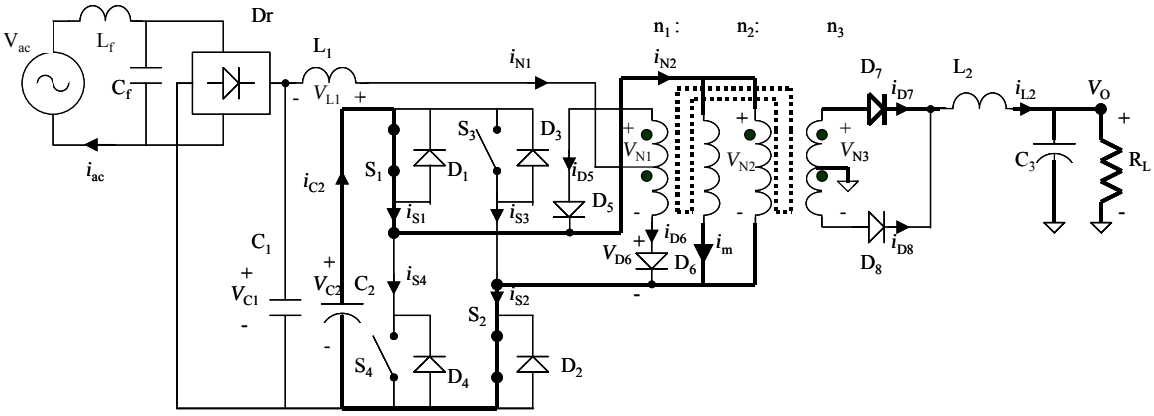
where D is defined as $\frac{t_{1,M1} - t_{0,M1}}{t_{2,M1} - t_{0,M1}}$ in mode M_1 or $\frac{t_{1,M2} - t_{0,M2}}{t_{3,M2} - t_{0,M2}}$ in mode M_2. Since the capacitance C_2 is assigned large, V_{C2} is assumed constant. Thus, for fixed load the duty ratio D can be assumed approximate to a constant in mode M_1 and M_2.

Since M_2 starts at the time when V_{C1} reach toV_{N1}. Thus, the time bound of mode M_1 can be obtained by

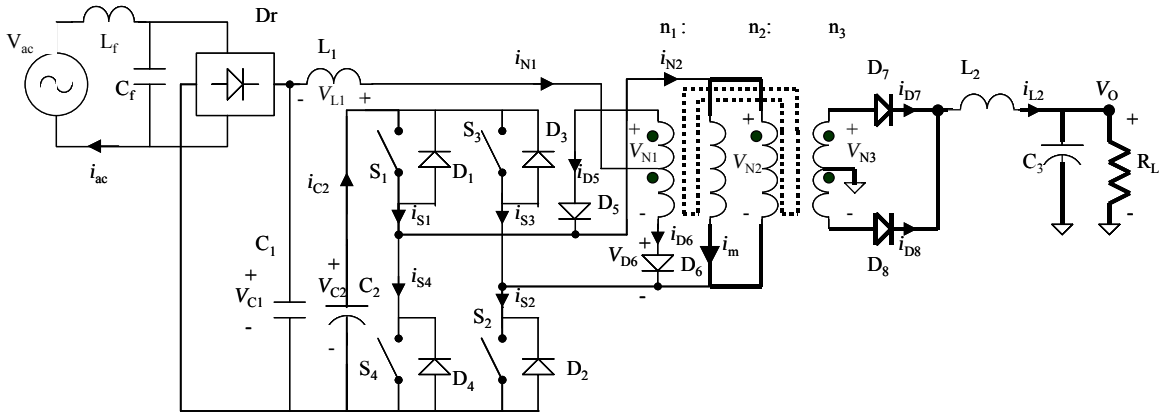
$$\mathrm{V_{BD}} = V_{C2} \cdot \frac{n_1}{2n_2} = V_o \cdot \frac{n_1}{D \cdot n_3} \tag{5.2}$$

or

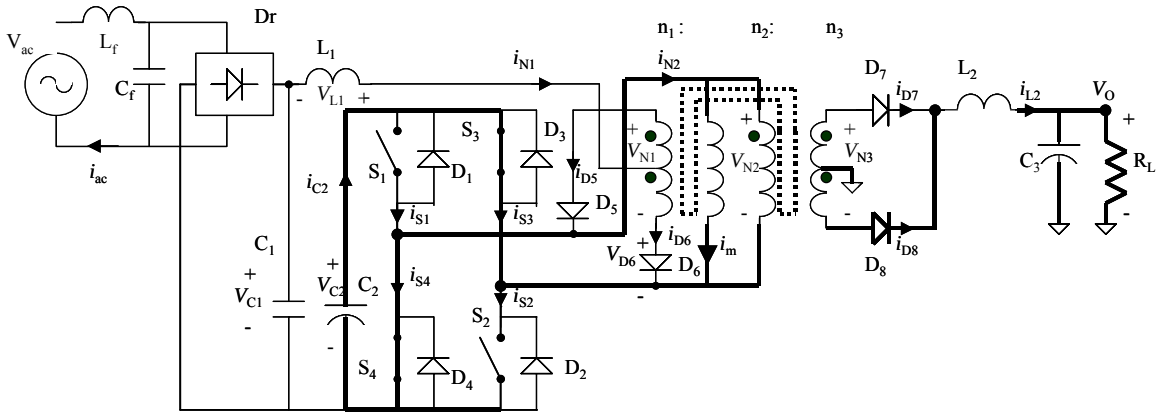
$$\omega t_1 = \sin^{-1}\left(\frac{V_o}{V_m} \cdot \frac{n_1}{D \cdot n_3}\right) \tag{5.3}$$



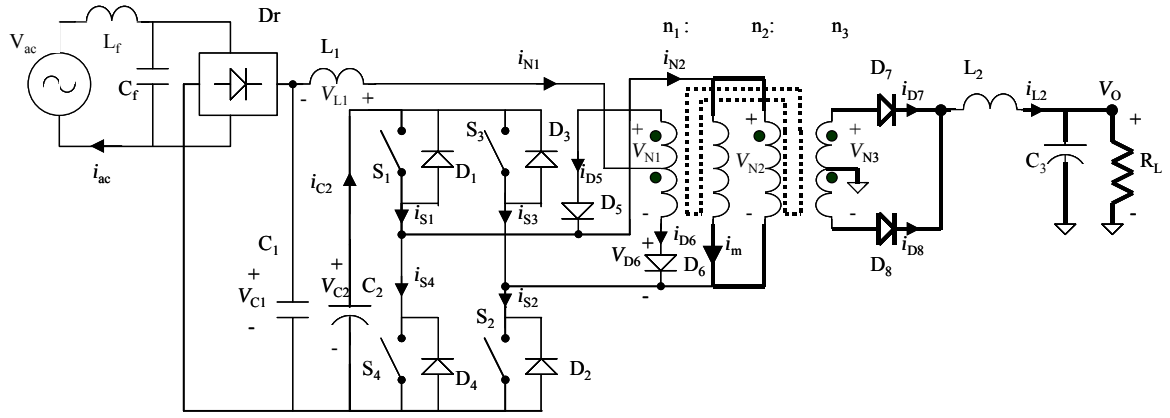
(a) $t_{0,M1} \leqq t < t_{1,M1}$



(b) $t_{1,M1} \leqq t < t_{2,M1}$



(c) $t_{2,M1} \leqq t < t_{3,M1}$



(d) $t_{3,M1} \leqq t < t_{4,M1}$

Fig. 5.4 Current loops while (a) S_1&S_2 turn on, (b) S_1&S_2 turn off, (c) S_3&S_4 turn on, and (d) S_3&S_4 turn off in M_1/M_4

1) **In $t_{0,M1} \leqq t < t_{1,M1}$** S_1&S_2 and D_7 are on, D_5, D_6, and D_8 are off. The capacitor C_2 discharges through S_1, N_2 and S_2 to ground. The magnetic current i_{Lm} has an initial value that flows in inverse direction at $t_{0,M1}$ and is left in the previous operation and the magnetic energy will be transferred to load through N_3 in the duration when i_{Lm} is still negative. The magnetic current keeps increasing linearly and changes to positive direction before $t_{1,M1}$. The induced current i_{N3} flows through D_7, L_2, C_3, and R_L. Since V_{C1} is smaller than $V_{N1}/2$, L_1 will not conduct in this mode.

2) In $t_{1,M1} \leqq t < t_{2,M1}$ D_7 and D_8 are turned on, S_1 and S_2 are off. Since L_2 is large and operates in CCM, i_{L2} is always large and forces both output regulators D_7 and D_8 conducting in the whole duty off duration.

3) In $t_{2,M1} \leqq t < t_{3,M1}$ S_3&S_4 and D_8 are on, D_5, D_6, and D_7 are off. The operation functions held in $t_{0,M1}$-$t_{1,M1}$ duration will also symmetrically happen in the other half circuit. The capacitor C_2 discharges through S_3, N_2 and S_4 to ground. The magnetic current i_{Lm} has an initial value that flows in inverse direction at $t_{2,M1}$ and left in the previous operation and the magnetic energy will be transferred to load through N_3 in the duration when i_{Lm} is still positive.

The magnetic current keeps decreasing linearly and changes to negative direction before $t_{3,M1}$. The induced current i_{N3} flows through D_7, L_2, C_3, and R_L. Since V_{C1} is smaller than $V_{N1}/2$, L_1 will not conduct in this mode.

4) In $t_{3,M1} \leqq t < t_{4,M1}$ D_7 and D_8 are turned on, S_3 and S_4 are off. Since L_2 is large and operates in CCM, i_{L2} is always large and forces both output regulators D_7 and D_8 conducting in the whole duty off duration.

Summing the descriptions above give the following results:

$$i_{N1} = \begin{cases} 0, & t_{0,M1} \le t < t_{2,M1} \\ 0, & t_{2,M1} \le t < t_{4,M1} \end{cases} \tag{5.4}$$

$$i_{N2} = \begin{cases} (I_o - \frac{1}{2}\Delta I_o) \cdot \frac{n_2}{2n_1} - \frac{I_m}{2} + \frac{(I_m + \frac{n_2}{2n_1} \cdot \Delta I_o)}{DT_s} \cdot t, & t_{0,M1} \le t < t_{1,M1}, \\ 0, & t_{1,M1} \le t < t_{3,M1} \end{cases} \tag{5.5}$$

$$i_m = \begin{cases} -\frac{I_m}{2} + \frac{V_{C2}}{L_m} \cdot t, & t_{0,M1} \le t < t_{1,M1} \\ \frac{I_m}{2}, & t_{1,M1} \le t < t_{2,M1} \\ \frac{I_m}{2} - \frac{V_{C2}}{L_m} \cdot t, & t_{2,M1} \le t < t_{3,M1} \\ -\frac{I_m}{2}, & t_{3,M1} \le t < t_{4,M1} \end{cases}, \tag{5.6}$$

where $\Delta I_o = \frac{(V_{C2} \times \frac{n_3}{n_2} - V_o)}{L_2} \cdot DT_s$, $I_m = \frac{V_{C2}}{L_m} \cdot DT_s$ and T_s is the period of switching cycle.

$$i_{D7}=\begin{cases}(I_o-\dfrac{\Delta I_o}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_o}{L_2}\cdot t, & t_{0,M1}\le t<t_{1,M1}\\ \dfrac{1}{2}(I_o+\dfrac{\Delta I_o}{2}-I_m\cdot\dfrac{n_2}{n_3})-\dfrac{V_o}{2L_2}\cdot t, & t_{1,M1}\le t<t_{2,M1}\\ 0, & t_{2,M1}\le t<t_{3,M1}\\ \dfrac{1}{2}(I_o+\dfrac{\Delta I_o}{2}+I_m\cdot\dfrac{n_2}{n_3})-\dfrac{V_o}{2L_2}\cdot t, & t_{3,M1}\le t<t_{4,M1}\end{cases} \tag{5.7}$$

$$i_{D8}=\begin{cases}0, & t_{0,M1}\le t<t_{1,M1}\\ \dfrac{1}{2}(I_o+\dfrac{\Delta I_o}{2}+I_m\cdot\dfrac{n_2}{n_3})-\dfrac{V_o}{2L_2}\cdot t, & t_{1,M1}\le t<t_{2,M1}\\ (I_o-\dfrac{\Delta I_o}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_o}{L_2}\cdot t, & t_{2,M1}\le t<t_{3,M1}\\ \dfrac{1}{2}(I_o+\dfrac{\Delta I_o}{2}-I_m\cdot\dfrac{n_2}{n_3})-\dfrac{V_o}{2L_2}\cdot t, & t_{3,M1}\le t<t_{4,M1}\end{cases}, \tag{5.8}$$

where ΔI_o is a ripple current.

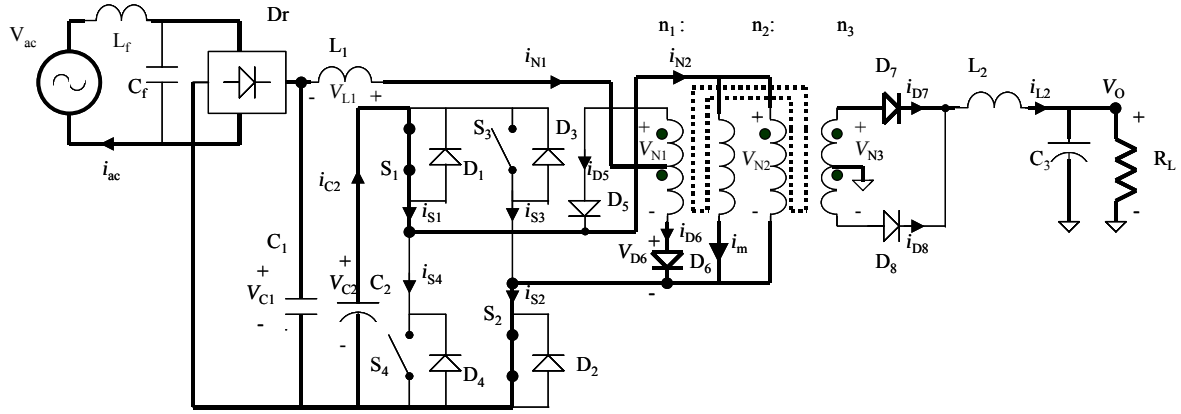
For the purpose of i_{L2} operating in CCM, the inductance L_2 has to conform to the following constraint. Let $i_{D7}\geqq 0$ at $t_{2,M1}$ in equation (5.7) can obtain the constraint.

$$L_2 \ge \frac{V_O(1-D)T_s}{I_O+\Delta I_O/2-I_m(n_2/n_3)}$$

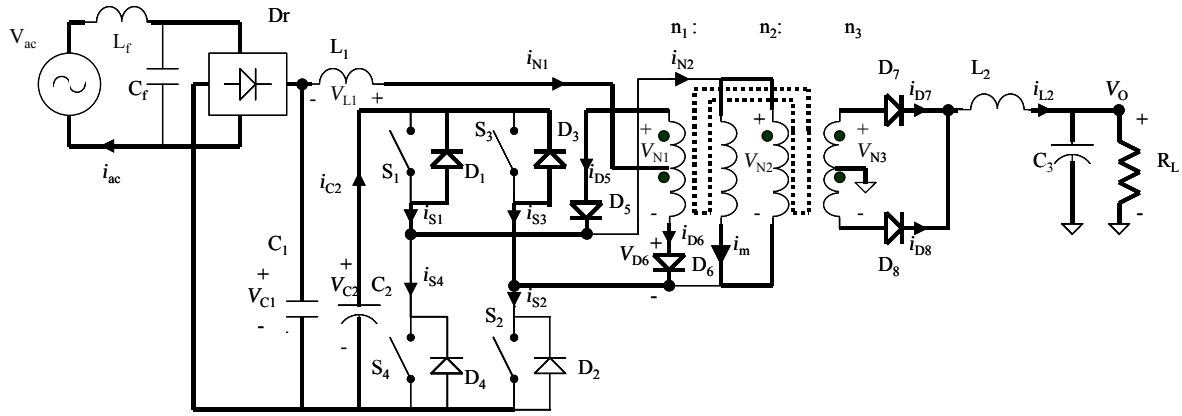
5.1.2 Operation Modes M_2 or M_3 (during t_1-t_2 or t_2-t_3)

The operation mode initially starts at the condition, $V_{ac}=V_{BD}$. When S_1 and S_2 turn on, D_6 is forced to turn on and current i_{N1} flows through the winding N_1, L_1, D_6, and S_2. Consequently, i_{N1} linearly increases. The capacitor C_2 supplies current i_{N2} flowing through S_1, winding N_2, and S_2. Simultaneously D_7 starts to turn on and the power is delivered to the load. When S_1 and S_2 turn off, the current i_{N1} starts to charge capacitor C_2 through L_1, winding N_1, D_5, D_6, D_1, and D_3 and linearly decreases to zero at time $t_{2,M2}$. Simultaneously D_7 and D_8 will continuously turn on and the power is delivered to the load. Figure 8 shows current loops in

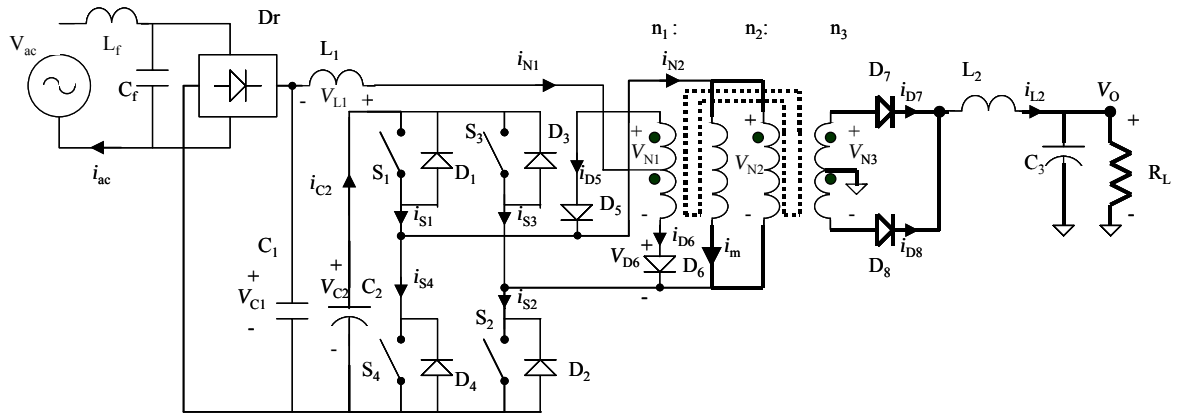
three operation stages in mode M_2/M_3.



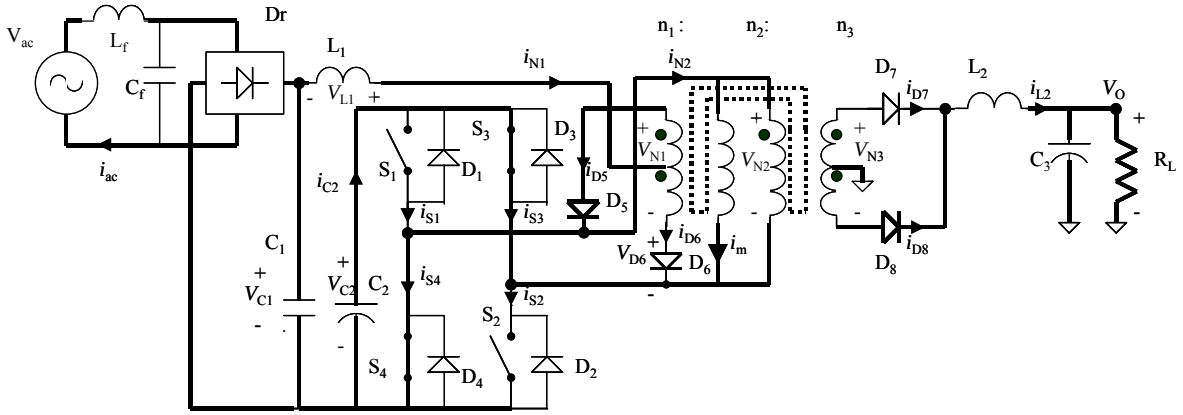
(a) $t_{0,M2} \leqq t < t_{1,M2}$



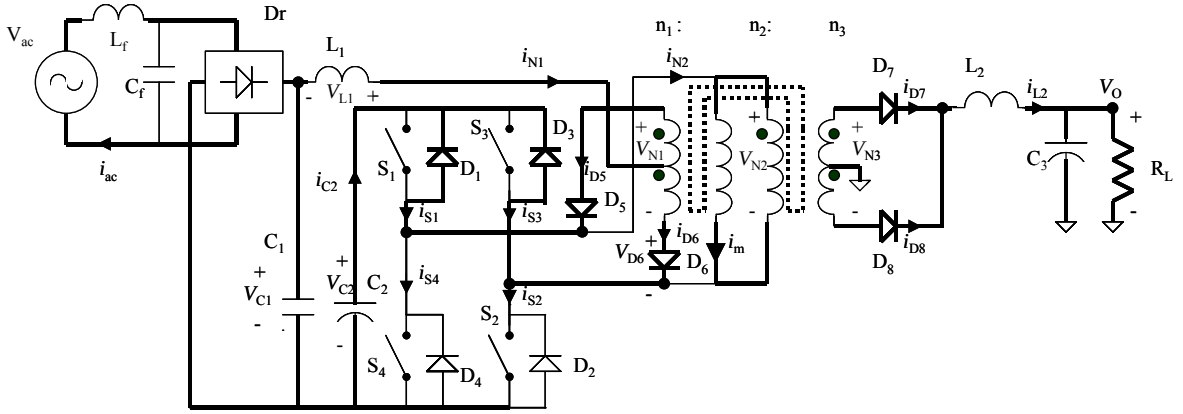
(b) $t_{1,M2} \leqq t < t_{2,M2}$



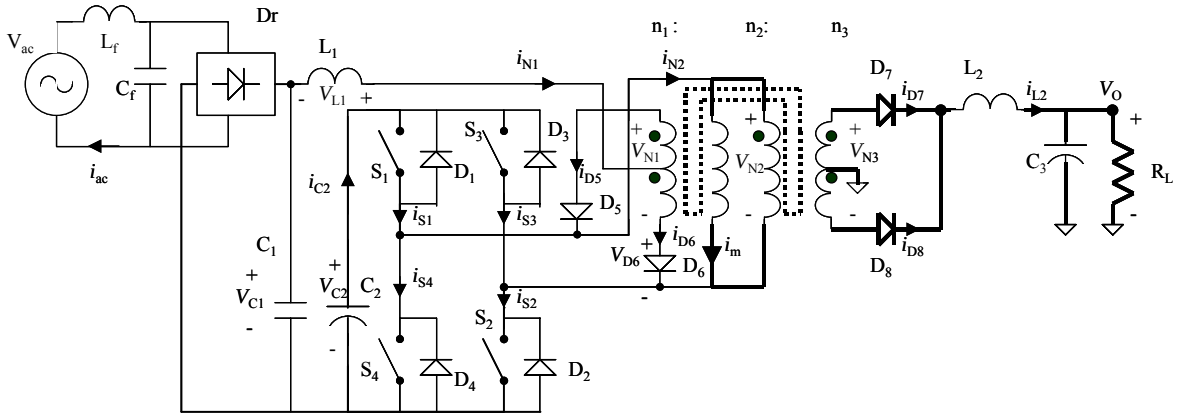
(c) $t_{2,M2} \leqq t < t_{3,M2}$



(d) $t_{3,M2} \leqq t < t_{4,M2}$



(e) $t_{4,M2} \leqq t < t_{5,M2}$



(f) $t_{5,M2} \leqq t < t_{6,M2}$

Fig. 5.5 Current loops while S_1&S_2 (a) turns on, (b)~(c) turns off in mode M_2/M_3, and S_3&S_4 (d) turns on, (e)~(f) turns off in mode M_2/M_3.

1) In $\mathbf{t_{0,M2}\text{-}t_{1,M2}}$ S_1, S_2, D_6, and D_7 are on, D_5 and D_8 are off. The capacitor C_2 begin to discharge through N_2, S_1, and S_2 to ground. That the input voltage V_{ac} is larger than $V_{N1}/2$ results in the difference voltage of V_{ac}-$V_{N1}/2$ dropped across on L_1. Hence the current i_{N1} begins to linearly increase from $t_{0,M2}$ to $t_{1,M1}$. When the current i_{N1} linearly increases as shown in Fig. 5.4 (a), the current i_{N1} will induce part of i_{N3} while the other part is provided by i_{N2}. Since winding N_2 is connected to V_{C2} through S_1 and S_2, the current i_m will increase linearly from negative to positive one as shown in Fig. 5.3. Therefore, i_{N2} must provide the current needed by i_m and part of i_{N3}, the other part of which is provided from N_1.

2) **In $\mathbf{t_{1,M2}\text{-}t_{2,M2}}$** D_1, D_3, D_5, and D_6 are on, S_1 and S_2 turn off. This duration ends at the time when i_{N1} falls to zero. The current i_{N1} starts to decrease and simultaneously provides a path to charge C_2 through L_1, N_1, D_5, D_6, D_1, and D_3. While consider the current continuity of the bottom part of winding N_1, the net current $i_{D8} - i_{D7}$ of winding N_1, will induce net current i_{D6}-i_{D5} to winding N_3. The output inductance current i_{L2}, that is designed to operate in CCM, will force both the diodes D_7 and D_8 conducting together. Therefore, V_{N3} is approximate to zero and results in V_{N1} being approximate to zero too. Consequently, the remaining magnetic current i_m will be diverted to windings N_3. Thus, i_m can be formulated by

$$i_m = (i_{D8} - i_{D7}) \cdot \frac{n_3}{n_2} + (i_{D6} - i_{D5}) \cdot \frac{n_1}{n_2}$$

3) In $\mathbf{t_{2,M2}\text{-}t_{3,M2}}$ D_7 and D_8 are on, D_1, D_3, D_5, D_6 , and S_1 and S_2 turn off. The current i_{N1} is zero . This situation implies that the energy stored in L_1 has released to C_2. The magnetic current i_m keeps almost a constant value since winding N_3 is still in shorted-circuit state and diverts to winding N_3. In this duration, the difference of i_{D8} and i_{D7} is kept near constant.

4) In $\mathbf{t_{3,M2}\text{-}t_{6,M2}}$ These time durations have same operation theory as described in the three statements above held in $t_{0,M2}$-$t_{1,M2}$.

The related equations are explained as followings.

$$i_{N1}=\begin{cases}\dfrac{V_{C1}-\dfrac{V_{N1}}{2}}{L_1}\cdot t, & t_{0,M2}\le t<tt_{1,M2}\\ \dfrac{V_{C1}-V_{C2}\cdot\dfrac{n_1}{2n_2}}{L_1}\cdot DT_s-\dfrac{V_{C2}-V_{C1}}{L_1}\cdot t, & t_{1,M2}\le t<t_{2,M2}\\ 0, & t_{2,M2}\le t<t_{3,M2}\end{cases} \tag{5.9}$$

Let i_{N1} be equal to zero at $t_{2,M2}$. The time $t_{2,M2}$-$t_{1,M2}$ (or $t_{5,M2}$-$t_{4,M2}$) can be obtained as below equations.

$$t_{2,M2}-t_{1,M2}=\frac{V_{C1}-V_{C2}\cdot\dfrac{n_1}{2n_2}}{V_{C2}-V_{C1}}\cdot DT_s \tag{5.10}$$

$$i_m=\begin{cases}-\dfrac{I_m}{2}+\dfrac{V_{C2}}{L_m}\cdot t, & t_{0,M2}\le t<t_{1,M2}\\ \dfrac{I_m}{2}, & t_{1,M2}\le t<t_{2,M2}\\ \dfrac{I_m}{2}, & t_{2,M2}\le t<t_{3,M2}\\ \dfrac{I_m}{2}-\dfrac{V_{C2}}{L_m}\cdot t, & t_{3,M2}\le t<t_{4,M2}\\ -\dfrac{I_m}{2}, & t_{4,M2}\le t<t_{5,M2}\\ -\dfrac{I_m}{2}, & t_{5,M2}\le t<t_{6,M2}\end{cases} \tag{5.11}$$

$$i_{D7}=\begin{cases}(I_o-\dfrac{\Delta I_o}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_o}{L_2}\cdot t, & t_{0,M2}\le t<t_{1,M2}\\ \dfrac{1}{2}[I_O+\dfrac{1}{2}\Delta I_O+\dfrac{V_{C1}-V_{C2}(n_1/2n_2)}{L_1}\cdot DT_s\cdot\dfrac{n_1}{n_3}-(\dfrac{V_{C2}-V_{C1}}{L_1}\cdot\dfrac{n_1}{n_3}+\dfrac{V_o}{L_2})(t-t_{1,M2})], & t_{1,M2}\le t<t_{2,M2}\\ i_{D7}(t_{2,M2})-\dfrac{V_o}{2L_2}\cdot t, & t_{2,M2}\le t<t_{3,M2}\\ 0, & t_{3,M2}\le t<t_{4,M2}\\ i_{L2}-i_{D8}, & t_{4,M2}\le t<t_{5,M2}\\ i_{D7}(t_{5,M2})-\dfrac{V_o}{2L_2}\cdot t, & t_{5,M2}\le t<t_{6,M2}\end{cases},$$

(5.12)

$$i_{D8}=\begin{cases}0, & t_{0,M2}\le t<t_{1,M2}\\ i_{L2}-i_{D7}, & t_{1,M2}\le t<t_{2,M2}\\ i_{D8}(t_{2,M2})-\dfrac{V_o}{2L_2}\cdot t, & t_{2,M2}\le t<t_{3,M2}\\ (I_o-\dfrac{\Delta I_o}{2})+\dfrac{V_{C2}\cdot\dfrac{n_3}{n_2}-V_o}{L_2}\cdot t, & t_{3,M2}\le t<t_{4,M2}\\ \dfrac{1}{2}[I_O+\dfrac{1}{2}\Delta I_O+\dfrac{V_{C1}-V_{C2}(n_1/2n_2)}{L_1}\cdot DT_s\cdot\dfrac{n_1}{n_3}-(\dfrac{V_{C2}-V_{C1}}{L_1}\cdot\dfrac{n_1}{n_3}+\dfrac{V_o}{L_2})(t-t_{4,M2})], & t_{4,M2}\le t<t_{5,M2}\\ i_{D8}(t_{5,M2})-\dfrac{V_o}{2L_2}\cdot t, & t_{5,M2}\le t<t_{6,M2}\end{cases}$$

(5.13)

$$i_{N2}=\begin{cases}i_m+(i_{D7}\cdot\dfrac{n_3}{n_2}-i_{N1}\cdot\dfrac{n_1}{n_2}), & t_{0,M2}\le t<t_{1,M2}\\ 0, & t_{1,M2}\le t<t_{2,M3}\\ -[i_m+(i_{D8}\cdot\dfrac{n_3}{n_2}-i_{N1}\cdot\dfrac{n_1}{n_2})], & t_{3,M2}\le t<t_{4,M2}\\ 0, & t_{4,M2}\le t<t_{6,M2}\end{cases}$$

(5.14)

$$V_{N1}=\begin{cases} V_{C2}\cdot\dfrac{n_1}{n_2}, & t_{0,M2}\le t<t_{1,M2} \\ 0, & t_{1,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \\ V_{C2}\cdot\dfrac{n_1}{n_2}, & t_{3,M2}\le t<t_{4,M2} \\ 0, & t_{4,M2}\le t<t_{5,M2} \\ 0, & t_{5,M2}\le t<t_{6,M2} \end{cases} \tag{5.15}$$

$$V_{N2}=\begin{cases} V_{C2}, & t_{0,M2}\le t<t_{1,M2} \\ 0, & t_{1,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \\ V_{C2}, & t_{3,M2}\le t<t_{4,M2} \\ 0, & t_{4,M2}\le t<t_{5,M2} \\ 0, & t_{5,M2}\le t<t_{6,M2} \end{cases} \tag{5.16}$$

$$V_{N3}=\begin{cases} V_{C2}\cdot\dfrac{n_3}{n_2}, & t_{0,M2}\le t<t_{1,M2} \\ 0, & t_{1,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \\ -V_{C2}\cdot\dfrac{n_3}{n_2}, & t_{3,M2}\le t<t_{4,M2} \\ 0, & t_{4,M2}\le t<t_{5,M2} \\ 0, & t_{5,M2}\le t<t_{6,M2} \end{cases} \tag{5.17}$$

$$V_{L1}=\begin{cases} \dfrac{V_{N1}}{2}-V_{C2}, & t_{0,M2}\le t<t_{1,M2} \\ V_{C2}-V_{C1}, & t_{1,M2}\le t<t_{2,M2} \\ 0, & t_{2,M2}\le t<t_{3,M2} \\ \dfrac{V_{N1}}{2}-V_{C2}, & t_{3,M2}\le t<t_{4,M2} \\ V_{C2}-V_{C1}, & t_{4,M2}\le t<t_{5,M2} \\ 0, & t_{5,M2}\le t<t_{6,M2} \end{cases} \tag{5.18}$$

5.2. Analysis of Converter Operation

5.2.1 Line current and Duty ratio

The line current i_{ac} mainly contains the line frequency part that is achieved by i_{N1}

through low pass filter L_r-C_r. The line current $|i_{ac}|$ is approximate to the average current of i_{N1} in a switching cycle. Equation (5.9) shows that i_{N1} is a linear function of V_{in}, or $|V_{ac}|$, in mode M_2 and also in mode M_3 due to the mirror-like symmetry relation between these two modes.

Since the capacitance C_2 is assigned large, V_{C2} is assumed constant. Thus, for fixed load the duty ratio D can be assumed approximate to a constant. Under the assumptions the relation of V_{C2} and duty ratio D can be found through employing equation (5.1)

Additionally, in the CCM operation regarding i_{L2}, the duty ratio D will be also kept approximately a constant in different load current since the inductor L_2 is large and operates in a continuous current mode. The relation between V_{C2} and duty ratio is shown in equation (5.1) and Fig. 5.6.

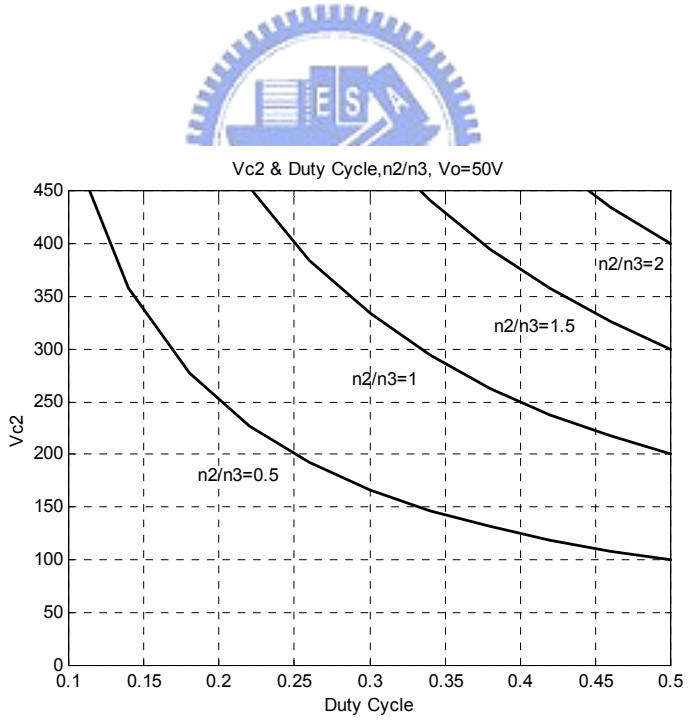


Fig. 5.6 V_{C2} & Duty cycle, n_2/n_3 at V_o=50V

5.2.2 Corner angle of line current

A corner angle (CA) of line current is defined as $\omega(t_1 - t_0)$. Equation (5.3) shows the

relation between CA and parameters. Equation (5.3) and Fig. 5.7 show that CA decreases as V_o/V_m or n_1/n_3 decrease. A smaller CA will result in a higher power factor and lower THD.

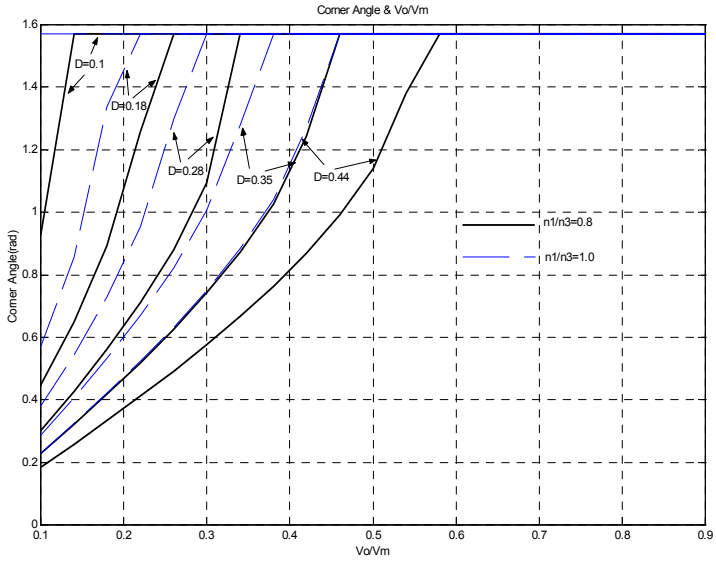


Fig. 5.7 Corner angle and V_o/V_m

5.2.3 Voltage across bulk capacitor

V_{C2} is the voltage across bulk capacitor C_2. There is an easy way to estimate V_{C2}. That is to find it at the time when the corner angle (CA) is reached. The inductance current i_{L1} is near zero at CA time and V_{C2} can be obtained as

$$V_{C2} = (V_m \sin\omega t_1) \cdot \frac{n_2}{n_1} \tag{5.19}$$

The relation between the voltage V_{C2}, n_2/n_1, CA, and input line voltage amplitude V_m, is shown in Fig. 5.8. In practical application, V_{C2} should be smaller than 450v/dc in wide range input (90v~265v/AC). Therefore, two parameters, n_2/n_1 and CA, have to meet the requirement in a given output V_o.

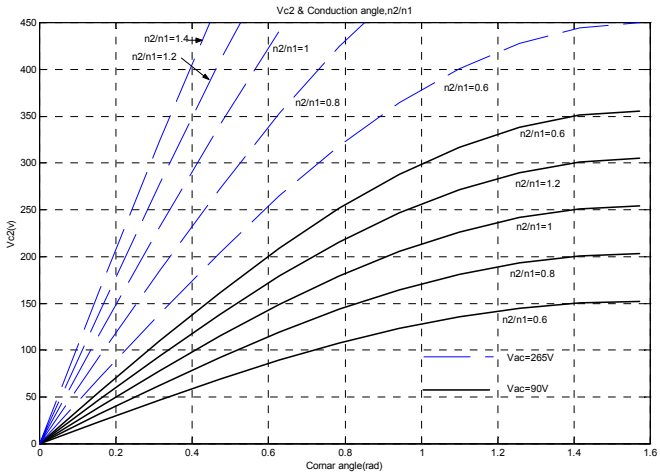


Fig. 5.8 V_{C2}, Conduction angle and n_2/n_1

5.2.4 Inductor L_1 calculation

The inductance of L_1 has three operation functions, providing energy storing in $t_{0,M2}$-$t_{1,M2}$ and transferring to capacitor C_2 in $t_{1,M2}$-$t_{2,M2}$ and line power energy transferring path to C_2 in duration $t_{1,M2}$-$t_{2,M2}$. Simultaneously, the inductance L_1 determines the line current waveform. A larger inductance L_1 will result in greater line current waveform distortion because the current i_{N1} will operate in CCM between t_2 and t_3, as shown in Fig. 5.9. Figure 5.10 shows the better waveform in line current while a suitable inductance is used and the inductance current i_{L1} operates in DCM.

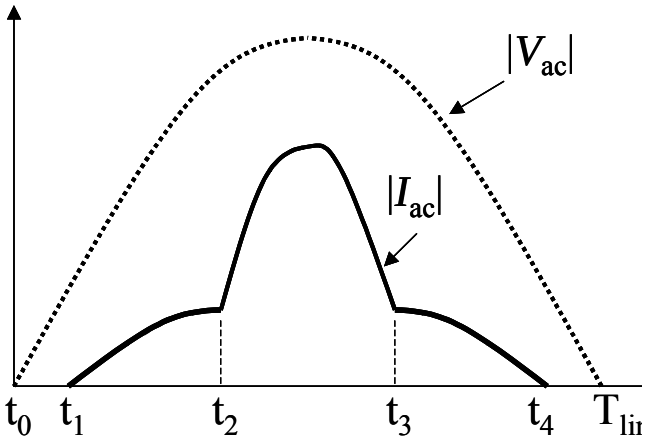


Fig. 5.9 Line voltage and line current waveforms, i_{N1} in CCM between t_2 and t_3.

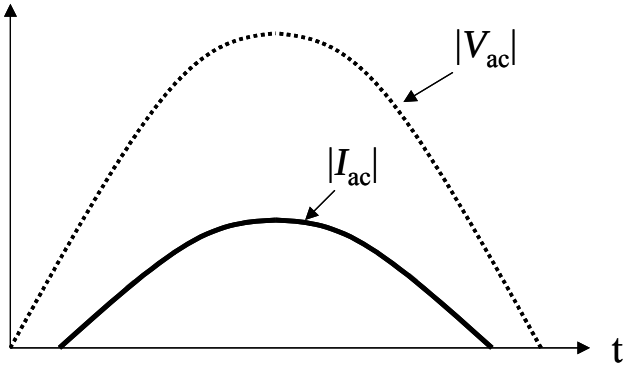


Fig. 5.10 Line voltage and line current waveforms, i_{N1} in DCM.

The inductance L_1 will be designed in considering the energy transportation operated in the steady state; it is that the output power should be equal to the input power by a factor of power efficiency in each switching cycle. Therefore, $P_{in} = P_o / \eta$, where η is power transfer efficiency. Further, the average input power can be obtained by $\overline{P}_{in} = \overline{V}_{C1} \times \overline{i}_{N1}$, where $\overline{V}_{C1}$ and $\overline{i}_{N1}$ is average value for V_{C1} and i_{N1} respectively.

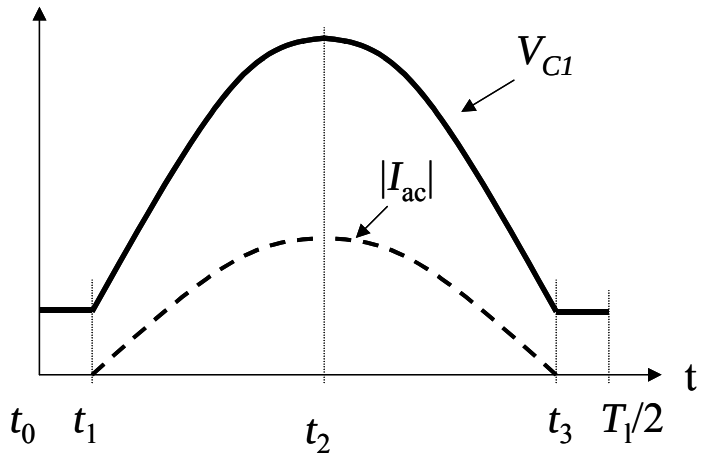


Fig. 5.11 The waveforms for V_{C1}&$|I_{ac}|$.

Fig. 5.11 shows the waveforms of the line voltage and current in a half-line cycle. Since C_1 is chosen as a switching frequency filter. Hence, according to Fig. 5.11, the average voltage $\overline{V}_{C1}$ of V_{C1} can be obtained by the following equation.

$$\begin{aligned}\overline{V}_{C1} &= \frac{2}{\pi}\cdot\int_0^{\pi/2} V_{ac}\,d\omega t = \frac{2}{\pi}\cdot\int_0^{\pi/2} V_m \sin\omega t d\omega t \\ &= (\omega t_1 \cdot V_m \sin\omega t_1 + V_m \cos\omega t_1)\cdot\frac{2}{\pi}\end{aligned} \tag{5.20}$$

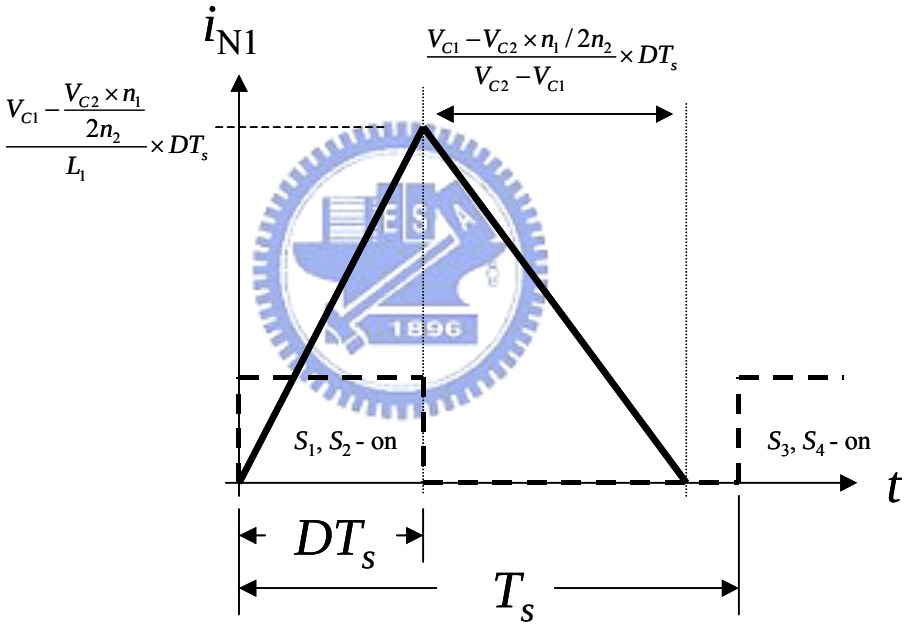


Fig. 5.12 The i_{N1} waveform and related parameters.

To formulate the equation of i_{N1}, the parameters, i_{N1peak} and the total falling time, as indicated in Fig.5.12, are formulated via equation (5.9). Since in a half line cycle the average of the high order harmonics of i_{N1} is zero, the average current $\bar{i}_{N1}$ can be obtained by simply averaging only the fundamental component of i_{N1}. Hence, the parameters, i_{N1peak} and the total falling time, as indicated in Fig.5.12, are formulated via equation (5.9). The fundamental component of i_{N1} is approximate to the average value of i_{N1} in a switching cycle. Therefore,

$\bar{i}_{N1}$ can be obtained as

$$\bar{i}_{N1}=\frac{2}{\pi}\int_{\omega t_1}^{\pi/2}\left(\frac{V_{C1}-\frac{V_{C2}\cdot n_1}{2n_2}}{L_1}\cdot\frac{DT_s}{2}\cdot\frac{DT_s+\frac{V_{C1}-V_{C2}\cdot n_1/2n_2}{V_{C2}-V_{C1}}\cdot DT_s}{T_s}\right)d\omega t \tag{5.21}$$

$$\begin{aligned}&=\frac{D^2T_sV_{C2}}{\pi L_1}\cdot(1-\frac{n_1}{2n_2})[(-\frac{\pi}{2}+wt_1)+2(1-\frac{n_1}{2n_2})\cdot\\&\frac{1}{\sqrt{1-(V_m/V_{C2})^2}}(\tan^{-1}\frac{\pi/2-V_m/V_{C2}}{\sqrt{1-(V_m/V_{C2})^2}}-\tan^{-1}\frac{wt_1-V_m/V_{C2}}{\sqrt{1-(V_m/V_{C2})^2}})]\end{aligned} \tag{5.22}$$

Substituting $\frac{P_o}{\eta V_{C1}}$ for i_{N1} gives the results of two equations below,

$$\begin{aligned}L_1=&\frac{1}{(P_o/\eta)/\bar{V}_{C1}}\cdot\frac{D^2T_sV_{C2}}{\pi}\cdot(1-\frac{n_1}{2n_2})[(-\frac{\pi}{2}+wt_1)+2(1-\frac{n_1}{2n_2})\cdot\\&\frac{1}{\sqrt{1-(V_m/V_{C2})^2}}(\tan^{-1}\frac{\pi/2-V_m/V_{C2}}{\sqrt{1-(V_m/V_{C2})^2}}-\tan^{-1}\frac{wt_1-V_m/V_{C2}}{\sqrt{1-(V_m/V_{C2})^2}})]\end{aligned} \tag{5.23}$$

V_{C1} is equal to $V_m\sin\omega t$.

5.3 Design Procedures

The method for designing the circuit of control loop and determining the voltage stresses of components voltage for the proposed converter is similar to that for designing the conventional forward converter. Again the transformer design needs more calculations and considerations. The design method for transformer is shown as following.

1) Windings turns ratio $n_1/n_2/n_3$: The turn ratio n_2/n_3 can be obtained from equations (5.1)-(5.3) by using the substitutions of the given $V_{m,min}$, $V_{m,max}$, V_o, D_{max}, and $\omega t_{1,min}$, where $V_{m,min}$ and $V_{m,max}$ is the amplitude of minimum line voltage and maximum line voltage respectively, V_o is typical output voltage, D_{max} is the maximum duty ratio, and $0.4\leqq D_{max}\leqq 0.45$. The corner angle $\omega t_{1,min}$, $0<\omega t_{1,min}\leq\frac{\pi}{4}$, can be obtained as long as $V_{m,min}$ is chosen. The detailed steps for obtaining the turn ratio n_2/n_3 is depicted as follows:

(i) Let V_{C2} be chosen not greater 420V at V_{in}=265V.

(ii) Assume that V_{C2} is proportional to V_{in}. Then $V_{C2} \fallingdotseq 85\times(420/265)\times k=168$ while V_{in}=85V, where k is nonlinear factor and let k=1.25

(iii) Let V_o=48V, D_{max}=0.4 then $48=168\times[n_3/(2n_2)]\times 0.4$, $n_3/n_2 \fallingdotseq 1.4$

(iv) Let $\omega t_{1,min}$=0.24, $V_{m,min} \fallingdotseq 120$V, V_o=48V, D_{max}=0.4, and n_2/n_3=0.7. Then replacing these data in (5.3) gives $n_1/n_3 \fallingdotseq 0.2$.

2) Magnetic inductance L_m and L_{N1}: Since the magnetizing current i_{Lm} transfers to output port each switching cycle, to reduce the output ripple voltage, the output inductance current i_{L2} is biased in CCM and to be much greater than the current component transferred from i_{Lm}. Therefore, the current transferred from i_{Lm} is recommended to be 10 percent of the primary load current.

$$L_m = \frac{V_{C2} \cdot D_{max} T_s}{\Delta i_{Lm}}, \tag{5.24}$$

$$L_{N1} / L_m = (\frac{n_1}{n_2})^2, \quad (i.e\ L_m = L_{N2}) \tag{5.25}$$

where n_2 can be obtained by solving Faraday's law,

$$n_2 = (V_{C2} \cdot D_{max} T_s)/(A_e dB). \tag{5.26}$$

A_e is effective area of core and dB is flux density swing in transformer core. The flux density swing, dB, can be designed as 2 times B_{sat} in full-bridge converter. For instance, B_{sat} for power ferrites such as 3C8 material is near 0.3 Tesla (3000 Gauss).

3) Series inductance L_1: The inductance L_1 can be yielded by putting above parameters in equation (5.23).

5.4. Simulation Results

The proposed structure has been simulated in the specifications of 85v~265v/ac input voltage, 50v/dc output voltage and 500w output power. The turn-ratio of n_1:n_2:n_3 is 0.2:0.7:1

and the ratio of L_1/L_{N1} (L_{N1}=54μH) is 0.31. Fig. 5.13 shows the line current in a full line cycle. The experiments have shown that the harmonic distribution complies with a standard of IEC 61000-3-2. Table.1 shows that the detail harmonic distribution of the prototype and the harmonic contents meet the requirements of class D.

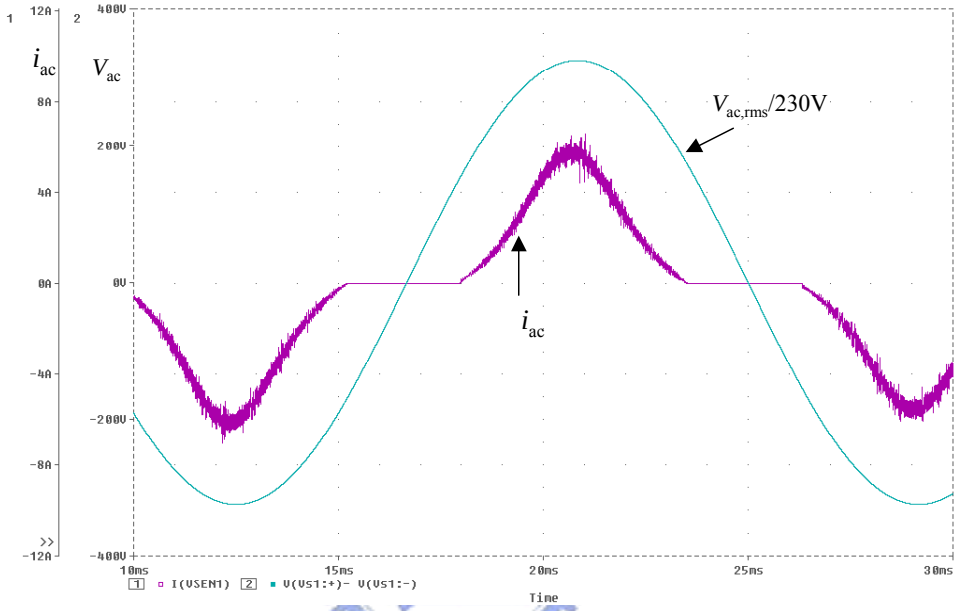


Fig. 5.13 i_{ac} & V_{ac} waveform at V_{ac}=230v ,I_o=10A

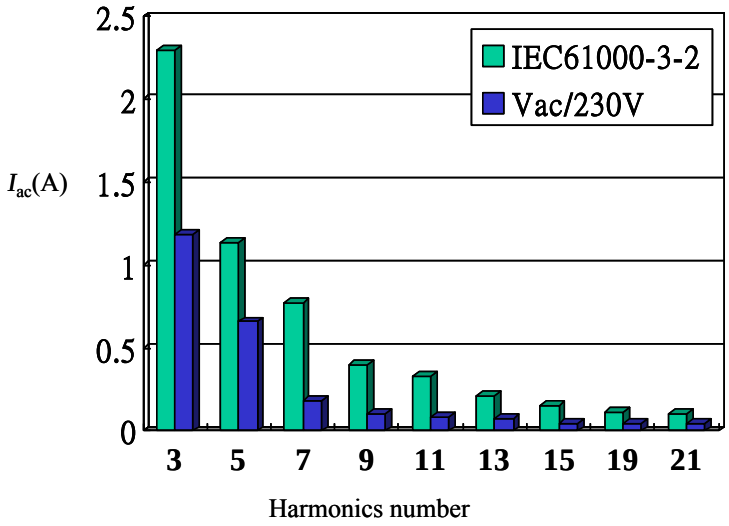


Table. 5.1 The major harmonic components of the line current, P_o=50V • 10A.

Figure 5.14 shows dynamic response from a half-load to full-load in 230V/AC input voltage. The output voltage of simulated circuit has a fast response and stable regulation. Figure 5.15 shows the voltages across on bulk capacitor in different input voltage at full load. The bulk capacitor's voltage will dependent on V_{ac}, duty ratio D, and turn-ratio n_2/n_3 but it is almost independent of load current. The maximum voltage can be held under 450v/dc, which is a commercially available voltage ratio for electrolytic capacitor, by adjusting turn-ratio n_1/n_3.

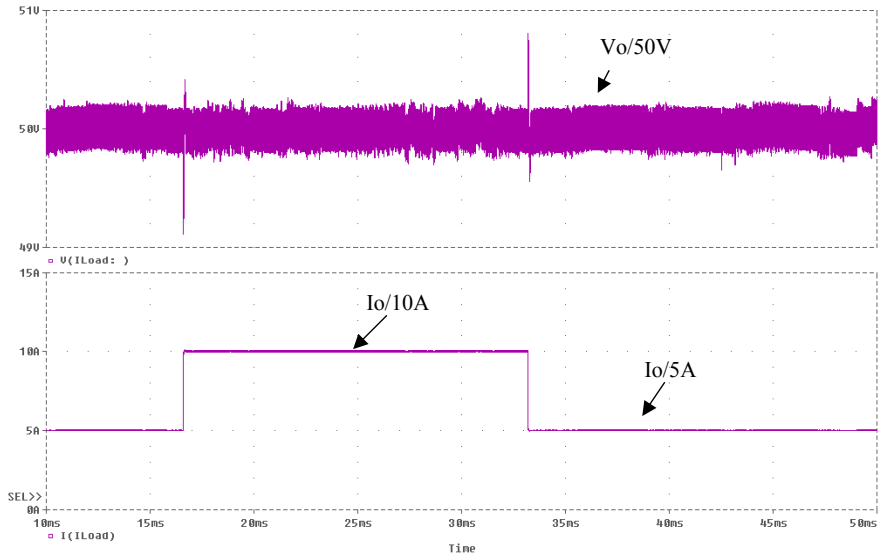


Fig. 5.14 Dynamic response waveforms for V_{ac}, i_{ac}, V_o

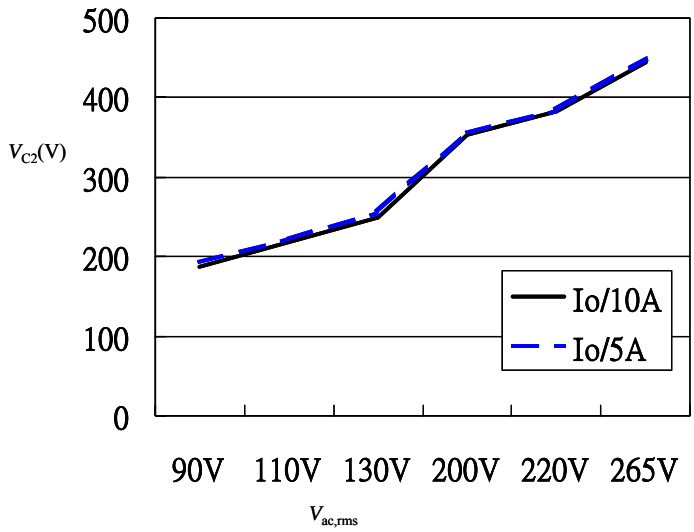


Fig. 5.15 Voltage rating of bulk capacitor and line voltage

5.5 Extension Circuits

The proposed full-bridge converter can deliver high power (up to 5.0KW) to output from input port. When the application doesn't need to deliver so much power and want to save MOSFET, user can employ half-bridge converter in his application. The proposed half-bridge converter is shown as Fig. 5.16.

The additional winding is different from the one in the proposed full-bridge converter, and it has not the center-tap in the winding N_1. Therefore, the voltage stress across S_1 and S_2 are different, and the voltage stress on S_1's will be larger than S_2's. Although the asymmetric operation between switch S_1 and S_2, the input line current can still conform to the standard, IEC61000-3-2 shown in table 5.2. The simulation results are shown in fig. 5.17.

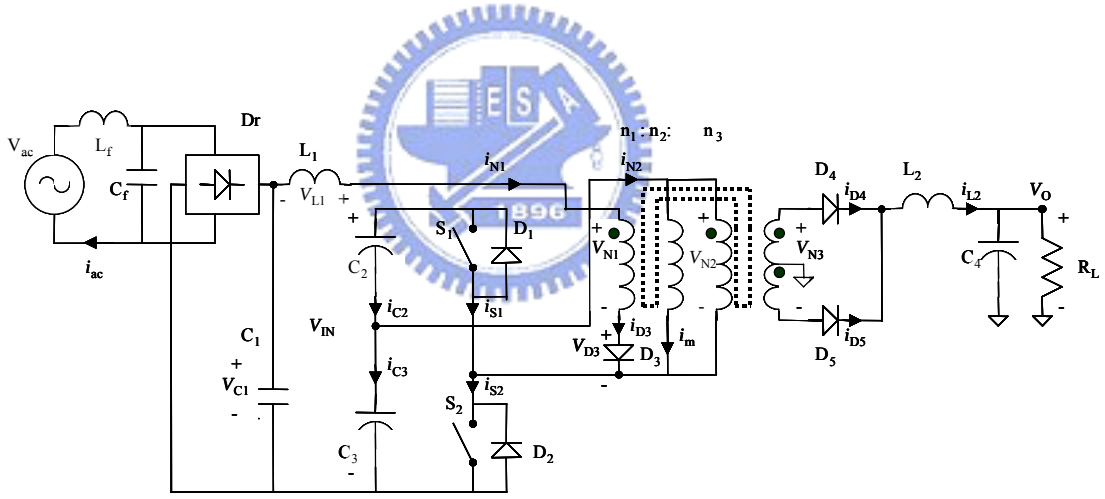


Fig. 5.16 The proposed asymmetric half-bridge converter

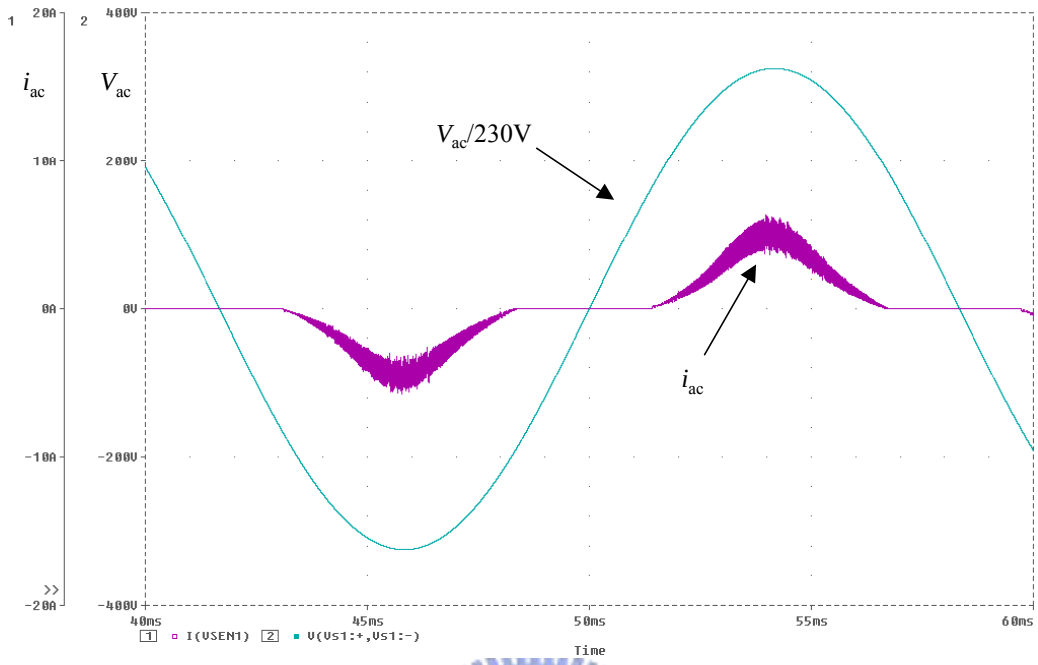


Fig. 5.17 Simulation waveforms in half-bridge converter

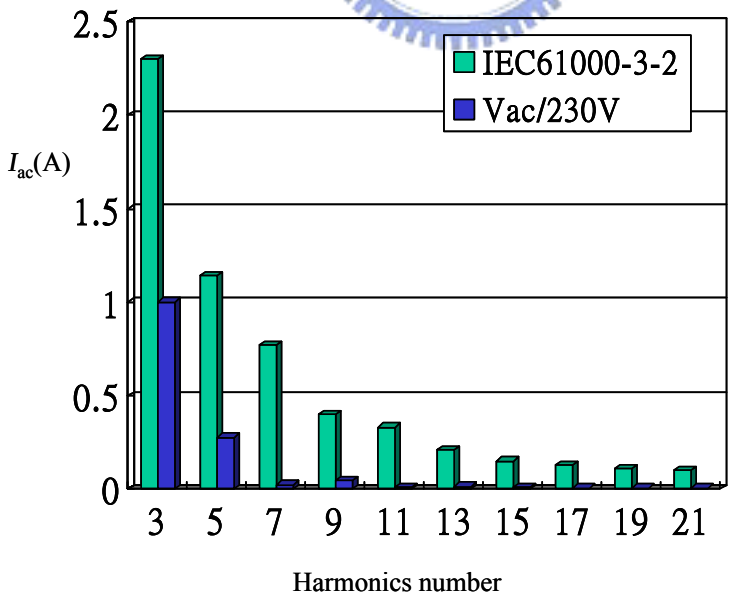


Table. 5.2 The major harmonic components of the line current, P_o=50V • 10A.

The proposed half-bridge converter can save two MOSFETs comparing to the full-bridge converter but the driver circuit for switch S_1 is still inconvenient. A push-pull converter could be another choice. Figure 5.18 is the proposed push-pull converter with input current shaper. The two switch S_1 and S_2 are low side switches so the driver method is simple and easy comparing to half-bridge or full-bridge converters. Besides, the voltage stress across on S1 and S2 are same, and the two switches operation is symmetric. The simulation results are shown in Fig.5.19. Table 5.3 shows the line current harmonics can meet standard IEC61000-3-2 class D.

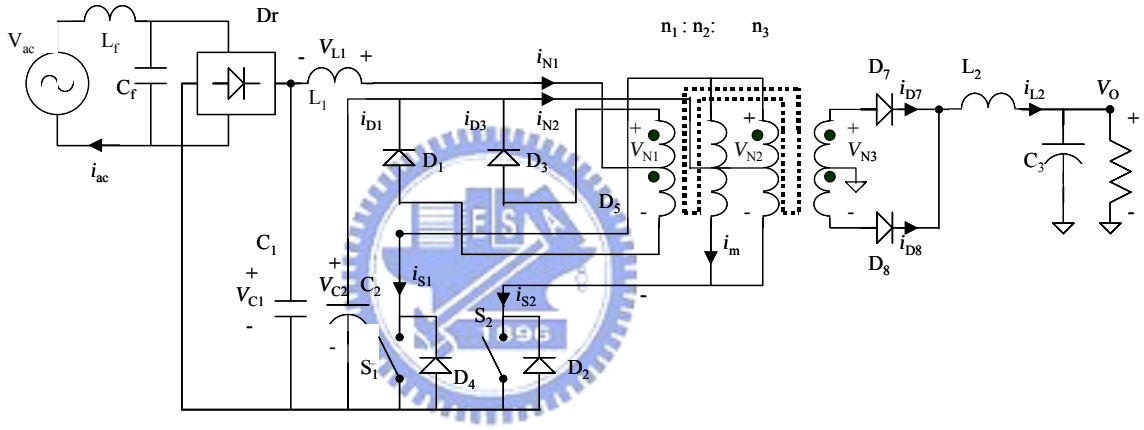


Fig. 5.18 The proposed push-pull converter

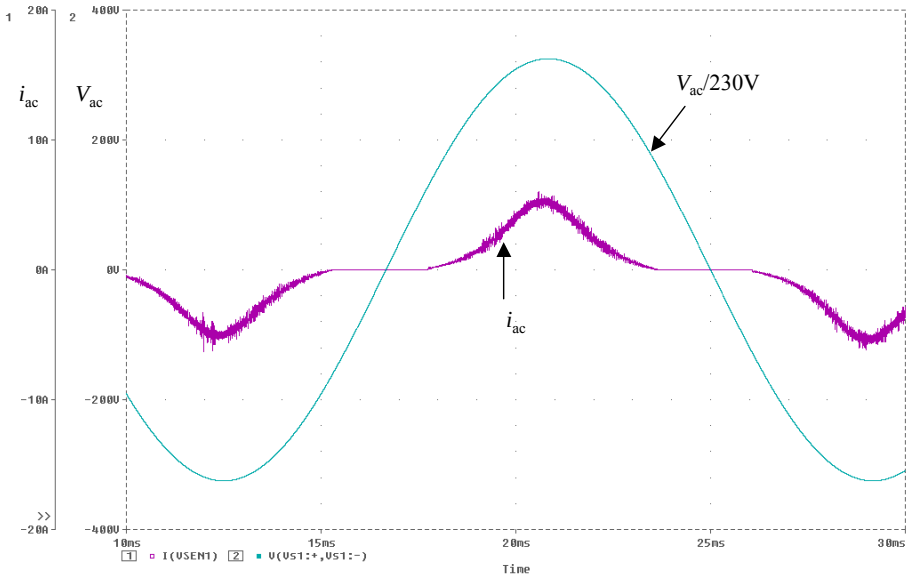


Fig. 5.19 Simulation waveforms in push-pull converter

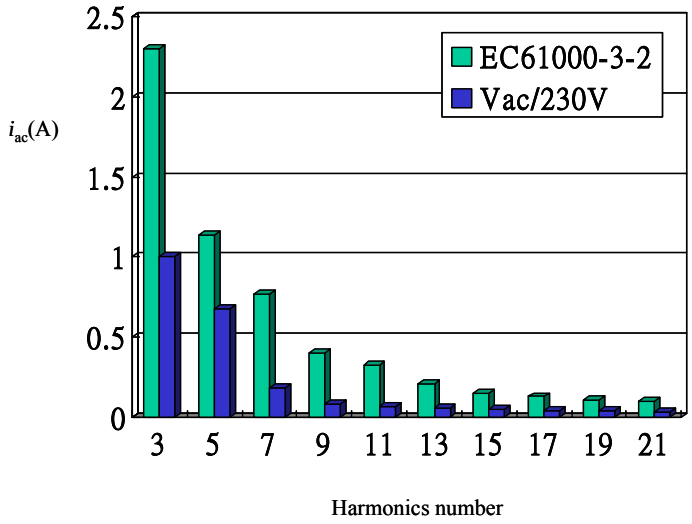


Table 5.3 The major harmonic components of the line current, P_o=50V • 10A, in proposed push-pull converter

CHAPTER 6

SUMMARY and FUTURE RESEARCHES

6.1 Summary

A new family of AC/DC converters with input current shaper is introduced in this dissertation. The proposed converter has the functions of harmonic current correction and fast output voltage regulation. It is implemented in a single-switch single-stage and single control loop fashion. The structure is simple. The main merit is that the magnetic material's volume and weight are reduced to much smaller and lighter than those are in conventional S^4IP^2 converters by employing a two-primary-windings transformer. The employment of additional primary winding is designed to provide a threshold level so that the voltage dropped in input inductor can be decreased. Therefore, the bulk inductor used in the conventional boost-based S^4IP^2 converters is not needed any more in this design. Instead, a small buffer inductor is used in the input loop to constraint the input current. The line current of the proposed converter complies with standard IEC 61000-3-2 and the voltage regulation is tight under load change and has been verified by experiment results. The voltage across bulk capacitor can be held under 450v by adjusting turn-ratio n_1/n_3 in full range operation (85v~265v/ac).

Table 6.1 shows several comparison data. BIFRED and BIBRED have high power factor corrector and high efficiency but their bulk capacitor's voltage tends higher than 450V, and the boost inductor is large in comparing to the proposed circuit. The circuit with magnetic switch has better features, high PFC, high efficiency, and light boost inductor, but the circuit suffers high voltage stress over 450V across bulk capacitor in light load operation. The circuit with magnetic feedback also has better features, light boost inductance and lower bulk voltage, but the harmonics current is higher than the proposed circuit.

Table. 6.1. Comparison table between proposed circuit and prior circuits

Circuits / Features	Proposed Circuit (Flyback)	BIFRED [28]	BIBRED [28]	Magnetic feedback, [10], [11], Fig. 2.7	Magnetic Switch, [33], [34]
PFC	~90%	~95%	~97%	~75%	98%
Power efficiency	~ 75%	~80%	~82%	~70%	82%
dc-bus voltage at V_{ac}=265V	Under 450V, almost load independent	over 450V	over 450V	Under 450V	Over 450V at light load, load dependent
Boost inductance, L_b	None; only smoothing inductor L_1	L_b~1.7L_m*	L_b~L_m/2	L_b~L_m/11	L_b~L_m/12
Operation mode	DCM(Boost cell), CCM(dc/dc)	DCM(Boost cell), CCM(dc/dc)	DCM(Boost cell), CCM(dc/dc)	DCM(Boost cell), CCM(dc/dc)	DCM(Boost cell), DCM(dc/dc)

* L_m: primary winding inductance

The value regarding the inrush current while the proposed circuits turning on, it will depend on the input impedance in the input port of the converters. The test results are shown as followings. Figure 6.1 (a) shows the inrush current in conventional flyback converter without input current shaper. Figure 6.1 (b) shows the inrush current in the proposed flyback converter with input current shaper. The inrush current in the proposed flyback converter has a smaller peak value than the one in conventional flyback converter. The reason is that the input current shaper of the proposed converter has greater input impedance than conventional flyback converter.

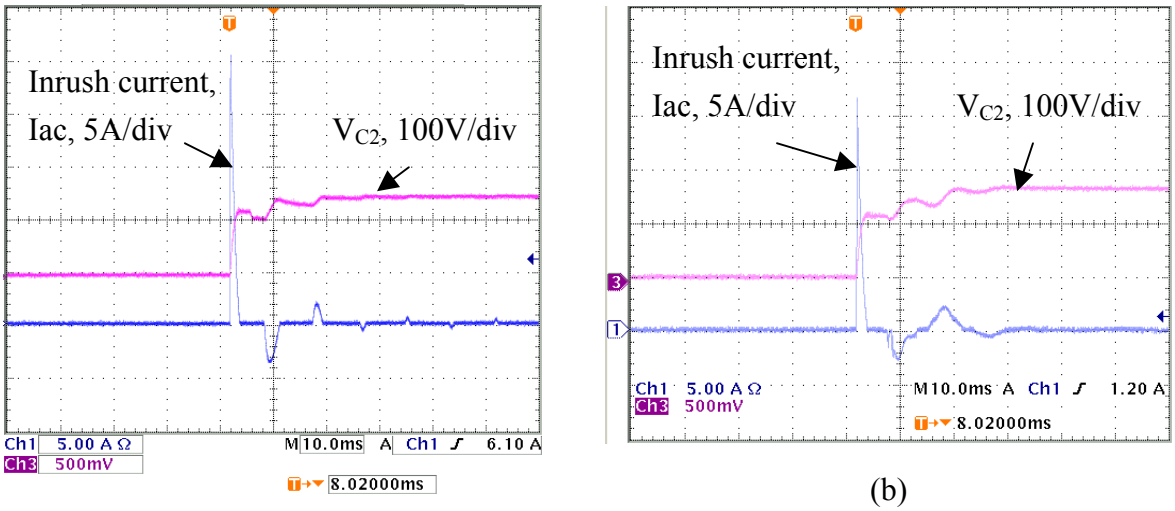


Fig. 6.1 The inrush current of input port while switching on input voltage in (a) conventional flyback converter (b) proposed flyback converter, at Vac=110V.

A reference selection guide for applying the proposed circuits is shown in figure 6.2. In typical application design of flyback converters the power is suggested up to 200W when output voltage is greater than 100V, but the application power is suggested a lower one when the output voltage is smaller than 100V. The output power is suggested between 10W and 200W while the output voltage is in 1V - 100V and the circuits can be flyback or forward converters. However, the maximum output power of forward converters is suggested no greater than 600W.

When output power is greater than 600W, bridge-type or push-pull converters are suggested to use in application. Full-bridge converter can deliver more output power than half-bridge converter or push-pull converter in using the same core size and the same input voltage. Furthermore, full-bridge converter has smaller voltage stress across on switching components in comparing to those in half-bridge and push-pull converters.

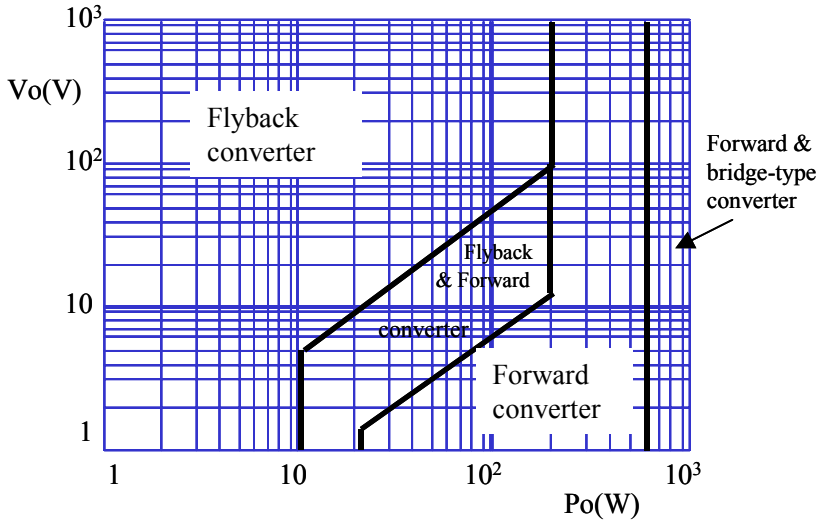


Fig. 6.2 Converter circuit selection as a function of output voltage and throughput power. [41]

6.2 Future Research

Based on the proposed circuits, the suggested future researches are to realize the proposed bridge-type converter, to implement soft-switching technique in these new converters and to improve power flow process in one times transformation from input terminal to output port. Although this research proposes the approach to reduce bulk inductance in boost cell of the boost-type input current shaper, the power efficiency is still not to be satisfied because a part of input power is transferred two times before deliver to output. The part of input power transfers to bulk capacitor via boost cell then the power transfers to output port via dc/dc cell. That is the reason why the power efficiency isn't satisfied.

The proposed flyback converter and forward converter can employ active-clamp technique to implement soft-switching approach [42]-[46]. Besides, the proposed bridge-type converters can employ phase-shift technique to implement zero-voltage-switching approach [47]-[49].

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Vita

Hsing-Fu Liu (M'00) was born in Hsingchu, Taiwan, R.O.C, in 1963. He received the M.S. degree in electrical engineering from Chung Yuan Christian University, Chung-Li, Taiwan, R.O.C., in 1991. He is currently working toward the Ph.D. degree at National Chiao Tung University, Hsingchu, Taiwan, R.O.C. From 1991 to 1995, he was with the Computer and Communications Research Laboratories, Industrial Technology Research Institute, Hsingchu, Taiwan, R.O.C., where his research focused on soft-switching techniques, high-density dc/dc converters, and ac/dc Power-factor-correction circuits. In 1995, he joined Philips Electronics, Chung-Li, Taiwan, R.O.C., as Senior Designer, developing ac/dc and dc/dc power circuits for new model PC monitors. In 1998, he joined Delta Electronics, Chung-Li, Taiwan, R.O.C., where he was involved in developing a switching-mode rectifier for a telecom power system. From 2000 to 2004, he was with Analog Integrations Corporation, Hsingchu, Taiwan, R.O.C., as Manager of the Application Engineering Department. His interests include high-frequency soft-switching techniques, passive and active snubber circuits, ac/dc power-factor-correction circuits, LEDs lighting power, and modeling simulation on power electronics.

姓名: 劉興富

性別: 男

生日: 中華民國 52 年 7 月 25 日

籍貫: 台灣省新竹縣

論文題目: 中文: 新型式單相單級交流轉直流且具有輸入電流修飾的電源轉換器

英文: Novel Single-Phase Single-Stage AC/DC Converters with Input Current Shaper

學歷:

1. 民國 80 年 6 月　　私立中原大學電子工程研究所畢業
2. 民國 94 年 6 月　　國立交通大學電機及控制工程研究所博士班畢業

經歷:

1. 民國 87 年 7 月　　任職台達電子公司研發工程部
2. 民國 89 年 8 月　　任職沛亨半導體公司應用工程部經理
3. 民國 93 年 2 月　　任職聚積科技公司應用工程部資深經理
4. IEEE member and member of IEEE Power Electronics Society since 2000.
5. IEEE APEC Technical Program Committee Member, 19th International Conference on Feb. 22-26, 2004.
6. IEEE PESC Technical Program Committee Member, 36th International Conference on June 12-16, 2005.

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