Timing Jitter and Modulation Profile Extraction for Spread-Spectrum Clocks

Jenchien Hsu and Chauchin Su, *Member, IEEE*

***Abstract*—This paper presents a built-in jitter measurement approach for measuring the timing jitter of spread-spectrum clocks (SSCs) and a jitter estimation method for validating the approach. Because of the lack of dedicated measurement instruments for SSC timing jitter measurement, the jitter estimation method is proposed to correlate SSC and non-SSC jitter. A 1.2-GHz eight-phase SSC generator with the jitter measurement circuit is designed and fabricated using the 0.18-μm complementary metal–oxide–semiconductor technology. The measured results are validated by the proposed estimation method, which is the key contribution of this paper. The experimental results show that the proposed built-in measurement approach has an error of less than 0.0026 UI.**

***Index Terms*—Analog testing, built-in self test, jitter, jitter measurement, phase-locked loop (PLL), spread-spectrum clock (SSCs).**

I. Introduction

ACCURATE jitter measurement for high-speed serial links is extremely challenging. Such a measurement is costly, because it requires instruments with excellent timing accuracy and a long test time to ensure a low bit error rate (BER). To reduce the testing cost, a built-in self test (BIST) is considered a feasible alternative.

Conventionally, BIST circuits use time-to-digital converters (TDCs) to compare the phase difference between a generated clock and reference clock [1]–[7]. The resolution of TDCs determines the accuracy of jitter measurement results. Therefore, self-calibration techniques have been implemented to improve resolution [8], [9]. Unfortunately, a spread-spectrum clock (SSC) has a frequency deviation due to a predefined modulation profile that attenuates the peak power (see Fig. 1). The phase variation of the SSC includes jitter and phase drifting that result from the designed frequency deviation. Separating them by conventional TDC approaches or external instruments is difficult. The phase drifting that was caused by the frequency modulation is deterministic jitter, and the deterministic jitter and random jitter separation algorithm [10] can be used to separate them. However, if the phase drifting is larger than 1UI, the histogram becomes flat and meaningless. It happens for most SSCs. Furthermore, even if deterministic jitter can be separated from random jitter, the SSC phase drifting and deterministic jitter induced by other components of the phase-locked loop (PLL) cannot be separated, because they are all deterministic jitter. Notably, the SSC phase drifting is a low-frequency signal that is not crucial for receivers to recover the data, but other high-frequency deterministic jitter is important; thus, separating different types of deterministic jitter is necessary. The timing jitter of SSCs cannot be measured using traditional approaches; thus, spectrum analyzers are frequently used to measure the power spectrum of SSCs to roughly estimate signal quality. The self-trigger function of oscilloscopes is typically utilized to measure period jitter. However, the period jitter is not useful for estimating BER.

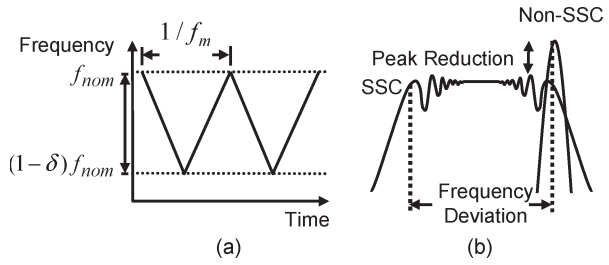


Fig. 1. (a) Modulation profile. (b) PSD of the SSC.

The timing jitter is more appropriate for BER estimation than the period jitter [11]; thus, Serial Advanced Technology Attachment (SATA) develops a timing jitter measurement methodology [12] (see Fig. 2). Jitter is defined as the time difference between a recovered clock and a data edge. The clock recovery circuit has a low-pass transfer function with a corner frequency of $f_{BAUD}/500$ or $f_{BAUD}/1667$, depending on the application, where f_{BAUD} is the nominal rate of data through the channel. However, jitter includes the transmitted jitter and the jitter that was induced by the clock recovery circuit when an ideal recovery circuit is not used. Moreover, an additional clock recovery circuit is needed when using this methodology.

There are two prior arts of BIST circuits for measuring jitter of SSCs [13], [14]. In [13], the modulation profile and period jitter of SSCs were measured. However, the resolution was insufficient, and the period jitter did not comply with the SATA standard. In [14], a BIST methodology for measuring the timing jitter and the modulation profile of SSCs was proposed. However, the BIST methodology was not validated using objective external instruments. In this paper, the measured results are validated by the estimation based on the measured results using external instruments. The estimation methodology is the key contribution of this paper.

The remainder of this paper is organized as follows. Section II presents the BIST methodology. Section III describes

Manuscript received February 12, 2009; revised April 1, 2009. First published September 22, 2009; current version published March 20, 2010. The Associate Editor coordinating the review process for this paper was Dr. Jesús Ureña.

The authors are with the Department of Electrical and Control Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: dennyshu@mail2000.com.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2009.2025992

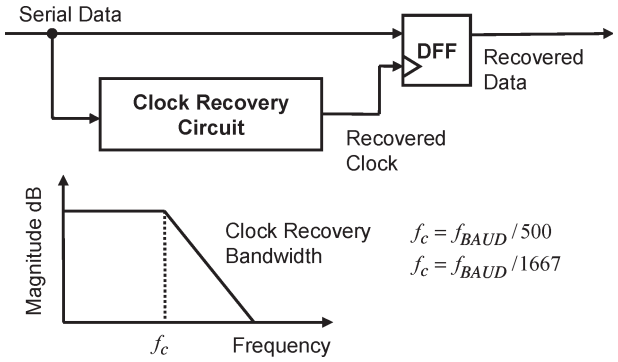


Fig. 2. Jitter measurement methodology.

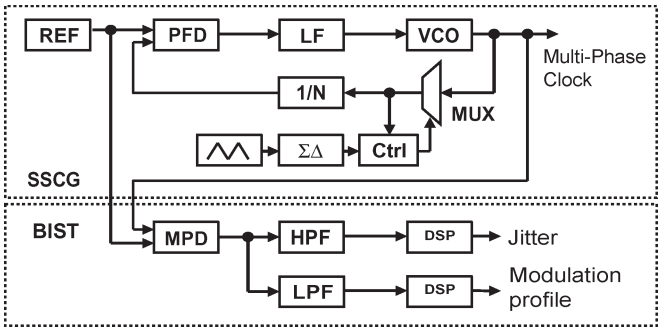


Fig. 3. Proposed BIST methodology.

the jitter estimation method that correlates non-SSC and SSC jitter based on the measurement results of external equipments. In Section IV, chip implementation and measured results are given. Finally, conclusions are drawn in Section V.

II. BIST Methodology Overview

Fig. 3 shows an SSC generator (SSCG) and the proposed BIST methodology. A triangular waveform is generated according to the modulation profile of a 5000-ppm down-spreading and a 30-kHz modulation frequency [see Fig. 1(a)]. The sigma−delta modulator (SDM) is used to control the ten-phase five-stage voltage-controlled oscillator (VCO) such that it oscillates in accordance with the modulation profile.

The BIST module is composed of hardware and software. The hardware comprises a ten-phase multiphase phase detector (MPD) (see Fig. 4). The MPD uses 10-D flip-flops (DFFs) to compare the reference clock to the ten clock phases that were generated by the VCO. The reference clock is used as a triggering signal of the DFFs, and the ten clock phases are the signals being sampled. When the clock edge of the reference clock comes, the ten clock phases are sampled, and the DFFs output a 10-b thermal meter code. The transition bit of the thermal meter code represents the detected phase. The phase-shift detector detects the phase shift by comparing the detected phases at the first and the next triggering times. One example is shown in Fig. 5. Phase 5 is sampled by the first reference clock edge, and Phase 7 is sampled by the next reference clock edge. A phase shift of 0.2 UI is detected. Notably, if the frequency deviation of the SSC is very large, the phase shift may exceed 1 UI. If so, a faster reference clock is needed. When the frequency deviation is 6 MHz (5000 ppm) with a reference

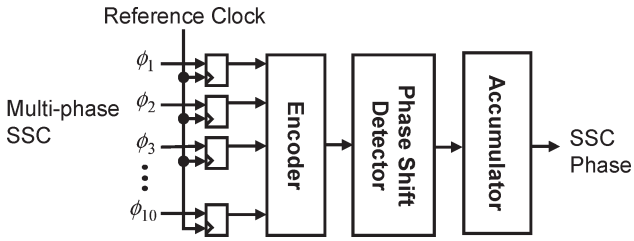


Fig. 4. MPD.

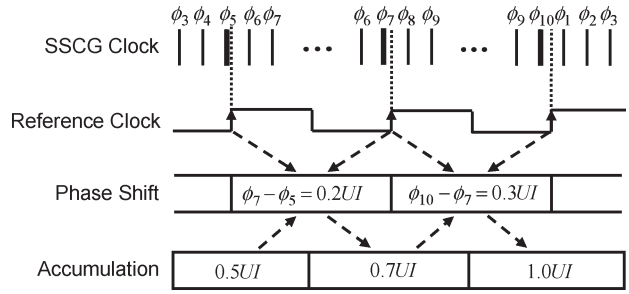


Fig. 5. Timing diagram of the MPD.

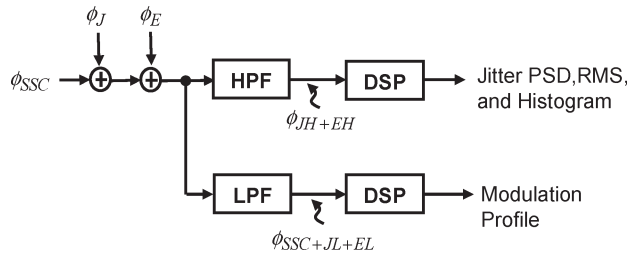


Fig. 6. BIST methodology model.

clock period of 50 ns, the phase shift is 0.3 UI. The next step in phase detection is to accumulate each phase shift to recover the absolute phase. Notably, without jitter, the accumulated phase is the integration of the modulation profile [see Fig. 1(a)]. The modulation profile is the timing diagram of the SSC frequency; thus, the integration of frequency in time is the absolute phase.

The software in the BIST modules comprises a digital signal processing (DSP) program that utilizes the on-chip DSP or microprocessor to extract jitter and the modulation profile after obtaining the accumulated phase using the MPD. Conceptually, the modulation profile can have a frequency that is as low as 30 kHz. Therefore, a low-pass filter (LPF) can extract the modulation profile from the accumulated phase. The high-frequency components of jitter are defined by the SATA standard. Therefore, jitter can be obtained using a high-pass filter (HPF). Notably, additional DSP functions are required to acquire the modulation profile and jitter after filtering. Fig. 6 shows the jitter measurement model, where ϕ_{SSC} is the ideal accumulated phase. Two added noise sources are given as follows: 1) jitter ϕ_J and 2) MPD phase quantization noise ϕ_E. The methodology has two processing paths: 1) the HPF path for jitter measurement and 2) the LPF path for modulation profile extraction.

For jitter measurement, the accumulated phase passes through the HPF. After that, only high-frequency components ϕ_{JH+EH} remain, where JH is the high-frequency jitter and EH is the high-frequency quantization noise. The power spectral density (PSD) function of high-frequency components

$S_{\phi_{JH+EH}}$ can be obtained by taking the square of the fast Fourier transform (FFT) as follows:

$$S_{\phi_{JH+EH}}(f) = FFT^2\left(\phi_{JH+EH}(t)\right). \tag{1}$$

Jitter variance or jitter power is the integration of $S_{\phi_{JH+EH}}$ in the frequency domain. We have

$$\phi^2_{JH+EH,RMS} = \int_{-fref/2}^{fref/2} S_{\phi_{JH+EH}}(f)df \tag{2}$$

where f_{ref} is the reference clock frequency, and RMS is root mean square value. Because f_{ref} is the sampling rate of MPD, the frequency band of the signals within the BIST circuit does not exceed the range of half of f_{ref} based on DSP theories. Jitter and quantization noise are independent random variables; thus, the jitter variance can be obtained by

$$\phi^2_{JH,RMS} = \phi^2_{JH+EH,RMS} - \phi^2_{EH,RMS}. \tag{3}$$

The quantization noise is typically regarded as white noise; thus, its PSD is

$$S_{\phi_E} = \frac{\Delta^2_{MPD}}{12 \cdot f_{ref}}. \tag{4}$$

The transfer function of the HPF is known; thus, $\phi_{EH,RMS}$ is obtained as

$$\phi^2_{EH,RMS} = \int_{-f_{ref}/2}^{f_{ref}/2} |H_{HPF}(j2\pi f)|^2 \cdot S_{\phi_E} df. \tag{5}$$

The modulation profile is extracted using the LPF. After the accumulated phase that passes through the LPF, only the low-frequency component $\phi_{SSC+JL+EL}$ remains, where JL is the low-frequency jitter, and EL is the low-frequency quantization noise. $\phi_{SSC+JL+EL}$ approximates ϕ_{SSC}, because the low-frequency jitter is relatively small. Most of the low-frequency jitter of the VCO is filtered out by the PLL, because the PLL acts like an HPF for VCO noise. Most high-frequency components of quantization noise are filtered out by the LPF. As mentioned, the accumulated phase shift is the integration of the modulation profile in time. Now, by taking the reverse operation, the derivative of $\phi_{SSC+JL+EL}$ generates the modulation profile. We have

$$f(t) = \frac{d\phi_{SSC+JL+EL}(t)}{dt}. \tag{6}$$

Using (1)–(6), the jitter and modulation profile can be extracted from the accumulated phase that was obtained by the MPD.

The next step is to validate the extracted result. Without dedicated SSC timing jitter measurement instruments, verifying that such a methodology can effectively measure SSC jitter is difficult. In Section III, this paper derives an equation that correlates the timing jitter in the SSC and non-SSC modes of the same PLL. In the non-SSC mode, jitter can be measured by external instruments. SSC jitter is estimated using measured results from the non-SSC mode and the derived equation. Thus, this paper can cross check and validate both the BIST methodology and the jitter estimation method.

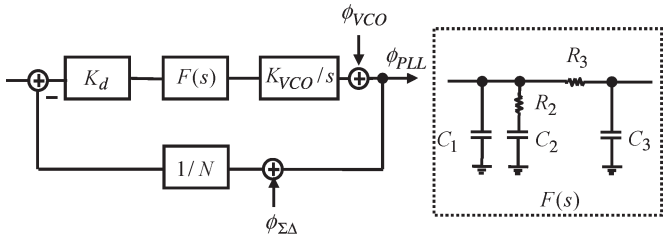


Fig. 7. Noise model of the SSCG.

III. SSC Jitter Estimation

In this section, a jitter estimation method that correlates a non-SSC timing jitter and the corresponding SSC jitter is used to validate the BIST methodology. One equation for SDM noise calculation is also presented for the specific SSCG in this paper.

The SSCG is made by a fractional-N PLL with a triangular modulation profile. Some prior arts have developed the jitter estimation methods for fractional-N PLLs [15], [16]. In these studies, a PLL is modeled as an ideal filter, and a common SDM is used. However, a PLL has a peak in the transfer function, which increases the jitter magnitude. In addition, the SDM in this paper is special such that a common analysis is not applicable. A more accurate model and a dedicated analysis are presented as follows.

Fig. 7 shows the noise model of an SSCG circuit with a third-order loop filter. Based on spectral analysis, the output jitter PSD of the SSCG and noise sources are related as follows:

$$\begin{aligned} S_{\Phi_{PLL}}(f) &= S_{\Phi_{PLL\Sigma\Delta}}(f) + S_{\Phi_{PLLVCO}}(f) \\ &= |H_{\Sigma\Delta}(j2\pi f)|^2 \cdot S_{\Phi_{\Sigma\Delta}}(f) \\ &\quad + |H_{VCO}(j2\pi f)|^2 \cdot S_{\Phi_{VCO}}(f) \end{aligned} \tag{7}$$

where $\mathrm{S}_{\Phi_{PLL}}$ is the PSD of the PLL output jitter. $\mathrm{S}_{\Phi_{PLL}}$ is composed of $S_{\Phi_{PLL\Sigma\Delta}}(f)$ and $\mathrm{S}_{\Phi_{PLLVCO}}(f)$, i.e., the PSDs of the PLL output jitter caused by the noise from the SDM and VCO. In addition, $S_{\Phi_{\Sigma\Delta}}$ and $S_{\Phi_{VCO}}$ are the PSDs of the SDM and VCO noise, respectively, and $H_{\Sigma\Delta}$ and H_{VCO} are the transfer functions from noise sources $\phi_{\Sigma\Delta}$ and ϕ_{VCO} to the PLL output, respectively. With this information, $\mathrm{S}_{\Phi_{PLL}}$ can be derived by (7). The RMS jitter is calculated as

$$\phi^2_{J,RMS} = \int_{-\infty}^{\infty} S_{\Phi_{PLL}}(f)df. \tag{8}$$

The high-frequency RMS jitter is calculated as

$$\phi^2_{JH,RMS} = \int_{-\infty}^{\infty} |H_{HPF}(j2\pi f)|^2 \cdot S_{\phi_{PLL}} df. \tag{9}$$

Next, the derivation and calibration of $S_{\Phi_{\Sigma\Delta}}$, $H_{\Sigma\Delta}(s)$, $S_{\Phi_{VCO}}$, and $H_{VCO}(s)$ are discussed.

A. Derivation of $H_{VCO}(s)$ and $H_{\Sigma\Delta}(s)$

Transfer functions $H_{\Sigma\Delta}(s)$ and $H_{VCO}(s)$ are defined as

$$H_{\Sigma\Delta}(s) = \frac{\phi_{PLL\Sigma\Delta}(s)}{\phi_{\Sigma\Delta}(s)} = -\frac{G(s)}{1+G(s)} \tag{10}$$

$$H_{VCO}(s) = \frac{\phi_{PLLVCO}(s)}{\phi_{VCO}(s)} = \frac{1}{1+G(s)} \tag{11}$$

where $\phi_{PLL\Sigma\Delta}$ and ϕ_{PLLVCO} are the PLL output phases that were caused by the SDM and VCO noise, respectively. The open-loop transfer function $G(s)$ is

$$G(s) = \frac{K_d F(s) K_{VCO}}{sN} \tag{12}$$

where K_d and K_{VCO} are the gains of the phase detector and the VCO, respectively, and N is the division ratio. The transfer function of the loop filter $F(s)$ is defined as

$$F(s) \cong \frac{K_h(s+z_1)}{s\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}. \tag{13}$$

The gain, zero, and poles of the third-order loop filter are

$$K_h = \frac{C_2R_2}{C_1+C_2} \quad z_1 = \frac{1}{C_2R_2}$$
$$p_1 = \frac{C_1+C_2}{C_1C_2R_2} \quad p_2 = \frac{1}{C_3R_3}. \tag{14}$$

$H_{\Sigma\Delta}(s)$ and $H_{VCO}(s)$ deviate from the design target due to the process variation. A proposed calibration flow is used to calibrate the parameters of the transfer functions. First, we assume that all capacitance and resistance values shift in the same ratio under process variation by factors k_1 and k_2, respectively. The values of the poles and the zero proportionally deviate with a factor α, where α is related to k_1 and k_2 as

$$\alpha = \frac{1}{k_1k_2}. \tag{15}$$

The poles and zero can be written as

$$z_1 = \alpha z_{1o} \quad p_1 = \alpha p_{1o} \quad p_2 = \alpha p_{2o} \tag{16}$$

where z_{1o}, p_{1o}, and p_{2o} are the design target. By substituting (13) and (16) into (12) and transforming (12) into the frequency domain, G can be rewritten as

$$\begin{aligned} G &= \frac{K_d F(j2\pi f) K_{VCO}}{j2\pi fN} \\ &= K_o \cdot H_o(\alpha, f) \\ &= F_G(K_0, \alpha, f) \end{aligned} \tag{17}$$

where

$$K_o = \frac{K_d K_{VCO} K_h}{N} \tag{18}$$

and H is the remaining part of G. From this derivation, G is a function of K_o, α, and f. Thus, H_{VCO} is also a function of K_o, α, and f, i.e.,

$$H_{VCO} = F_{H_{VCO}}(K_0, \alpha, f). \tag{19}$$

One can approximately define the natural frequency f_n as the frequency at which the maximum gain of H_{VCO} occurs. The natural frequency f_n is obtained by solving the following equation:

$$\frac{\partial}{\partial f}\left|F_{H_{VCO}}(K_0, \alpha, f)\right| = 0. \tag{20}$$

Based on (19) and (20), f_n is a function of K_0 and α, i.e.,

$$f_n = F_{f_n}(K_0, \alpha). \tag{21}$$

Rearranging (21) shows that constant K_0 is a function of α and f_n, i.e.,

$$K_0 = F_{K_0}(\alpha, f_n). \tag{22}$$

By substituting (22) into (19), H_{VCO} is a function of α, f_n, and f, i.e.,

$$H_{VCO} = F_{H_{VCO}}(\alpha, f_n, f). \tag{23}$$

This relation means that, when the natural frequency and process variation factor α are known, H_{VCO} and $H_{\Sigma\Delta}$ can be derived. f_n and α are obtained using the following method. We assume that the output phase noise of a PLL in the non-SSC mode is dominated by VCO noise and the output phase noise of the PLL and VCO noise are related as follows:

$$S_{\Phi_{PLL},nonSSC} = S_{\Phi_{VCO}}(f) \cdot |H_{VCO}(j2\pi f)|^2 \tag{24}$$

where $\mathrm{S}_{\Phi_{PLL},nonSSC}(f)$ is the PSD of the PLL output jitter in the non-SSC mode. The charge pump current of the phase detector determines the phase detector gain K_d and the values of K_o and f_n in (17) and (21), but the value of α is not affected by the charge pump current. When the charge pump current is changed, the phase noises with different natural frequencies f_{n1} and f_{n2} are produced. Notably, the charge pump current is affected by process variation, and it is difficult to know its exact values. However, knowing the exact values of charge pump current is not necessary. The parameter of the charge pump current is included in the natural frequency, as shown in (21), and the natural frequency can be observed by a spectrum analyzer. It is the same reason that knowing the exact values of other parameters, e.g., the VCO gain, is not necessary. The non-SSC jitter PSD and transfer functions are related as follows:

$$S_{\Phi_{PLL1},nonSSC} = S_{\Phi_{VCO}}(f) \cdot |F_{H_{VCO}}(\alpha, f_{n1}, f)|^2 \tag{25}$$

$$S_{\Phi_{PLL2},nonSSC} = S_{\Phi_{VCO}}(f) \cdot |F_{H_{VCO}}(\alpha, f_{n2}, f)|^2. \tag{26}$$

This paper divides (26) by (25) to eliminate the VCO noise. We have

$$\frac{S_{\Phi_{PLL2},nonSSC}}{S_{\Phi_{PLL1},nonSSC}} = \frac{|F_{H_{VCO}}(\alpha, f_{n2}, f)|^2}{|F_{H_{VCO}}(\alpha, f_{n1}, f)|^2}. \tag{27}$$

The equation is expressed in log scale as follows:

$$\begin{aligned}\Delta S &= 10\log(\mathrm{S}_{\Phi_{PLL2},nonSSC}) \\ &\quad - 10\log(\mathrm{S}_{\Phi_{PLL1},nonSSC}) \\ &= 10\log\left(|F_{H_{VCO}}(\alpha, f_{n2}, f)|^2\right) \\ &\quad - 10log\left(|F_{H_{VCO}}(\alpha, f_{n1}, f)|^2\right) \\ &= \Delta H^2(\alpha, f_{n1}, f_{n2}, f) \end{aligned} \tag{28}$$

where ΔH^2 is the difference between two transfer functions in log scale, and ΔS is the difference between PSDs in log scale measured by a spectrum analyzer. The value of α is calibrated as follows. Using the originally designed charge pump current, f_{n1} is measured. Next, the charge pump current is increased to obtain f_{n2} and ΔS. If f_{n1}, f_{n2}, ΔS, and f are known, α can be calculated using (28). To increase the calibration accuracy, several f_{n2} and ΔS are obtained by again increasing the charge pump current and using a curve-fitting procedure to determine the value of α that best satisfies (28).

B. Derivation of $S_{\Phi_{\Sigma\Delta}}$

Fig. 8 shows the SSCG under test [17]. A ten-phase clock is generated and fed into the multiplexer (MUX). The SDM and MUX select a suitable phase shift according to the frequency deviation determined by the given modulation profile. The division ratio for a 20-MHz reference clock and a 1.2-GHz output clock is 60. The phase shift is 0.1UI, which is confined with the division ratio of 60; thus, the frequency deviation is 0.167%. This value is 33% of the 5000-ppm frequency deviation. Thus, the phase-shift speed must increase by 300%, and the SDM must operate at 300% of the reference clock rate to achieve a 5000-ppm frequency deviation. The data rate of the SDM is 300% of the frequency of the reference clock and the divider output; thus, three consecutive data of SDM are summed in one reference clock period. The equivalent output of the SDM is the sum of three consecutive data of the original SDM.

The output signal of the SDM is denoted as $x[n]$, and the sum of three consecutive data is

$$y[k] = x[3k-2] + x[3k-1] + x[3k]. \tag{29}$$

It can be regarded as a three-time downsampling of the moving sum $x'[n]$, i.e.,

$$x'[n] = x[n-2] + x[n-1] + x[n]. \tag{30}$$

The PSD of the noise at the output of a MASH-111 SDM is

$$S_{QE}(z) = \left|(1-z^{-1})^3\right|^2 \cdot S_E \tag{31}$$

where S_E is the quantization noise in the SDM with the following probability density function:

$$S_E = \frac{\Delta^2}{12 f_s} \tag{32}$$

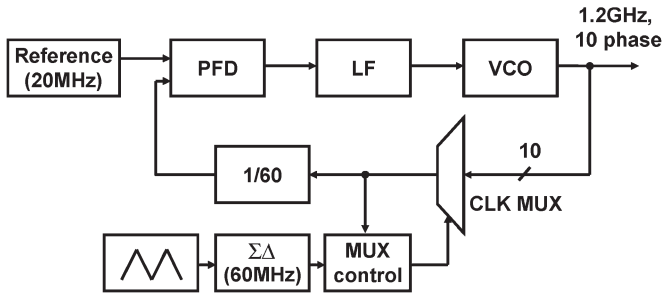


Fig. 8. The SSCG structure with multiphase selection.

where Δ is 1 least significant bit of the quantizer or 0.1 UI for a ten-phase MUX; f_s is 300% of the reference clock rate. We have

$$f_s = 3 f_{ref}. \tag{33}$$

In addition, (31) is transformed into the frequency domain as

$$S_{QE}(f) = \Delta^2 \frac{16}{3 f_s} \sin^6\left(\frac{\pi f}{f_s}\right). \tag{34}$$

The PSD of the moving sum is

$$S_{QE1}(z) = |1 + z^{-1} + z^{-2}|^2 \cdot S_{QE}(z). \tag{35}$$

The PSD of the moving sum is transformed into the frequency domain as

$$S_{QE1}(f) = \left(3 + 4\cos\left(\frac{2\pi f}{f_s}\right) + 2\cos\left(\frac{4\pi f}{f_s}\right)\right) \cdot S_{QE}(f). \tag{36}$$

After downsampling thrice, the PSD of $y[k]$ is

$$\begin{aligned} S_{QE2}(f) &= S_{QE1}(f) + S_{QE1}\left(f + \frac{f_s}{3}\right) \\ &\quad + S_{QE1}\left(f + \frac{2 \cdot f_s}{3}\right). \end{aligned} \tag{37}$$

The PSD of the equivalent noise at the divider input is calculated as

$$S_{\Phi_{\Sigma\Delta}}(z) = \left|\frac{1}{1-z^{-1}}\right|^2 \cdot S_{QE2}(z). \tag{38}$$

The PSD of the equivalent noise at the divider input is transformed into the frequency domain as

$$S_{\Phi_{\Sigma\Delta}}(f) = \frac{1}{4\sin^2\left(\frac{\pi f}{f_{ref}}\right)} \cdot S_{QE2}(f). \tag{39}$$

C. Derivation of $S_{\Phi_{VCO}}$

The next step is to estimate the VCO noise. We assume that the PSD of the VCO noise is

$$S_{\Phi_{VCO}}(f) = \frac{A_{VCO}}{f^2}. \tag{40}$$

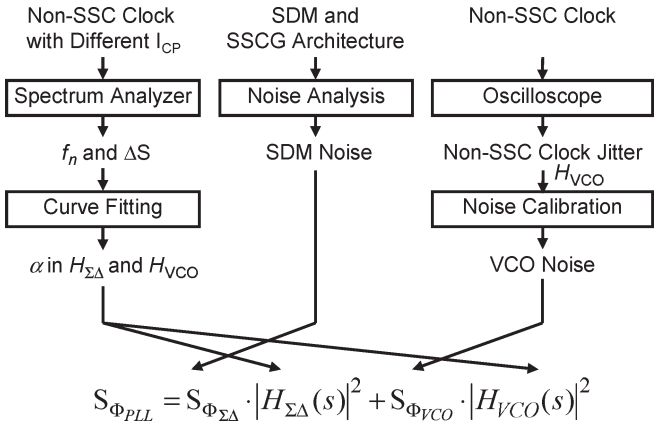


Fig. 9. Jitter estimation and calibration flow.

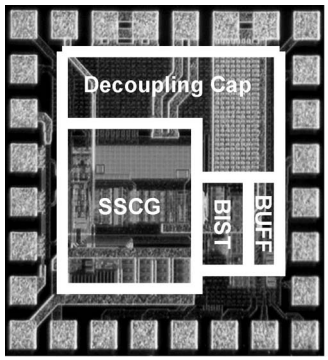
The jitter of the non-SSC and the PSD of the VCO noise are related as follows:

$$\phi^2_{\mathrm{JnonSSC,RMS}} = \int_{-\infty}^{\infty} |H_{VCO}(j2\pi f)|^2 \cdot S_{\Phi_{VCO}}(f) df = \int_{-\infty}^{\infty} |H_{VCO}(j2\pi f)|^2 \cdot \frac{A_{VCO}}{f^2} df. \quad (41)$$

After measuring the RMS jitter of the non-SSC, $\phi_{\mathrm{JnonSSC,RMS}}$, A_{VCO} can be obtained by (41).

Fig. 9 shows the jitter estimation and the calibration flow. First, the phase noise of the non-SSC is measured, and the natural frequency and peak values at the natural frequency are observed from the phase noise diagrams. Then, the charge pump current is increased, and the phase noise is again measured to identify another natural frequency and the peak value. Using these measured parameters and (28), α, which represents pole/zero deviations due to process variation, is calibrated. To increase the estimation accuracy, this step can be repeated several times for the curve-fitting procedure. The SDM noise is theoretically obtained. The RMS jitter of the non-SSC is measured by an oscilloscope, and (41) is applied to obtain the PSD of the VCO noise. After all the parameters are acquired, (7) is used to calculate the jitter PSD and its RMS value.

Fig. 10 presents a chip photograph of this paper and its summary. The technology used is a 0.18-μm complementary metal–oxide–semiconductor (CMOS) with a supply voltage of 1.8 V. The BIST circuit area is 15% of the SSCG, which includes the DFFs and phase-shift detector of the MPD but does not include the accumulator or other digital circuits. The BIST is operated at 20 MHz, which is the same as the reference clock frequency. The SSCG is a fractional-N PLL with a ten-phase 1.2-GHz VCO, a third-order loop filter, and a MASH-111 SDM to meet the SATA-III specification. In total, 10^4 data outputs by the phase-shift detector are recorded by a logic analyzer. A personal computer is used for digital signal processing. The SSC and non-SSC are measured using a spectrum analyzer and oscilloscope.



Technology	0.18 µm
Supply Voltage	1.8V
BIST Power Consumption	1.28mW
SSCG Power Consumption	86.45mW
BIST Area	150µmx250µm (15%)
SSCG Area	500µmx500µm
BIST clock	20MHz
SSCG clock	1.2GHz,10phase

Fig. 10. Chip photograph.

IV. Experimental and Measurement Results

Fig. 11 shows the power spectrums measured using a spectrum analyzer of a non-SSC and an SSC. Measured results indicate that the non-SSC has a frequency of 1.2 GHz and the SSC has a maximum frequency deviation of 6 MHz (5000 ppm) from a nominal frequency of 1.2 GHz.

Fig. 12 shows the phase-shift detector outputs. As expected, a 6-MHz frequency deviation in a 50-ns reference clock period causes a maximum phase shift of 0.3 UI. With noise, an additional phase shift of 0.1 UI can be generated. Fig. 13 shows the accumulated phase, which includes the ideal SSC phase drifting, phase quantization noise that was produced by the MPD, and jitter. The MPD output is passed through the digital filters and DSPs for further analysis. Fig. 14 shows the SSC modulation profile of the SSC obtained using a fifth-order infinite impulse response (IIR) LPF with a corner frequency of 500 kHz. The corner frequency is selected to filter out as much noise as possible to retrieve the SSC phase and its harmonics. The measurement results for the BIST show that the frequency deviation is 6.1 MHz, which is in agreement with the value that was measured by the oscilloscope (see Fig. 11). The modulation frequency is 29.4 kHz compared with the design target of 29.3 kHz.

The calibration process is explained as follows. First, the phase noise of the non-SSC of the PLL is measured. Second, the charge pump current is increased, and the phase noise is again measured. The natural frequencies are observed from these two phase noise diagrams. Fig. 15 shows the phase noise of the non-SSCs with natural frequencies of 0.4 MHz (f_{n1}) and 0.9 MHz (f_{n2}), as defined in (28). The frequency f is chosen to equal f_{n2}. Comparing the phase noise at 0.9 MHz (f_{n2}), the difference in phase noise ΔS is 2 dB. For the curve-fitting procedure, one should repeat this step several times with different charge pump currents. Fig. 16 shows the case with an f_{n2} of 2.2 MHz. In this case, ΔS is 18 dB at 2.2 MHz.

Fig. 17 shows the curve-fitting procedure; the y-axis is ΔH^2, and the x-axis is the natural frequency f_{n2}. In addition, f_{n1} is fixed at 0.4 MHz, and the f chosen is f_{n2}. Curves with different values of α are shown. The most appropriate value of α is 0.85 in this case. The calibration of the VCO noise is presented as follows. Fig. 18 shows the non-SSC jitter with a natural frequency of 0.4 MHz, which is measured by the oscilloscope. The measured RMS jitter is 12.59 ps; thus, A_{VCO} in the PSD of the VCO noise is estimated as 24 (UI^2/Hz) in (40). The

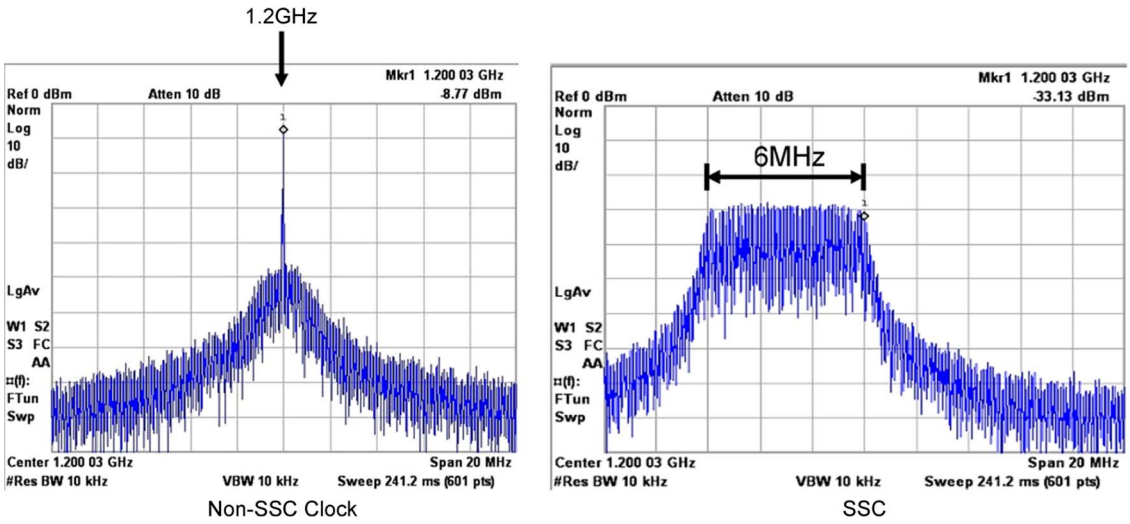


Fig. 11. PSD of the non-SSC clock and SSC measured using a spectrum analyzer.

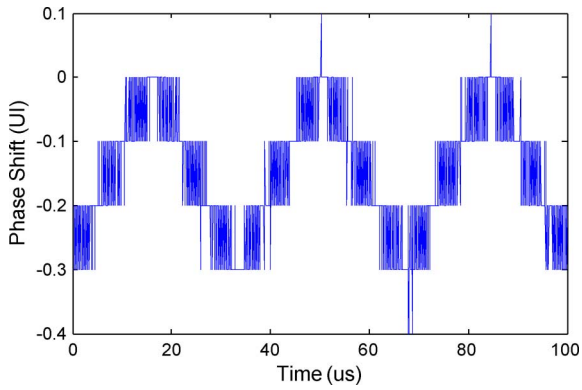


Fig. 12. Phase-shift detector output signal.

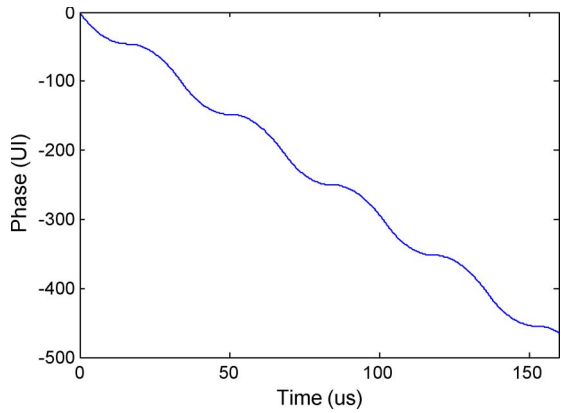


Fig. 13. Accumulator output signal.

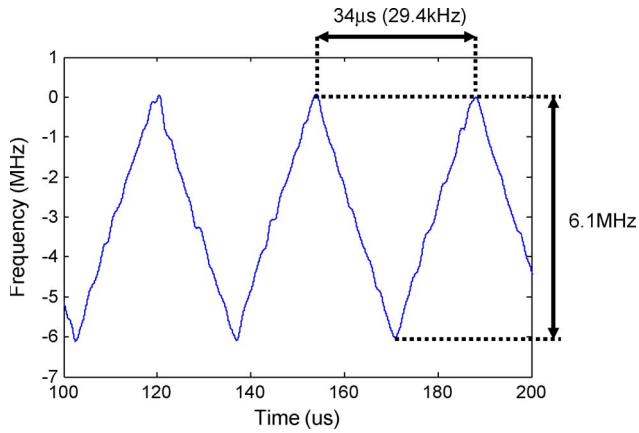


Fig. 14. Modulation profile of the SSCG.

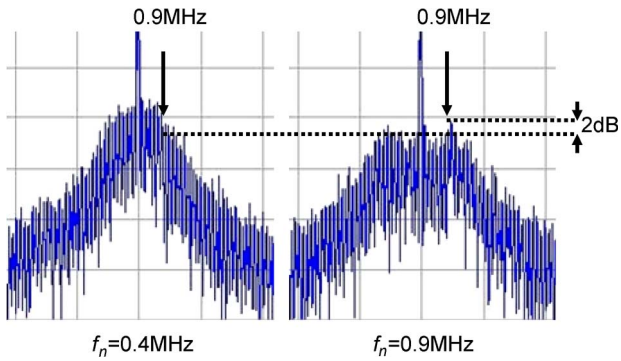


Fig. 15. Phase noise of non-SSC clocks with natural frequencies of 0.4 and 0.9 MHz.

SDM noise is also analyzed using (29)–(39). The SSC has ten phases; the frequency of the reference clock is 20 MHz, and the frequency of the SDM is 60 MHz. Fig. 19 shows the estimated $S_{\Phi_E}(f)$, $S_{\Phi_{PLLVCO}}(f)$, and $S_{\Phi_{PLL\Sigma\Delta}}(f)$. Each line represents the PSD of the jitter with different charge pump currents. The natural frequencies in this figure are 0.1–2.3 MHz. Notably, the optimal bandwidth of the PLL is 0.2 MHz in this paper. If the bandwidths exceed the optimal bandwidth, jitter increases as natural frequency increases.

Figs. 20–22 show the estimated and measured values of PSDs of the HPF output signal $S_{\Phi_{JH+EH}}(f)$ in (1) for different natural frequencies. The estimated jitters (thick lines) are the sum of the PSD of the SDM noise, VCO noise, and quantization noise (thin lines). The measurement results are acquired from the HPF outputs. A fifth-order IIR HPF with a corner frequency of 500 kHz is utilized. The corner frequency of 500 kHz is chosen to filter out most of the SSC 30-kHz phase drifting and its harmonics caused by the frequency modulation. Using

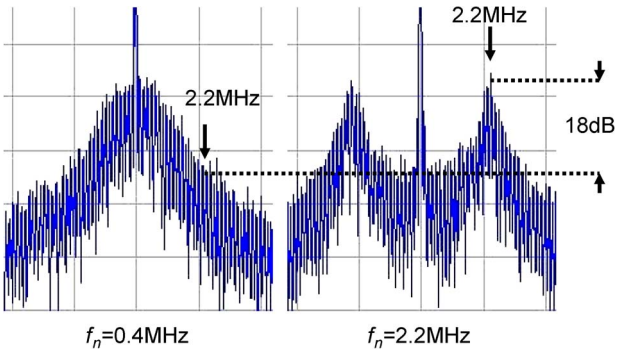


Fig. 16. Phase noise of non-SSC clocks with natural frequencies of 0.4 and 2.2 MHz.

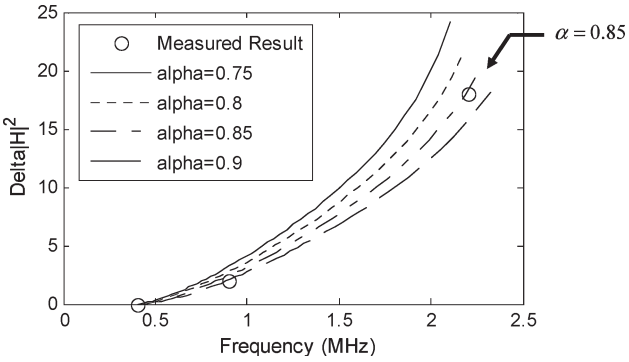


Fig. 17. Curve-fitting procedure for the calibration of transfer functions.

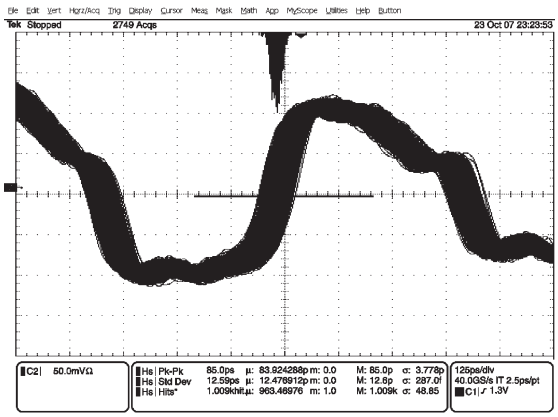


Fig. 18. Non-SSC jitter with a natural frequency of 400 kHz.

calculation tools, it is estimated that a 500-kHz fifth-order HPF can filter out most of the unwanted SSC phase drifting with a modulation frequency of 30 kHz. The unfiltered phase drifting is 0.003 UI (RMS), which causes a 1% error when the jitter being measured is, for example, 0.02 UI (RMS). If the corner frequency is decreased to 400 kHz, the error increases to 4%. Therefore, a corner frequency of 500 kHz is chosen if an error below 1% is required. The BIST results of the SSCs are in good agreement with the estimated results based on the phase noise of the non-SSC measured by a spectrum analyzer (see Figs. 15 and 16) and the RMS jitter measured by an oscilloscope (Fig. 18).

Fig. 23 shows the histogram of the jitter plus high-frequency phase quantization noise calculated based on the HPF output.

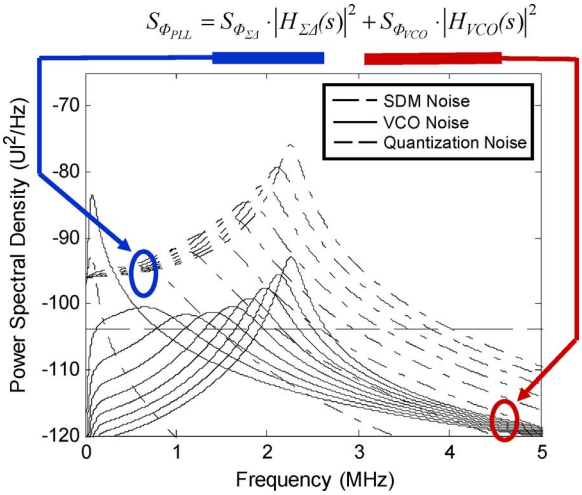


Fig. 19. Theoretical PSDs of the jitter and phase quantization noise.

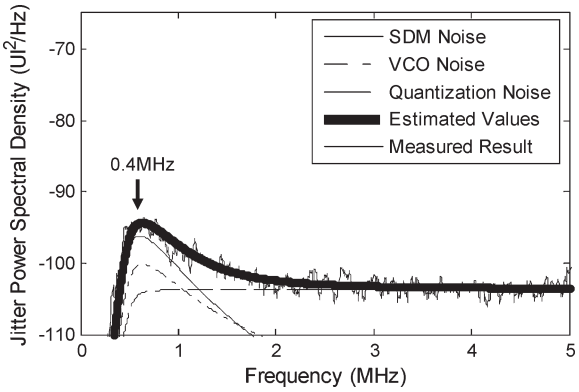


Fig. 20. Theoretical and measured PSDs of jitters ($f_n = 0.4$ MHz).

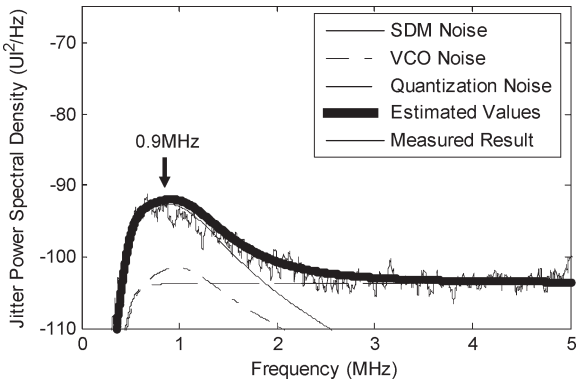


Fig. 21. Theoretical and measured PSDs of jitters ($f_n = 0.9$ MHz).

The RMS jitter can statistically be obtained from the histogram. For experimental purposes, a fifth-order HPF with a corner frequency of 500 kHz and a third-order HPF with a corner frequency of 3.6 MHz are used. The latter HPF complies with the SATA standard, which requires $f_{BAUD}/1667$, where f_{BAUD} is 6 Gbps. Fig. 24 shows the BIST and estimation results. Table I lists the BIST and estimation result for the 3.6-MHz case, which complies with the SATA standard. The maximal error is 0.026 UI. Such errors are systematic errors, because all measured results exceed the estimated ones. This result may be due to the phase imbalance of the multiphase

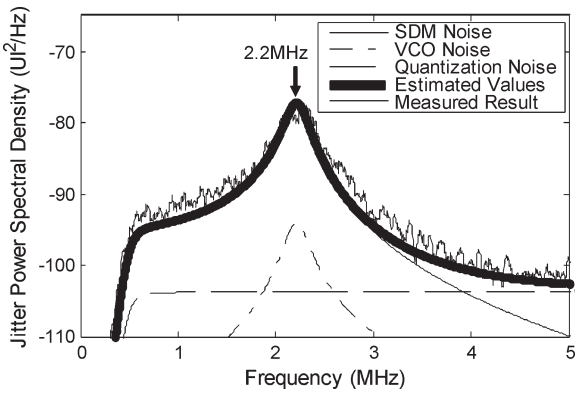


Fig. 22. Theoretical and measured PSDs of jitters ($f_n = 2.2$ MHz).

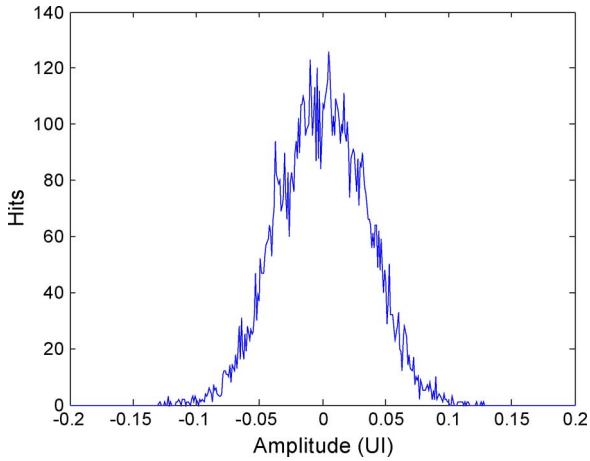


Fig. 23. Jitter histogram measured by BIST ($f_n = 0.4$ MHz).

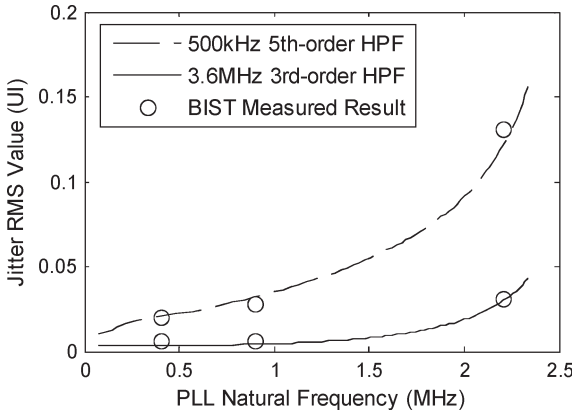


Fig. 24. Jitter RMS value: BIST versus estimation results.

clock. Such an imbalance generated additional phase noise at the MPD output. Notably, the estimation result is based on the non-SSC, which does not involve the multiphase clock. If phase imbalance is considered, (3) can be modified as

$$\phi^2_{JH,RMS} = \phi^2_{JH+EH+PIM,RMS} - \phi^2_{EH,RMS} - \phi^2_{PIM,RMS} \tag{42}$$

where ϕ_{PIM} is the phase imbalance noise, and PIM is the phase imbalance. Comparing the estimation and BIST results and using linear regression to estimate the unknown term ϕ_{PIM}, the phase imbalance noise is likely to be 0.0053 UI. However, this noise cannot individually be tested or calibrated; thus, the phase imbalance noise puts a limit to the measurement range of this BIST approach.

TABLE I
COMPARISON OF MEASURED RMS JITTER AND ESTIMATED VALUES THAT MEET THE SATA STANDARD

PLL Natural Frequency	Estimation	BIST	Error
0.4 MHz	0.0034 UI	0.0060 UI	0.0026 UI
0.9 MHz	0.0042 UI	0.0067 UI	0.0025 UI
2.2 MHz	0.0298 UI	0.0315 UI	0.0017 UI

V. CONCLUSION

This paper has presented the feasibility of a built-in jitter measurement method for multiphase SSCGs. This method is based on a ten-phase MPD and DSP algorithms for extracting the jitter histogram and PSD, with the timing jitter definition complying with the SATA standard. The method for measuring the modulation profile, which includes modulation frequency and frequency deviation, is also presented. The jitter estimation method that correlates SSC jitter and non-SSC jitter is used to validate the jitter measurement methodology. A 1.2-GHz ten-phase SSC PLL with the proposed jitter measurement circuit was designed and implemented using the 0.18-μm CMOS technology. Measurement results show that the errors of the estimation and BIST results are less than 0.0026 UI.

REFERENCES

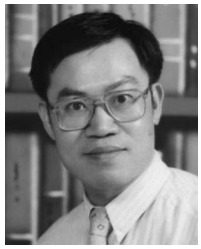
[1] S. Sunter and A. Roy, "BIST for phase-locked loops in digital application," in *Proc. Int. Test Conf.*, 1999, pp. 532–540.
[2] N. Abaskharoun and G. W. Roberts, "Circuits for on-chip subnanosecond signal capture and characterization," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2001, pp. 251–254.
[3] S. Cherubal and A. Chatterjee, "A high-resolution jitter measurement technique using ADC sampling," in *Proc. Int. Test Conf.*, 2001, pp. 838–847.
[4] T. Xia and J. C. Lo, "Time-to-voltage converter for on-chip jitter measurement," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 6, pp. 1738–1748, Dec. 2003.
[5] J. M. Cazeaux, M. Omana, and C. Metra, "Novel on-chip circuit for jitter testing in high-speed PLLs," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 5, pp. 1779–1788, Oct. 2005.
[6] K. Ichiyama, M. Ishida, T. J. Yamaguchi, and M. Soma, "Data jitter measurement using a delta-time-to-voltage converter method," in *Proc. Int. Test Conf.*, 2007, pp. 1–7.
[7] J. Hsu and C. Su, "BIST for measuring clock jitter of charge-pump phase-locked loops," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 2, pp. 276–285, Feb. 2008.
[8] B. Nelson and M. Soma, "On-chip calibration technique for delay-line-based BIST jitter measurement," in *Proc. Int. Symp. Circuits Syst.*, 2004, pp. 944–947.
[9] J. Rivoir, "Fully digital time-to-digital converter for ATE with autonomous calibration," in *Proc. Int. Test Conf.*, 2006, pp. 1–10.
[10] Y. Cai, S. A. Werner, G. J. Olsen, and R. D. Brink, "Jitter testing for multigigabit backplane SerDes," in *Proc. Int. Test Conf.*, 2002, pp. 1–10.
[11] D. Hong, C. K. Ong, and K. T. Cheng, "Bit-error-rate estimation for high-speed serial links," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 53, no. 12, pp. 2616–2627, Dec. 2006.
[12] *Serial ATA Revision 2.5*, Serial ATA Int. Org., Beaverton, OR, Oct. 2005.
[13] M. Chou, J. Hsu, and C. Su, "A digital BIST methodology for spread-spectrum clock generators," in *Proc. Asian Test Symp.*, 2006, pp. 251–254.
[14] J. Hsu, M. Chou, and C. Su, "Built-in jitter measurement methodology for spread-spectrum clock generators," in *Proc. IEEE Int. Symp. VLSI Des., Autom. Test*, 2008, pp. 67–72.

[15] W. Rhee, B. S. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order $\Delta\Sigma$ modulator," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1453–1460, Oct. 2000.

[16] B. De Muer and M. S. J. Steyaert, "On the analysis of $\Delta\Sigma$ fractional-N frequency synthesizers for high-spectral purity," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 784–793, Nov. 2003.

[17] H. Lee, O. Kim, G. Ahn, and D. Jeong, "A low-jitter 5000-ppm spread-spectrum clock generator for multichannel SATA transceiver in 0.18/spl mu/m CMOS," in *Proc. Int. Solid State Circuits Conf.*, 2005, p. 162.

Jenchien Hsu received the B.S. and M.S. degrees in electronic engineering from the National Central University, Chung-Li, Taiwan, in 2000 and 2003, respectively. He is currently working toward the Ph.D. degree, with a specialization in mixed-signal testing, in the Department of Electrical and Control Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan.



Chauchin Su (M'90) received the B.S. and M.S. degrees in electrical engineering from the National Chiao-Tung University, Hsin-Chu, Taiwan, in 1979 and 1981, respectively. He received the Ph.D. degree in electrical and computer engineering from the University of Wisconsin, Madison, in 1990.

He is currently with the Department of Electrical and Control Engineering, National Chiao-Tung University. His research interests include mixed analog and digital system testing and design for testability. He is also involved in projects on base-band and circuit design for wireless communications.