# Origins of Performance Enhancement in Independent Double-Gated Poly-Si Nanowire Devices

Hsing-Hui Hsu, Horng-Chih Lin, *Senior Member, IEEE*, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—In this paper, we characterize and compare the characteristics of a poly-Si nanowire (NW) device with independent double-gated configuration under different operation modes. In the device, the tiny NW channels are surrounded by an inverted-T-shaped gate and a top gate. It is found that the device under double-gate (DG) mode exhibits significantly better performance with respect to the two single-gate (SG) modes, as indicated by a higher current drive than the combined sum of the two SG modes and a smaller subthreshold swing of less than 100 mV/dec. Origins of such improvement have been identified to be due to the elimination of the back-gate effect as well as an enhancement in the effective mobility with the DG operation.**

***Index Terms*—Double gate (DG), mobility, nanowire (NW), poly-Si, thin-film transistor (TFT).**

## I. Introduction

Si NANOWIRE (NW)-based device technology has recently received considerable attention and has been widely exploited for various applications in nanoelectronics. The NW structure features a high surface-to-volume ratio, making it extremely sensitive to the variation of surface conditions and suitable for a number of device applications, including NW field-effect transistors (FETs) [1], nonvolatile memories [2], and sensors [3]. Preparations of NW structures can be categorized into bottom-up [4], [5] and top-down [6], [7] approaches. The former approach is flexible in preparing the NW composition and structure but lacks the controllability over precise positioning and alignment of NW patterns and is therefore not suitable for manufacturing. On the other hand, top-down methods typically employ advanced but costly lithography tools like e-beam or deep ultraviolet steppers to generate the NW patterns. To address these issues, we have recently proposed and developed a simple NW FET fabrication method by taking advantage of the sidewall spacer etching technique to form poly-Si NWs serving as the device channel and have demonstrated that most advantages pertaining to the NW structure could be retained with the new scheme [8], [9]. One major concern associated with the proposed devices is the use of poly-Si NWs as channels. Defects contained in the poly-Si material are known to hinder carrier transport and lead to degradation in device's current drive. This concern may be relaxed with multiple-gate configuration, which can increase the gate controllability over the channel and potentially improve the device performance [10].

In this paper, we investigate the characteristics of inverted-T DG NW FETs with ultrathin body that were developed recently by our group [11]. In this scheme, the tiny NW channels are surrounded by an inverted-T gate and a top gate. Since the two gates can be biased independently, more freedom is allowed for device operation. For example, a specified voltage can be applied to one of the gates for modulation of the threshold voltage ($V_{\rm TH}$) of the transfer curve driven by the other gate [11]–[13]. Due to the strong coupling between two separate gates, $V_{\rm TH}$ can be widely modulated with independent gate control scheme. This phenomenon is called "back-gate effect" in independent double-gated silicon-on-insulator (SOI) metal–oxide–semiconductor transistors [12], [13]. Impacts of such effect on the NW device performance operated with various modes are examined in this work.

## II. Device Structures and Fabrication

Fig. 1 shows the fabrication and structure of the NWFET devices characterized in this study. Process flow of the device fabrication was detailed in our previous work [11]. In short, the inverted-T-shaped gate was formed by applying twice the lithography/etching processes. After the deposition of an oxide layer serving as the gate dielectric of the inverted-T gate, deposition of a Si layer and source/drain (S/D) doping with phosphorous ion implantation were executed. The poly-Si NW channels and S/D regions were subsequently formed using anisotropic plasma etching. This way, the two NW channels were precisely positioned on the upper stud of the inverted-T gate (denoted as G1) in a self-aligned manner. The NW channels were further capped with another gate oxide and the top $n^+$ poly-Si gate (G2). A transmission electron microscopic (TEM) picture of a device is also shown as an inset in Fig. 1. From the picture, gate oxides of G1 and G2 are both 18.5 nm, and peripheral lengths of the NW channel cross section abutting against G1 and G2 are 45 and 40 nm, respectively. The NW channel is almost completely surrounded by G1 and G2, ensuring excellent gate coupling during operation. For comparison purposes, planar double-gated thin-film transistors (TFTs) with symmetrical gate oxide of 20 nm and poly-Si channel of 50 nm were also fabricated and characterized.

Manuscript received September 17, 2009; revised January 6, 2010. First published March 1, 2010; current version published April 2, 2010. This work was supported in part by the National Science Council under Contract NSC 96-2221-E-009-212-MY3. The review of this paper was arranged by Editor M. Reed.

The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hclin@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2010.2041857

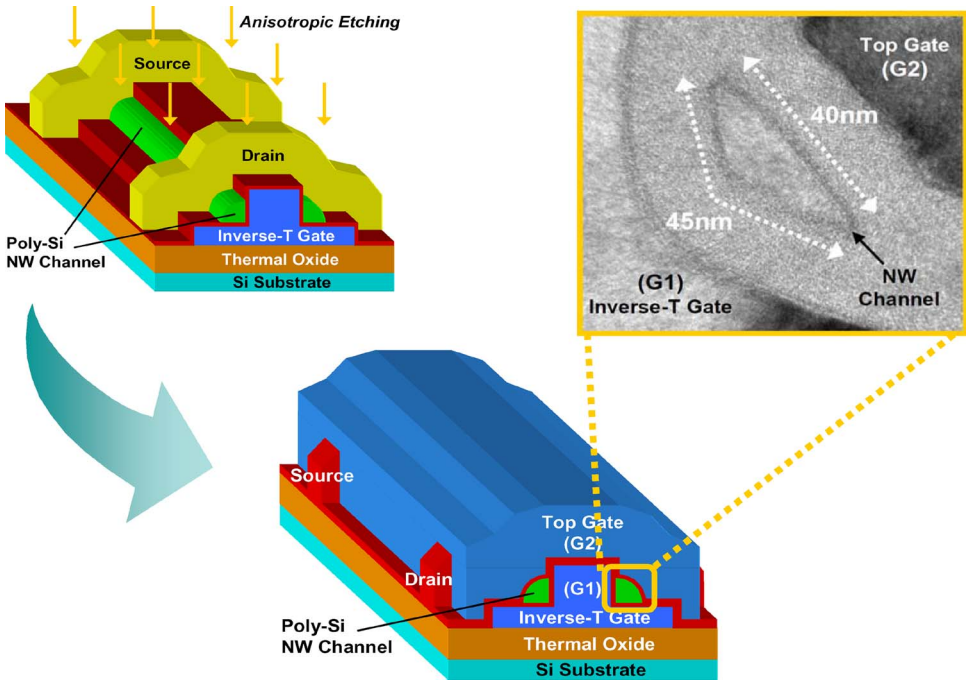



Fig. 1. Key fabrication steps and schematic 3-D structure of the DG NW FET device. Inset TEM picture shows the cross section profile and dimensions of the fabricated NW channel.

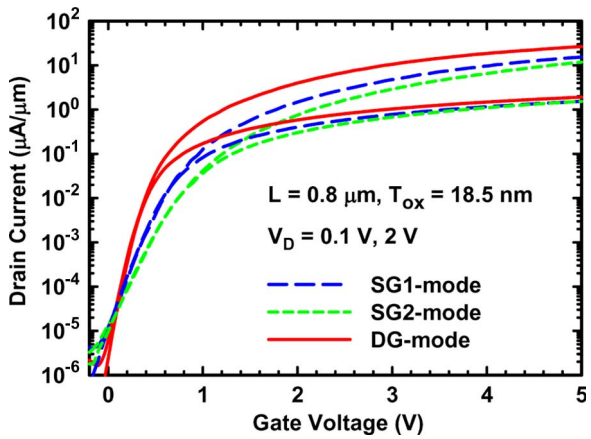



Fig. 2. Transfer characteristics under SG and DG operations. SG1 and SG2 refer to the SG modes with the G1 and G2 serving as the driving gate, respectively.

## III. Modulation of $V_{\rm TH}$ With Back-Gate Bias

Typical transfer characteristics under single-gate (SG) and double-gate (DG) modes are shown in Fig. 2. The SG modes refer to the two modes when the sweeping voltage is applied to one of the two gates (the driving gate), while the other gate is grounded during the measurement. In the figure, G1 and G2 serve as the driving gate for SG1 and SG2 modes, respectively. For the DG mode, the sweeping voltage is applied simultaneously to G1 and G2. As can be seen in the figure, the DG mode exhibits significantly better performance with respect to the two SG modes, as indicated by a higher current drive and a smaller subthreshold swing (SS) of less than 100 mV/dec. The improvement in SS is attributed to the reduction in the effective defect density per unit gated area [11]. Reasons for the increase in current drive are addressed in the next sections.

Fig. 3(a) shows the ability of the device in modulating the $V_{\rm TH}$ of operation. In this case, the sweeping voltage is applied to G1 $(V_{G1})$, while G2, which is dubbed as the $V_{\rm TH}$-control gate, is fixed at a bias $(V_{G2})$ ranging from $-3$ to 3 V. It can be seen that the transfer curves are effectively shifted by varying $V_{G2}$. This is due to the use of the tiny NW channels, which makes the potential level of the entire channel layer sensitive to either gate, allowing a strong back-gate effect; hence, the $V_{\rm TH}$ can be effectively modulated by $V_{G2}$. To further emphasize this point, we also characterize planar devices with similar operation conditions; typical results are shown in Fig. 3(b). The planar devices contain a 50-nm-thick poly-Si channel film sandwiched between a top gate and a bottom gate. Gate oxides of the gates are both 20 nm. In Fig. 3(b), we can see that the $V_{\rm TH}$ is only slightly affected by the bottom-gate voltage. This indicates that the potential of the top channel interface is only weakly dependent on the bottom gate voltage for the planar device. Such a trend is reasonable when considering the large amount of defects contained in the poly-Si layer that tend to trap charges and screen the electric field originating from the bottom gate. A totally different picture emerges with the implementation of tiny NW channels because of the dramatic reduction in the amount of defects. With the tunable $V_{\rm TH}$ capability, the NW devices could be applied for low standby power circuits [13]. For example, in standby circuit operation, a lower subthreshold leakage can be attained by raising the $V_{\rm TH}$ of the transistors. While in active mode, the $V_{\rm TH}$ can be adjusted to a moderate value to provide sufficient driving current.

The extracted $V_{\rm TH}$ and SS from Fig. 3(a) as a function of $V_{G2}$ are depicted in Fig. 4. The plot is divided into two regions by $V_{\rm THDG}$ $(= 0.4$ V), which is the threshold voltage measured under DG mode (see Fig. 2). It can be seen that the $V_{\rm TH}$ of

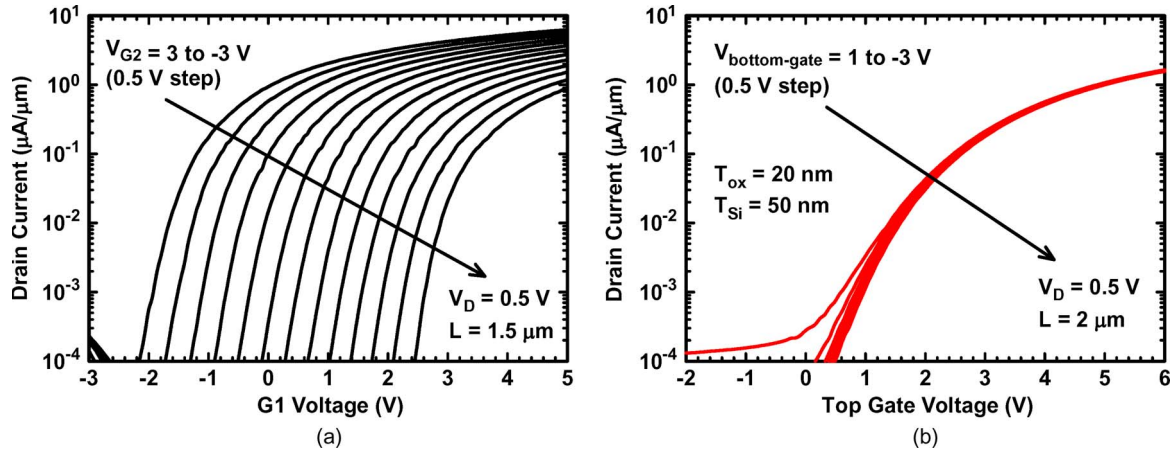



Fig. 3. (a) Transfer characteristics of the NW device having G1 as the driving gate and G2 as the $V_{\rm TH}$-control gate. (b) Transfer characteristics of the planar device driven by the top gate as a function of the bias applied to the bottom gate.

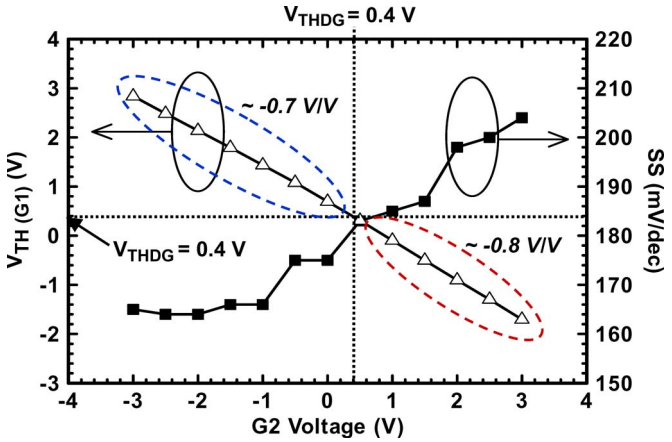



Fig. 4. Extracted $V_{\rm TH}$ and SS as functions of $V_{G2}$ for the NW device under SG1 mode of operation. $V_{\rm THDG}$ denotes the $V_{\rm TH}$ measured in DG mode.

the transfers curves driven by G1 $(V_{\rm TH(G1)})$ is almost linearly modulated by $V_{G2}$. However, a closer look reveals that the exact $V_{\rm TH}$-shift rate $(dV_{\rm TH(G1)}/dV_{G2})$ is $-0.7$ V/V for $V_{G2} < V_{\rm THDG}$, which is slightly smaller than the rate of $-0.8$ V/V in the region where $V_{G2} > V_{\rm THDG}$. Moreover, the SS values in the region where $V_{G2} > V_{\rm THDG}$ are much larger than those where $V_{G2} < V_{\rm THDG}$. When $V_{G2}$ is smaller than $V_{\rm THDG}$, the portion of channel surface gated by G2 is essentially depleted, and the inversion electron layer is mainly induced in the channel near the G1 side as the device is turned on. Under this situation, the $V_{\rm TH}$ modulation ability by $V_{G2}$ is relatively weak due to the longer distance between G2 and the inversion layer. On the other hand, when $V_{G2}$ is larger than $V_{\rm THDG}$, an inversion layer would form near the surface of the NW channel close to the G2 side, unless a sufficiently negative G1 bias is applied to deplete the channel. Under this situation, the effective gate dielectric consists of the gate oxide adjacent to the G1 and the fully depleted body and is thus thicker than the nominal gate oxide. Accordingly, the SS becomes worse. Moreover, switching of the device is mainly determined by the conduction path in the channel near the G2 side, therefore, the $V_{\rm TH}$ is more sensitive to $V_{G2}$.

To more clearly understand the coupling effect between two gates, we can exchange the functions of the G1 and G2 performed in Fig. 3(a) to further investigate the transfer characteristics of the device. The results are shown in Fig. 5(a). Fig. 5(b) depicts and compares the capability of the $V_{\rm TH}$-control gate voltage in modulating the device's $V_{\rm TH}$ based on the results shown in Figs. 3(a) and 5(a). Due to the asymmetrical double-gated configuration, we can see that the $V_{\rm TH}$-shift rates are different in the two cases and that the rate is larger when G1 is employed as the $V_{\rm TH}$-control gate. This is attributed to the better controllability of G1 over the NW channel than G2 due to its larger gated width.

The characteristics about $V_{\rm TH}$ modulation in double-gated device with an ultrathin body have been explored by Masahara *et al.* [13] who proposed a linear potential distribution model to describe the back-gate effect. From the theoretical model, Table I lists equations of $V_{\rm TH}$-shift rate (or back-gate effect factor $\gamma$ [13]) corresponding to the four operation regions specified as (i)–(iv) in Fig. 5(b) with a form related to equivalent channel film $(T_{\rm Si})$ and gate oxide thickness ($T_{\rm OX1}$ and $T_{\rm OX2}$). The extracted $\gamma$ values from the experimental data in different regions shown in Fig. 5(b) are also given in the table. From the equations, the $\gamma$ value in region (i) is equal to the reciprocal of that in region (iv). Similarly, the $V_{\rm TH}$-shift rate in region (ii) is equal to the reciprocal of that in region (iii). Such a relation is experimentally confirmed by the extracted $\gamma$ values since 0.7 is nearly equal to 1/(1.4) and 0.8 is equal to 1/(1.25).

## IV. Impacts of Back-Gate Effect on Device Performance

Comparisons of output characteristics between SG and DG modes are shown in Fig. 6(a). The long-channel device ($L = 5\ \mu$m) is chosen here to eliminate the series resistance effect on drain current. It can be seen that the drain current under DG mode is significantly larger than that under SG modes. To illustrate this finding more clearly more clearly, Fig. 6(b) shows the ratio of drain current of the DG mode to the sum of the two SG modes against drain voltage. The ratio is found to increase with increasing drain voltage from a value around 1.2

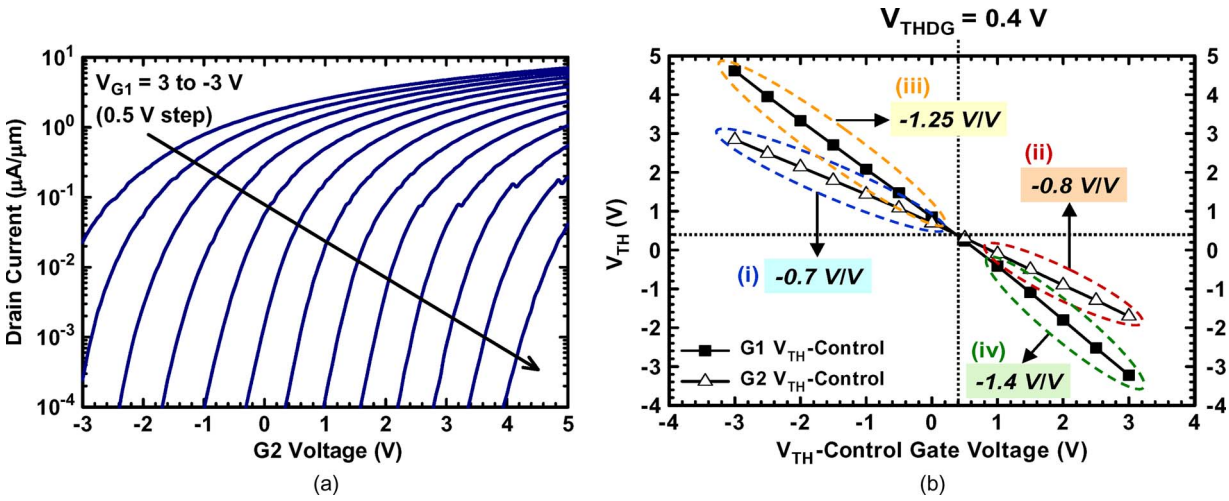



Fig. 5. (a) Transfer characteristics with G2 as the driving gate and G1 as the $V_{\rm TH}$-control gate. (b) Extracted $V_{\rm TH}$ as functions of $V_{\rm TH}$-control gate voltage. The values of the $V_{\rm TH}$-shift rate for the four operation regions are also indicated.

TABLE I
EQUATIONS FOR THE $V_{\rm TH}$-SHIFT RATE UNDER DIFFERENT OPERATION AND BIAS CONDITIONS FROM THE THEORETICAL MODEL [13] AND THE EXPERIMENTAL $V_{\rm TH}$-SHIFT RATES

| $V_{TH}$-control Gate | Top Gate (G2) | | Inverse-T Gate (G1) | |
|---|---|---|---|---|
| Bias Condition | (i) $V_{G2} < V_{THDG}$ | (ii) $V_{G2} > V_{THDG}$ | (iii) $V_{G1} < V_{THDG}$ | (iv) $V_{G1} > V_{THDG}$ |
| Eqs. of $V_{TH}$-shift Rate [13] (Back-gate-effect Factor γ) | $\left\|\frac{\partial V_{THG1}}{\partial V_{G2}}\right\| = \frac{3T_{OX1}}{3T_{OX2}+T_{Si}}$ | $\left\|\frac{\partial V_{THG1}}{\partial V_{G2}}\right\| = \frac{3T_{OX1}+T_{Si}}{3T_{OX2}}$ | $\left\|\frac{\partial V_{THG2}}{\partial V_{G1}}\right\| = \frac{3T_{OX2}}{3T_{OX1}+T_{Si}}$ | $\left\|\frac{\partial V_{THG2}}{\partial V_{G1}}\right\| = \frac{3T_{OX2}+T_{Si}}{3T_{OX1}}$ |
| Exp. Data (V/V) | 0.7 | 0.8 | 1.25 | 1.4 |

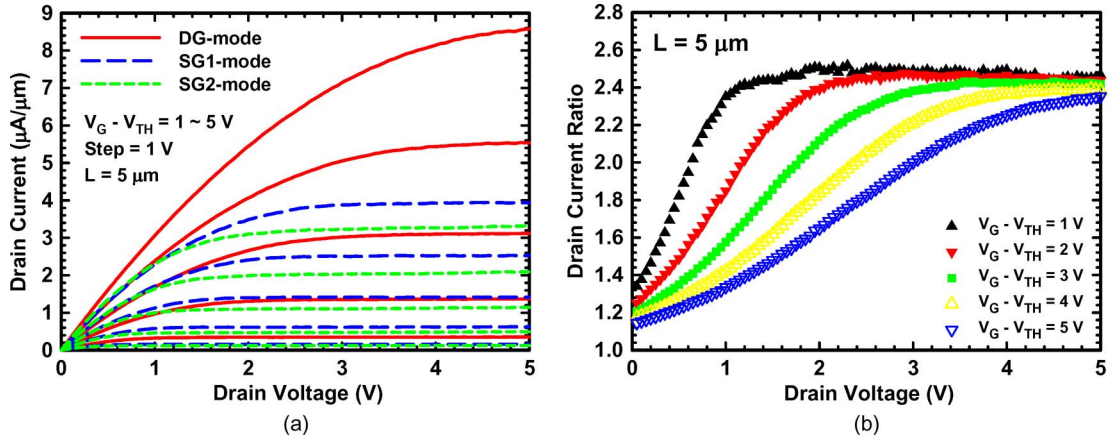



Fig. 6. (a) Output characteristics of the NW device under different operation modes with $L = 5$ $\mu$m. (b) Ratio of the drain current of the DG mode to the sum of the two SG modes. $V_G - V_{\rm TH}$ varies from 1 to 5 V with a step of 1 V.

and becomes saturated at around 2.4. Moreover, the saturation occurs at a smaller drain voltage as $V_G - V_{\rm TH}$ is reduced. We also performed similar measurements on the planar devices having a 50-nm-thick channel, and the results (not shown) indicate that the ratio is around unity. This suggests that due to the thick channel film, the two opposite channels in the planar device do not have any coupling during DG operation. In other words, the overlap of wavefunction (or distribution) of the induced electrons in one of the channels with that of the other channel is negligible. In contrast to the characteristics of the planar device, the tremendous enhancement in the current drive of the NW device shown in Fig. 6 with the DG operation originates from the strong coupling effect of the two opposite gates, owing to the use of ultrathin NW channels.

To gain an insight into the above phenomenon, we have rechecked the output characteristics of the NW device. In Fig. 6(a), it can be noticed that the drain voltage at the onset of a pinchoff (i.e., the saturation drain voltage $V_{\rm Dsat}$) [14] is smaller in SG modes than in DG mode under the same $V_G - V_{\rm TH}$ condition. We replot the $I_D$–$V_D$ curves at $V_G - V_{\rm TH} = 4$ V in Fig. 7 and specify the position of $V_{\rm Dsat}$ for each mode as an example. Apparently, the abnormally high drain current ratio could be partly attributed to the lower $V_{\rm Dsat}$ in the two SG modes, which would limit the saturation current. Such

"early saturation" phenomenon in SG modes could also be described by the aforementioned back-gate effect [15]. Previously, some analytical current voltage ($I$–$V$) models for thin-film SOI devices with a back-gate effect have already been proposed [15]–[17]; here, we utilize a different approach with the potential distribution diagrams under SG1-mode operation illustrated in Fig. 8(a) and (b) to help us understand the cause in a much simpler way. As stated above, for SG1 mode the G2 is grounded while G1 serves as the driving gate. Fig. 8(a) shows the potential distribution in the channel at the source end as $V_{G1}$ is above $V_{\rm TH}$. The channel surface potential ($\varphi_S$) would be pinned at $\varphi_{\rm TH}$, which is the level corresponding to the onset of strong inversion [14], and the voltage drop is mainly across the G1 oxide. On the other hand, the inversion condition for the onset of a pinchoff at the drain side of the channel is $\varphi_S \sim \varphi_{\rm TH} + V_{\rm Dsat}$ due to the shift of quasi-Fermi potential with the applied drain bias, as shown in Fig. 8(b) [14]. Consequently, $V_{\rm Dsat}$ could easily be derived by using the similarity of the triangles formed by the potential line in Fig. 8(b) and can be expressed as

$$V_{\rm Dsat} = (V_G - V_{\rm TH}) \times \frac{3T_{\rm OX2} + T_{\rm Si}}{3T_{\rm OX2} + T_{\rm Si} + 3T_{\rm OX1}} = \frac{V_G - V_{\rm TH}}{1+\gamma} \tag{1}$$

where $\gamma = 3T_{\rm OX1}/(3T_{\rm OX2} + T_{\rm Si})$ is the back-gate-effect factor of region (i) shown in Fig. 5(b) and Table I. $V_{\rm Dsat}$ for SG2 mode can be analogically derived with the form similar to (1), except $\gamma = 3T_{\rm OX2}/(3T_{\rm OX1} + T_{\rm Si})$ corresponding to the region (iii) shown in Fig. 5(b) and Table I. By using the gradual-channel and charge-sheet approximation [14], the inversion charge density along the channel can be expressed as

$$Q_i(V) = -C_{\rm ox}\left[V_G - V_{\rm TH} - (1+\gamma)V\right] \tag{2}$$

where $C_{\rm ox}$ is the gate oxide capacitance per unit area and $V$ is the location-dependent quasi-Fermi potential due to the drain bias. Subsequently, by integrating $Q_i(V)$ through the entire channel with the integral equation form $I_D = (W/L)\mu_{\rm eff}\int_0^{V_D}[-Q_i(V)]dV$, the drain current at ON-state can be expressed as

$$I_D = K\left(V_G - V_{\rm TH} - \frac{1+\gamma}{2}V_D\right)V_D, \quad \text{when } V_D \le V_{\rm Dsat} \tag{3}$$

$$I_{\rm Dsat} = K\frac{(V_G - V_{\rm TH})^2}{2(1+\gamma)}, \quad \text{when } V_D \ge V_{\rm Dsat} \tag{4}$$

where $K$ is the transconductance parameter equal to $(W/L)\mu_{\rm eff}C_{\rm ox}$, $\mu_{\rm eff}$ is the effective carrier mobility, $L$ is the channel length, and $W$ is the channel width. It should be noted that $\gamma$ is equal to zero under DG mode [13] because there is no back-gate effect under DG operation as the channel body is ultrathin. It should be noted that, although based on a simple scheme shown in Fig. 8, the above derivation based on the simple potential diagrams (Fig. 8) is actually consistent with the theoretical models presented previously [15], [16].

Furthermore, by applying the extracted $\gamma$ value for each operation mode into (3) and (4), interestingly, we found that the measured output characteristics can be well fitted by the equations as an appropriate $K$ value is used. Such treatments are shown in Fig. 9, in which the output characteristics measured under different operation modes are compared with the computational $I$–$V$ curves based on (3) and (4). The $K$ values used in the computational $I$–$V$ curves are $4.9 \times 10^{-8}$, $4.65 \times 10^{-8}$, and $1.15 \times 10^{-7}$ S/V for SG1, SG2, and DG modes, respectively. As can be seen in the figures, the calculation results well describe the experimental data.

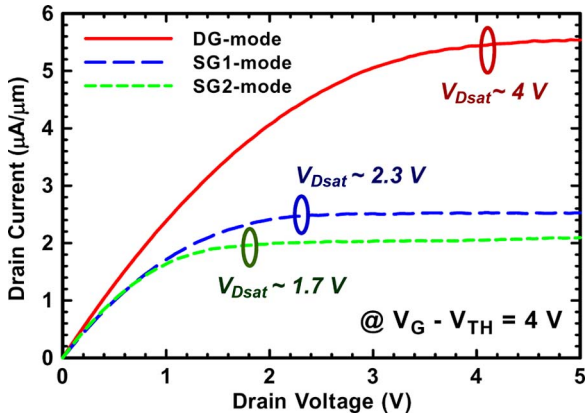



Fig. 7. $I_D$–$V_D$ curves for the NW device operated under various modes at $V_G - V_{\rm TH} = 4$ V.

From the above analysis, we can understand that the reason for the much higher $V_{\rm Dsat}$ of DG operation is the elimination of the back-gate effect. Moreover, the current ratio should reach a constant as the applied drain bias is larger than $V_G - V_{\rm TH}$, i.e., the $V_{\rm Dsat}$ of DG mode, since then, the drain currents of all operation modes become saturated. This is, indeed, confirmed in Fig. 6(b). However, one remaining issue is the assumption of a constant $K$ value for each operation mode as we use (3) and (4) to fit the experimental $I$–$V$ curves in Fig. 9. Since $K$ is closely related to the transconductance ($GM$) and $\mu_{\rm eff}$, we present the measured results of these parameters and probe their influences on device characteristics next.

## V. Mobility Enhancement With DG Operation

Fig. 10(a) shows the $GM$ of the device under different operation modes at $V_D = 0.1$ V. As can be seen in the figure, the $GM$ approaches a constant value as $V_G$ is sufficiently high. The less attenuation in high vertical field region is ascribed to the fact that carrier transport in poly-Si channel is mainly affected and limited by the defect-induced potential barrier at grain boundaries [18]–[20]. This would answer the question of why a constant $K$ value can be used for fitting the experimental data shown in Fig. 9. The extracted ratio of $GM$ of the DG mode to the sum of the two SG modes $(GM_{\rm DG}/(GM_{\rm SG1} + GM_{\rm SG2}))$ as a function of $V_G - V_{\rm TH}$ is depicted in Fig. 10(b). In the same figure, the data of a planar device are also included for comparison. The ratio is essentially unity for the planar device, indicating the two opposite gates are operated independently. Unlike the planar counterpart, it can be seen that the $GM$ ratio of the NW device is obviously higher than unity, and a large enhancement reaching ~40% at a

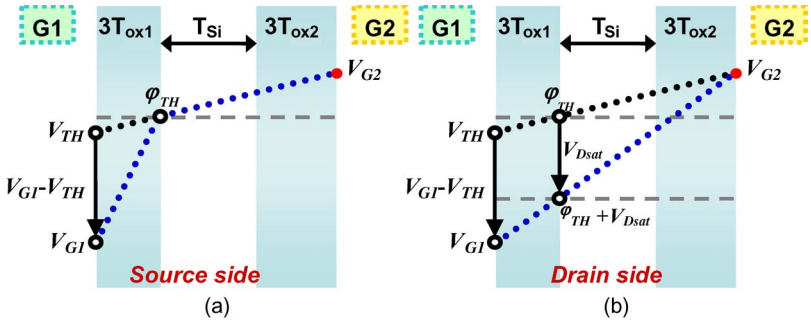



Fig. 8. Schematic potential distribution for SG1-mode operation of the NW device at (a) the source side and (b) the drain side of the channel under a pinchoff bias condition.

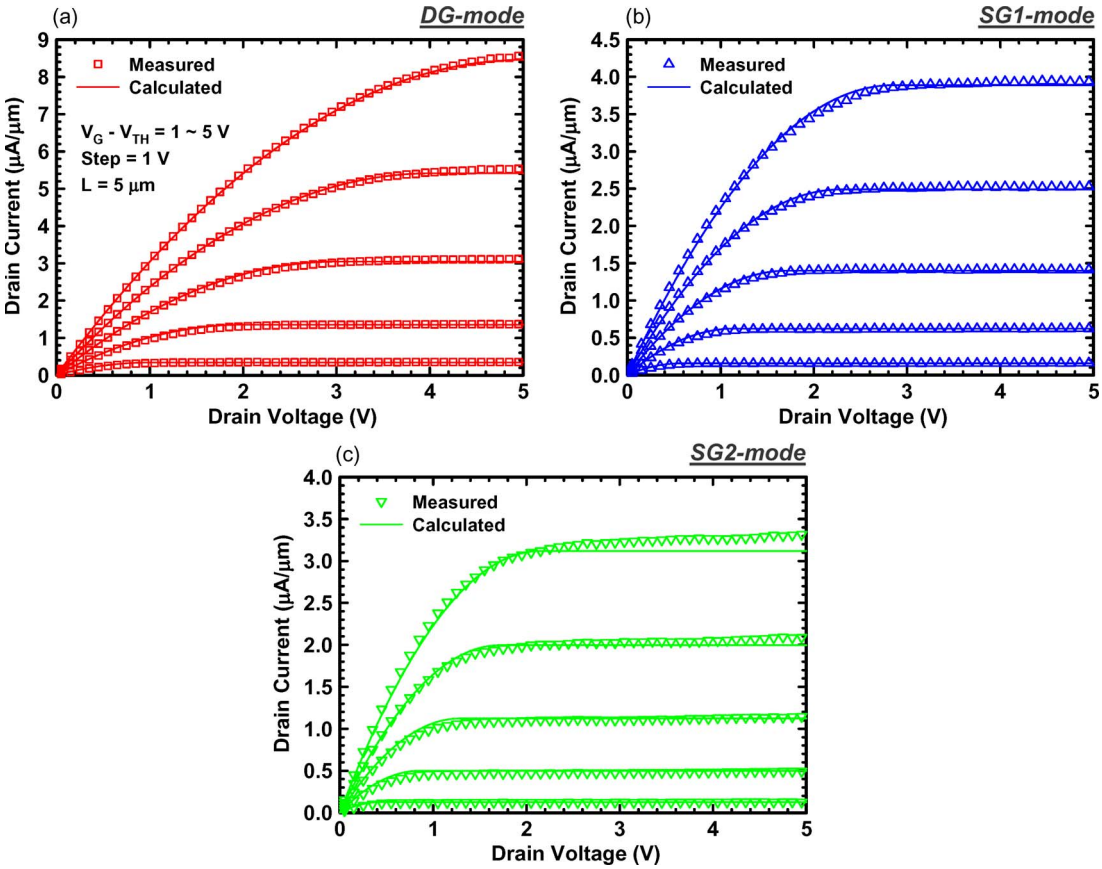



Fig. 9. Comparisons of output characteristics between the measured data and calculated results of each operation mode based on the proposed model.

low vertical electric field is obtained. This implies that the DG operation, indeed, offers enhancement in the effective mobility of the NW device.

In a previous work [19], it has been shown that the carrier conduction is mainly governed by the potential barrier presented at the grain boundaries, and the effective mobility contained in $K$ can be expressed as

$$\mu_{\text{eff}} = \mu_o e^{-qV_B/k_BT} \tag{5}$$

where $\mu_o$ is a constant, $q$ is the charge of an electron, $V_B$ is the grain boundary potential barrier, $k_B$ is the Boltzmann constant, and $T$ is the absolute temperature. The values of $V_B$ extracted from the $I$–$V$ characteristics measured at different temperatures are shown in Fig. 11. For all operation modes, $V_B$ decreases with increasing $V_G$–$V_{\text{TH}}$, owing to the increase in the concentration of inversion electrons in the channel [18]. However, with respect to the SG modes, $V_B$ is effectively lowered for the DG mode, confirming the inference made above that the DG operation can provide mobility enhancement. In Fig. 12, the $GM$ ratio is plotted together with the ratio $[W \times e^{-qV_B/k_BT}]_{\text{DG}}/([W \times e^{-qV_B/k_BT}]_{\text{SG1}} + [W \times e^{-qV_B/k_BT}]_{\text{SG2}})$ against $V_G - V_{\text{TH}}$, where $W$ is the channel width for each operation mode. It is interesting to note that the two curves are very close and follows the same trend. This observation and the above analysis confirm that the mobility enhancement due to the reduction of potential barrier height for transport carriers is another major factor responsible for the performance improvement with the DG operation.

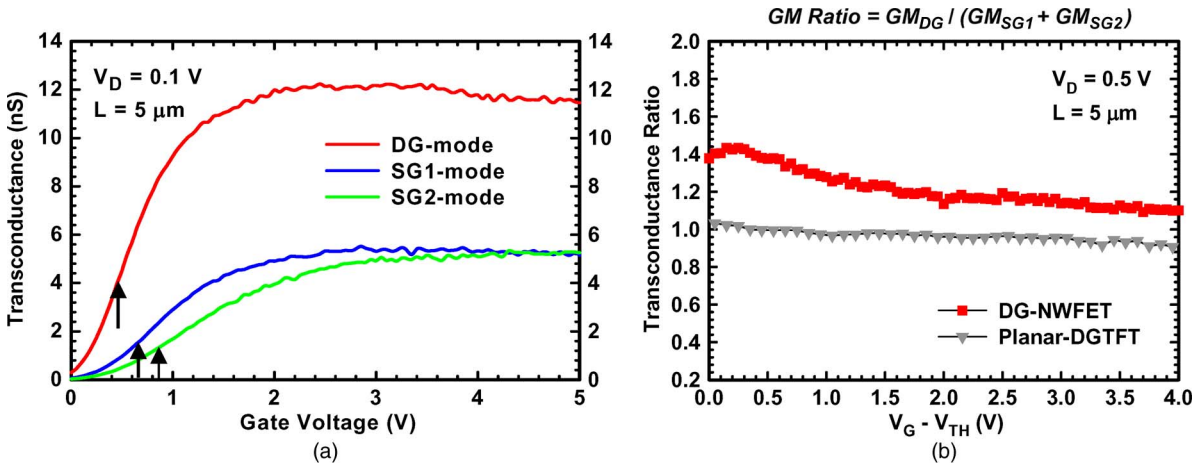



Fig. 10. (a) $GM$ of the NW device versus $V_G$ under different operation modes. The arrows indicate the $V_{\rm TH}$. (b) Ratio of the $GM$ of the DG mode to the sum of the two SG modes as a function of $V_G - V_{\rm TH}$. Results for the planar device are also included for comparison.

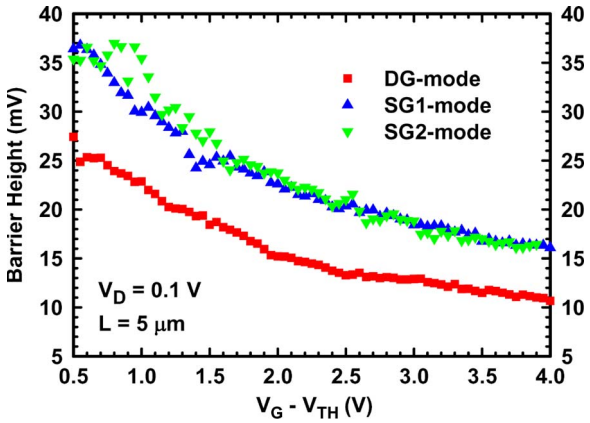



Fig. 11. Extracted barrier height for the NW device operated under SG and SG modes as a function of $V_G - V_{\rm TH}$.

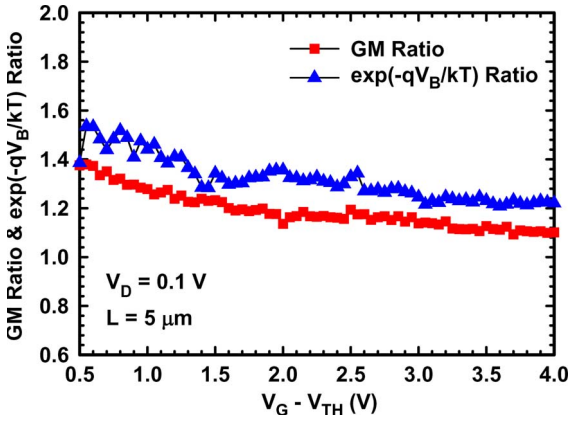



Fig. 12. Ratios of $GM$ and $e^{-qV_B/k_BT}$ of DG mode to the sum of two SG modes as a function of $V_G - V_{\rm TH}$.

## VI. Conclusion

In this paper, characteristics of a poly-Si NW device featuring independent DG configuration have been characterized and analyzed. In the device, the ultrathin NW channels are surrounded by an inverted-T gate and a top gate. With the independent DG scheme, several modes, including the DG and two SG modes, can be implemented in the device operation. In addition, because of the ultrathin NW channels, the transfer characteristics of the device driven by one of the gates are profoundly affected by the bias condition of the other gate. The experimental results point out that the DG mode outperforms the sum of the two SG modes. For example, transfer curves with an SS of less than 100 mV/dec are only seen with the DG mode. Anomalous enhancement in the current drive with the DG mode is also observed. Based on the analysis, the above current enhancement with the DG mode is mainly because of the elimination of the back-gate effect encountered in SG mode as well as the improved effective mobility.

## Acknowledgment

The authors would like to thank J.-F. Huang and the National Nano Device Laboratories for the assistance in device fabrication.

## References

[1] D. Hisamoto, W. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asana, T. King, J. Bokor, and C. Hu, "A folded channel MOSFET for deep-sub-tenth micron era," in *IEDM Tech. Dig.*, 1998, pp. 1032–1034.

[2] J. Fu, N. Singh, C. Zhu, G.-Q. Lo, and D.-L. Kwong, "Integration of High- $k$ dielectrics and metal gate on gate-all-around Si-nanowire-based architecture for high-speed nonvolatile charge-trapping memory," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 662–664, Jun. 2009.

[3] E. Stern, A. Vacic, and M. A. Reed, "Semiconducting nanowire field-effect transistor biomolecular sensors," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3119–3130, Nov. 2008.

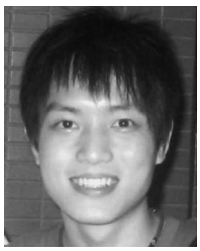
[4] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, no. 5533, pp. 1289–1292, Aug. 2001.

[5] Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, "Controlled growth and structures of molecular-scale silicon nanowires," *Nano Lett.*, vol. 4, no. 3, pp. 433–436, Mar. 2004.

[6] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C. C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5 nm-gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.

[7] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, "High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm)

gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.
[8] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee, and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 643–645, Sep. 2005.
[9] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2471–2477, Oct. 2006.
[10] M. Im, J.-W. Han, H. Lee, L.-E. Yu, S. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y.-K. Choi, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102–104, Jan. 2008.
[11] H. C. Lin, H. H. Hsu, C. J. Su, and T. Y. Huang, "A novel multiple-gate polycrystalline silicon nanowire transistor featuring an inverse-T gate," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 718–720, Jul. 2008.
[12] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-30, no. 10, pp. 1244–1251, Oct. 1983.
[13] M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Matsukawa, K. Ishii, T. Sekigawa, H. Yamauchi, H. Tanoue, S. Kanemaru, H. Koike, and E. Suzuki, "Demonstration, analysis and device design considerations for independent double-gate MOSFETS," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2046–2053, Sep. 2005.
[14] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[15] J. P. Colinge, *Silicon on Insulator Technology: Materials to VLSI*. Boston, MA: Kluwer, 1997.
[16] H. K. Lim and J. G. Fossum, "Current–voltage characteristics of thin-film SOI MOSFETs in strong inversion," *IEEE Trans. Electron Devices*, vol. 31, no. 4, pp. 401–408, Apr. 1984.
[17] D. D. Lu, M. V. Dunga, C. H. Lin, A. M. Niknejad, and C. Hu, "A multi-gate MOSFET compact model featuring independent-gate operation," in *IEDM Tech. Dig.*, 2007, pp. 565–568.
[18] J. Y. W. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, no. 12, pp. 5247–5254, Dec. 1975.
[19] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, no. 2, pp. 1193–1202, Feb. 1982.
[20] F. V. Farmakis, J. Brini, G. Kamarinos, C. T. Angelis, C. A. Dimitriadis, and M. Miyasaka, "On-current modeling of large-grain polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 701–706, Apr. 2001.



**Hsing-Hui Hsu** was born in Taipei, Taiwan, in 1982. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, in 2004 and the M.S. degree from the National Chiao Tung University, Hsinchu, Taiwan, in 2008, where he is currently working toward the Ph.D. degree at the Department of Electronics Engineering.

His current research interests include the fabrication and characterization of Si nanowire FETs and memory devices.

**Horng-Chih Lin** (S'91–M'95–SM'01) was born in I-Lan, Taiwan, on August 1, 1967. He received the B.S. degree from the National Central University, Chung Li, Taiwan, in 1989 and the Ph.D. degree from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1994.

From 1994 to 2004, he was with the National Nano Device Laboratories, where he was engaged in the research projects on nanoscale device technology development. He joined the faculty of NCTU in 2004, where he is currently a Professor with the Department of Electronics Engineering and the Institute of Electronics. His current research interests include thin-film transistor (TFT) fabrication and characterization, reliability of CMOS devices, and nanowire device technology. He is the author or a coauthor of over 100 technical papers in international journals and conference proceedings in the above areas.

Dr. Lin served on the Program Committee of the International Reliability Physics Symposium (IRPS) 2001 and 2002 and the International Conference on Solid State Devices and Materials (SSDM) 2005–2008.

**Tiao-Yuan Huang** (S'78–M'78–SM'88–F'95) received the B.S. and M.S. degrees in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1971 and 1973, respectively, and the Ph.D. degree from the University of New Mexico, Albuquerque, in 1981.

After serving for two years in the Taiwanese Navy as fulfillment of his conscription duty, he left for the U.S. in 1977. He has worked in the U.S. semiconductor industry for 14 years prior to his return to his native country, Taiwan. Since 1995, he has been a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he is also with the Institute of Electronics.

Prof. Huang was the recipient of the Semiconductor International's Technology Achievement Award for his invention and demonstration of the fully overlapped lightly doped drain MOS transistors.