provide both positive and negative optical signals in the same device by changing only the pattern of the negative bias, and does not need the second short s.a.w. pulse for scanning optical image as used in usual convolvers.[1] Because of the large photoconductivity of CdS, the device proposed in this letter is competent for a high-sensitivity optical imaging device. However, with respect to the spatial resolution of the optical image the device is not satisfactory at present. The semiconductive CdS s.a.w. delay line with a high resistivity surface layer can improve both spatial resolution and sensitivity.

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8th November 1977

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0013-5194/78/0676-0026 $1.50/0

FAULT DETECTION IN SEQUENTIAL MACHINES WITH INCREASED FAULT COVERAGE

Indexing terms: Fault detection, Sequential machines

This letter develops an approach for fault detection and checking sequence design of sequential machines based on the principle of machine modification through augmentation of extra input and extra outputs, taking into consideration the case where faults occurring in a machine may cause an increase in its number of states.

In recent years, with increasing demand in system reliability, the problem of fault-tolerant machine design and fault diagnosis has assumed significant importance. Concurrently, advances in the technology of circuit modules and integrated circuits have limited the experimenter's freedom in checking all interconnections, putting more emphasis on terminal measurements. The problem of fault detection, and design of checking sequences for sequential machines, was considered by many authors.[1-6] Recent work by several authors demonstrated that the problem can be much simplified by modifying a given sequential machine M into a new machine M' by augmenting extra input symbols, or output terminals. This letter considers the problem of fault detection and that of designing checking sequences for sequential machines based on the aforesaid principle of machine modification through augmenting special input and output symbols. Given a sequential machine, an approach is developed in the letter that utilises the above principle to considerably simplify the problem of fault detection and that of designing checking sequences. One major advantage of this approach is that it is applicable even if the original machine is not strongly connected, because the original machine, on modification, becomes strongly connected; further, the modified machine always possesses distinguishing sequences even if the original machine does not. In particular situations where faults occurring in a machine cause an increase in the number of states of the machine, the present approach still remains applicable. This latter type of machine faults may occur where the total number of machine states q satisfies the inequality $2^{m-1} < q < 2^m$, with some of the m-tuples of the m state variables being left unassigned.

Define a finite, deterministic, synchronous, completely specified, reduced sequential machine of the Mealy type by the quintuple $M = \langle I, S, 0, f, g \rangle$ where I, S and 0 are, respectively, the input, state and output alphabets of the machine, and f and g denote, respectively, the next state and output mappings. Without any loss of generality, assume that the number of states q of the machine M satisfies the inequality $2^{m-1} < q < 2^m = q'$, m being the number of memory elements used in the realisation. We propose to modify the given machine M by augmenting one extra input symbol I_e, and $[\log_2 q]$ output terminals, where $[r]$ denotes the smallest integer greater than or equal to r. The m-tuples of the state variables are arbitrarily assigned to the states of M as follows. Assign the m-tuple 00 ... 001 to the state S_1, 00 ... 010 to the state S_2, and so on up to the state S_q, while the remaining unused m-tuples, $q' - q$, excepting the all-zero combination, are each designated by $S_{q+1}, S_{q+2}, \ldots, S_{q'-1}$, where the number j in each S_j is the decimal value of the m-tuple designated by S_j, the all zero combination being designated by $S_{q'}$. The next state and output mappings corresponding to the special input symbol I_e are defined as follows: $f(S_i, I_e) = S_{i+1}$; $g(S_i, I_e) = i$; $f(S_{q'}, I_e) = S_1$; $g(S_{q'}, I_e) = 0$; $1 \leqslant i \leqslant q' - 1$. The outputs corresponding to the augmented input I_e appear at the augmented output terminals, the decimal value of the output being $\beta \in \{0, 1, \ldots, q' - 1\}$. The modified machine is evidently a c.c. machine.[5] The input symbol I_e happens to be a distinguishing sequence of length one for the modified machine. Assume here that no faults can occur in M associated with the next state transitions and outputs corresponding to the input I_e, and during the fault detection experiment, no new faults can occur. As an illustration consider the transition table of a machine M_1 as given in Table 1. Table 2 gives the transition table of the modified machine M_1'.

Table 1 MACHINE M_1

State \ Input	0	1
$S_1(01)$	$S_2, 1$	$S_3, 0$
$S_2(10)$	$S_2, 0$	$S_3, 0$
$S_3(11)$	$S_2, 0$	$S_1, 1$

Table 2 MODIFIED MACHINE M_1'

State \ Input	0	1	I_e
$S_1(01)$	$S_2, 1$	$S_3, 0$	$S_2, 1$
$S_2(10)$	$S_2, 0$	$S_3, 0$	$S_3, 2$
$S_3(11)$	$S_2, 0$	$S_1, 1$	$S_4, 3$
$S_4(00)$	–	–	$S_1, 0$

We finally give a procedure that can be utilised in the detection of faults and in designing checking sequences for a given sequential machine M.

Procedure

(*a*) Apply the special input symbol I_e at the augmented input terminal repeatedly until an output of zero appears at the augmented output terminals. This ensures that the machine M is at the initial state S_1.

(*b*) Start at S_1. Apply I_e at the augmented input terminal $k - 1$ times, $k \leqslant q$, and record the corresponding output responses produced at the augmented output terminals. This operation transfers M from S_1 to a state S_k.

(*c*) At the state S_k, apply the input symbol I_i at the original input terminals, and observe the corresponding output O_i at the original output terminals. This transfers M from S_k to

some other state S_j. Next apply I_e at the augmented input terminal once, and note the resulting output at the augmented output terminals. If the transition S_j is nonfaulty, then M can be transferred from S_j to only $S_{j+1}, j \leqslant q$. For a faulty transition S_j, M is transferred either to $S_{j+1}, q+1 \leqslant j \leqslant q'-1$, or to S_1, for $j = q'$. The response produced at the augmented output terminals definitely identifies the state S_j.

(*d*) Continue (*b*) and (*c*) for every state S_k, $k = 1, 2, \ldots, q$ of M, and for every state S_m, for all inputs $I_i, i = 1, 2, \ldots, p$.

Based on a knowledge of the aforesaid steps, the checking sequence for M can also be designed quite readily. The present approach for fault detection and design of checking experiments for sequential machines by adding extra input and output logic not only results in short, simple and efficient experiments, but simultaneously permits an increased fault coverage not usually possible in most checking experiments. In the process the only compromise that is adopted, viz. added logic against complex and lengthy experiments, does not appear too costly and hence unacceptable.

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2nd December 1977

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0013-5194/78/0713-0028 $1.50/0

MEDIUM POWER 12-18 GHz AMPLIFIER MODULE

Indexing terms: Field-effect transistor circuits, Microwave amplifiers, Schottky gate field-effect transistors, Solid-state microwave circuits

Broadband Ku-band amplification has been extended into the range of medium power levels. A single-ended 100 mW amplifier stage has been developed for the 12-18 GHz frequency band using a GaAs Schottky-barrier field-effect transistor. Minimum gain at 20 dBm of output power was 4 dB. When operating in the driver mode, a minimum gain of 5 dB at an output power of 15 dBm was measured across Ku-band. Higher gains can easily be achieved by cascading several of these amplifier stages. Gain, output power and impedance characteristics as a function of frequency are discussed.

Recently a power transistor was described by W. R. Wisseman that yielded a spot frequency output power of 850 mW at 18 GHz.[1] Another excellent result was published in 1975 by RCA researchers who succeeded in achieving 220 mW at 18 GHz.[2] While medium power transistors working at 18 GHz were reported as early as 1975,[2] and broadband low noise amplification as early as 1976,[3] medium power broadband amplification covering the entire frequency range of Ku-band is just beginning to emerge.

This letter describes the results obtained on a single-ended Ku-band amplifier module using a medium-power GaAs Schottky-barrier field-effect transistor. The module was designed for the 12-18 GHz band to yield a small-signal gain of at least 4·5 dB and an output power of 100 mW at a minimum gain of 4 dB. To the best of our knowledge this is the first time that the entire Ku-band has been covered with a single-ended GaAs f.e.t. amplifier yielding a minimum output power of 20 dBm. We shall summarise the small-signal gain and the gain characteristics at the 20 dBm output power level, as well as the amplifier module's impedance behaviour.

The GaAs field-effect transistor used in our experiments is the power version of the WJ-F110. Gate length of this transistor is 1 μm while gate width is 300 μm. The active epitaxial layer of the WJ-F110 power version has been grown to a thickness yielding saturation currents (I_{DSS}) of 100-125 mA. When tuned for optimum output power at 18 GHz, this device has exhibited output powers in excess of 22·5 dBm at 1 dB compression points ($V_{DS} = 10$ V, $I_{DS} = 60$ mA).

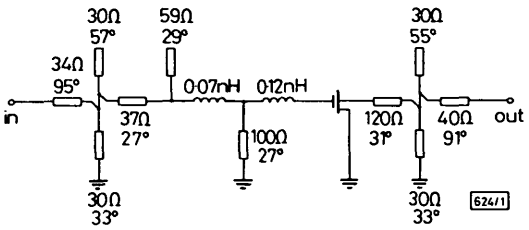

Fig. 1 *Single-ended Ku-band amplifier module showing input and output matching networks for the WJ-F110*

$f_0 = 15$ GHz

Fig. 1 is a schematic of the input and output matching networks consisting of open-ended and shorted stubs interconnected by either transforming microstrip line elements or inductors. All transmission-line lengths in Fig. 1 are given in degrees at 15 GHz. The complicated input network was necessitated by a relatively low real component of the input impedance of the transistor (between 3 and 5 ohms). The reactive component of the transistor's input impedance was approximately represented by a series-resonant circuit consisting of a capacitor (0·42 pF) and an inductor (0·12 nH) intro-

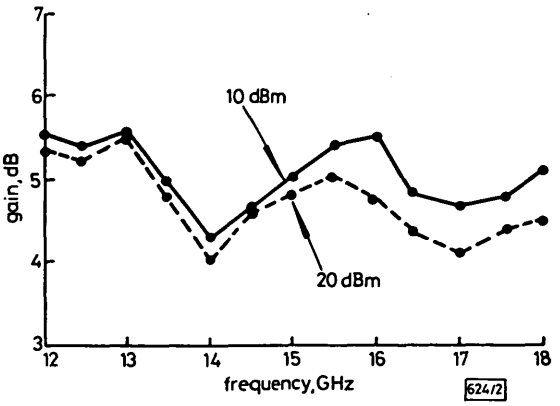

Fig. 2 *Gain against frequency for $V_{DS} = 9$ V and $I_{DS} = 55$-61 mA*

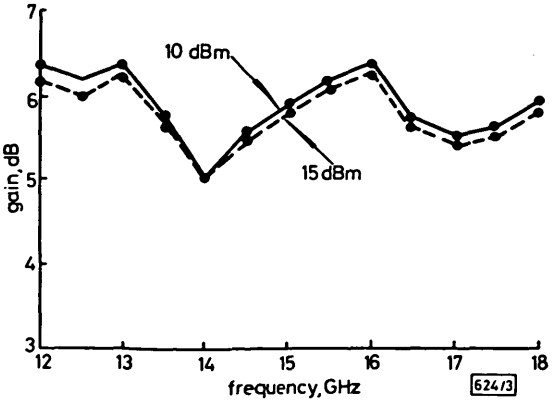

Fig. 3 *Gain against frequency for $V_{DS} = 7$ V and $I_{DS} = 74$ mA*