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Large-Signal Analysis of Lo–Hi–Lo Double-Drift Silicon IMPATT Diodes at 50 GHz

LANG-CHEE CHANG MEMBER, IEEE, AND DING-HUA HU

***Abstract*—Large-signal analysis of a lo-hi-lo double-drift silicon IMPATT diode at 50 GHz shows that the device is capable of output power of 1.1 W and efficiency of 20 percent for a device area of 2×10^{-5} cm^2 at a dc biasing current density of 12 kA/cm^2 and ac voltage amplitude of 12 V. It is also found that, both output power values and efficiencies decrease with increasing enhanced leakage current.**

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L. C. Chang is with Telecommunication Laboratories, Ministry of Communications, P.O. Box 71, Chung-Li, Taiwan, Republic of China.
D. H. Hu is with National Chiao Tung University, Taiwan, Republic of China.

I. Introduction

High-efficiency double-drift (DD) silicon IMPATT diodes with lo-hi-lo doping profiles have been previously proposed [1]. Devices with efficiency of 25 percent for 12 GHz, 24 percent for 18 GHz, and 19 percent for 50 GHz have been predicted. It has also been shown that efficiencies can be improved significantly by varying buried positions if proper buried widths and background doping concentrations are chosen [1], [10].

The purpose of this paper is to report the large-signal properties of a lo-hi-lo DD silicon IMPATT diode at 50 GHz. The

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effects of enhanced leakage current on the output power and efficiency are also discussed.

II. Large-Signal Analysis

A computer program similar to that described by Yu and Tantraporn [2] has been developed to analyze the large-signal characteristics of IMPATT diodes. Specifically, given a periodic voltage waveform applied to a diode, the program simulates the one-dimensional dynamic behaviors of the electric-field intensity, hole concentration, electron concentrations, and current waveform, and then evaluates the large-signal characteristics of the diode.

The diode is biased with a dc voltage and driven by an ac voltage through a coupling capacitor [3], i.e., $V_D = V_{dc} + V_{ac} \sin(2\pi f t)$, where f is the operating frequency. The normalizing factors used to normalize the basic semiconductor equations are the same as those presented by Peterson [4]. The results of Canali *et al.* [5] are used to calculate carrier velocities at 430 K. Carrier ionization rates are evaluated by fitting Grant's data [6].

The initial values of the hole and electron concentrations are either supplied by a previous run or are given by solving the following normalized equations [4], $\partial E/\partial X = D(X)$, $\partial p/\partial X = EP$, and $\partial n/\partial X = -En$, where $D(X)$ is the doping concentration, and all other quantities have their conventional meanings. The above equations are obtained by neglecting electron and hole concentrations in Poisson's equation, and assuming that both electron and hole currents equal zero. For boundary conditions, the concept of the energy barrier [2] is applied at the electrodes. The injection currents, given by $J_{inj} = AT^2 \exp[-(\beta - C\sqrt{E})/kT]$, are used to simulate the saturation currents at electrodes, with $\beta = 1.0$ eV for silicon material, where J_{inj} is the injection hole (electron) current density at n-side (p-side) electrode, A the Richardson constant, C the image force constant, E the electric field, k the Boltzmann constant, and T the temperature.

The terminal current as seen external to the diode is calculated as

$$J_{ext}(t) = \frac{1}{W} \int_0^W J_T(X, t)\, dX \tag{1}$$

where the total current $J_T(X, t)$ is composed of particle currents and displacement current. By Fourier analysis, we have

$$J_{ext}(t) = A_0 + A_1 \cos 2\pi f t + B_1 \sin 2\pi f t + \cdots . \tag{2}$$

A_0 is the dc current density J_{dc} of the diode. The diode large-signal conductance and susceptance are evaluated as $G = B_1/V_{ac}$ and $B = A_1/V_{ac}$, respectively. The microwave output power density is given by $P_{out} = -V_{ac}B_1/2$. The dc to microwave generating efficiency is $\eta = (P_{out}/J_{dc}V_{dc}) \cdot 100$ percent.

Basically, the continuity equations are in the form of nonlinear elliptic equations [7], [8]. For a given number of space gridding i, the number of time gridding j should be large enough so that the stability criterion is satisfied, i.e., $\lambda \leq \epsilon_1$, where $\lambda = \Delta t/\Delta x^2$, $\Delta t = \tau/j$, and $\Delta x = W/i$. $\tau = 1/f$ is the period of oscillation. Note that the quantities discussed in this paragraph are in normalized form [4]. In our calculations for the 50-GHz device, j should not be less than 420, if $\epsilon_1 = 0.05$ and $i = 100$. Typical computer time on a CDC CYBER 172 computer is about 8 min for each run, if $i = 100$ and $j = 420$.

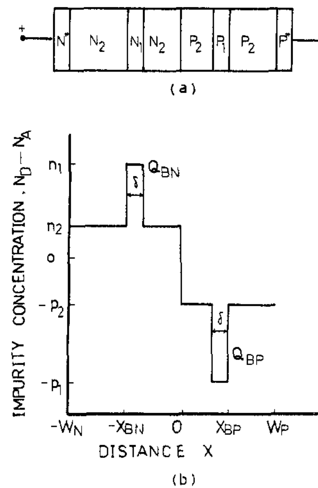

Fig. 1. Lo-hi-lo doping profile DD IMPATT diode. (a) Device structure. (b) Doping profile.

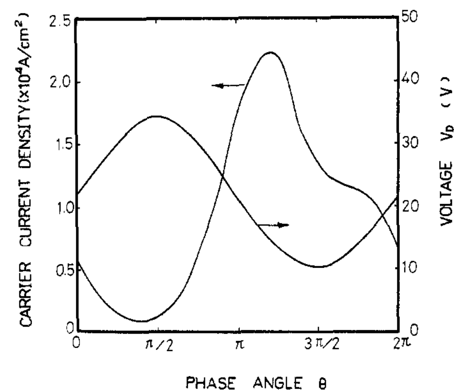

Fig. 2. Current and voltage waveforms as a function of the phase angle. $J_{dc} = 10$ kA/cm^2, $V_{ac} = 12$ V, $V_{dc} = 22$ V, $G = -629$ mhos/cm^2, $B = 2606$ mhos/cm^2, $\eta = 20.6$ percent, $P_{out} = 45.3$ kW/cm^2.

III. Numerical Results

The device structure and doping profile of this diode are shown in Fig. 1, with n-type background concentration $n_2 = 3.65 \times 10^{16}$ cm^{-3}, p-type background concentration $p_2 = 4.02 \times 10^{16}$ cm^{-3}, n-type buried quantity $Q_{BN} = 2.46 \times 10^{12}$ cm^{-2}, p-type buried quantity $Q_{BP} = 2.47 \times 10^{12}$ cm^{-2}, n-type buried position $X_{BN} = 0.08$ µm, p-type buried position $X_{BP} = 0.073$ µm, buried width $\delta = 0.03$ µm, n-type depletion width $W_N = 0.56$ µm, p-type depletion width $W_P = 0.51$ µm, and total depletion width $W = W_N + W_P = 1.07$ µm. According to the results of static calculations [1], [10], the above device parameters are chosen so that the diode has moderate high efficiency.

The current and voltage waveforms are shown in Fig. 2. The spatial distributions of the electric field, electron density,

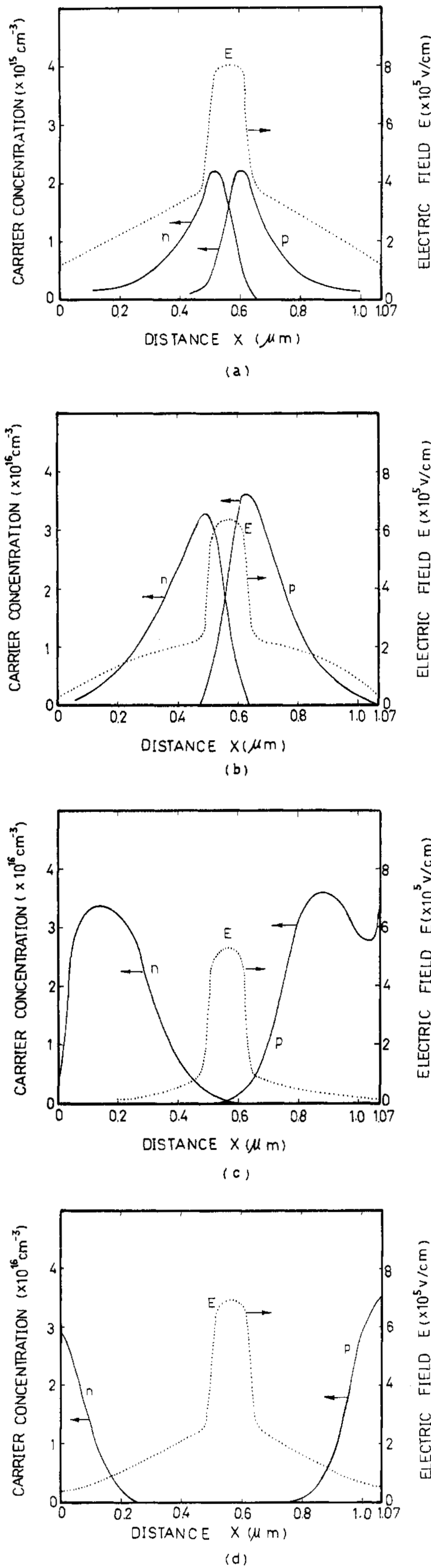

Fig. 3. Spatial distributions of the electric field, electrons, and holes in the diode, with the same operation condition as that of Fig. 2, at the time specified by the indicated phase angle. (a) Phase angle $\theta = \pi/2$. (b) Phase angle $\theta = \pi$. (c) Phase angle $\theta = 3\pi/2$. (d) Phase angle $\theta = 2\pi$.

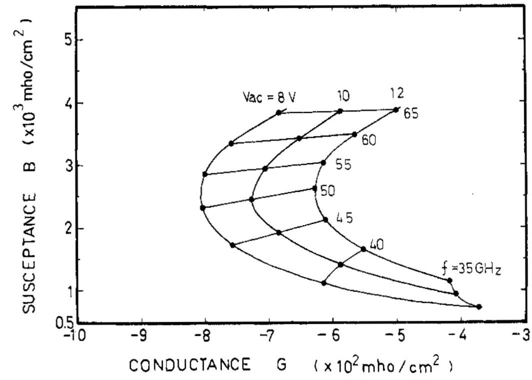

Fig. 4. Diode admittance (susceptance versus conductance) as a function of frequency and ac voltage amplitude. J_{dc} = 10 kA/cm^2.

and hole density are shown in Fig. 3 for phase angle $\theta = \pi/2$, π, $3\pi/2$, and 2π. Electrons and holes are generated at $\theta = \pi/2$. As $\theta > \pi/2$, the electron and hole bunches are growing both temporally and spatially. At $\theta = \pi$, the carrier bunches are fully grown. As $\theta > \pi$, the carrier bunches are traveling toward the electrodes nearly at their scattering-limited velocities.

Fig. 4 shows that diode admittance plot. For a diode area of 2×10^{-5} cm^2, the depletion capacitance is about 0.2 pF, which is equivalent to a susceptance value of 0.06 mho (or 3000 mho/cm^2) at 50 GHz. We may conclude from Fig. 4 that the diode susceptance is predominately due to the diode's depletion capacitance.

Figs. 5 and 6 show the variations of output power and efficiency as functions of the dc current density for various leakage current levels. The leakage current J_l is simulated by adding $J_{lN} = J_l \cdot W_N/W$ and $J_{lP} = J_l \cdot W_P/W$ to the injection currents of n-type and p-type electrodes, respectively. It has been found that output power and efficiency decrease significantly when the leakage current density is greater than 25 A/cm^2. For $J_l = 0$, maximum efficiency of 20.7 percent is obtained for $J_{dc} = 9.9$ kA/cm^2, and $V_{ac} = 12$ V. For $J_l = 0$, $J_{dc} = 12$ kA/cm^2, and $V_{ac} = 12$ V, the output power density is about 54 kW/cm^2, and the efficiency is 20 percent. For a device area of 2×10^{-5} cm^2, this implies that we can have an output power of 1.1 W.

IV. Conclusions and Discussions

A computer simulation program for large-signal analysis of IMPATT diodes has been developed. Detailed "snapshots" for the spatial distributions of the electric field, electron density, and hole density are presented to show the dynamic characteristics of the DD IMPATT diodes.

Microwave output power values and efficiencies for various dc operation current densities and leakage currents, have been evaluated. It has been found that, for dc current density larger than 9.9 kA/cm^2, as the current density increases, output power increases, while efficiency decreases. Therefore, there are tradeoffs between the output power and the efficiency. In addition, output power values and efficiencies decrease significantly when the leakage current density is greater than 25 A/cm^2. This shows that radiation-enhanced leakage current can significantly affect the device operation [9].

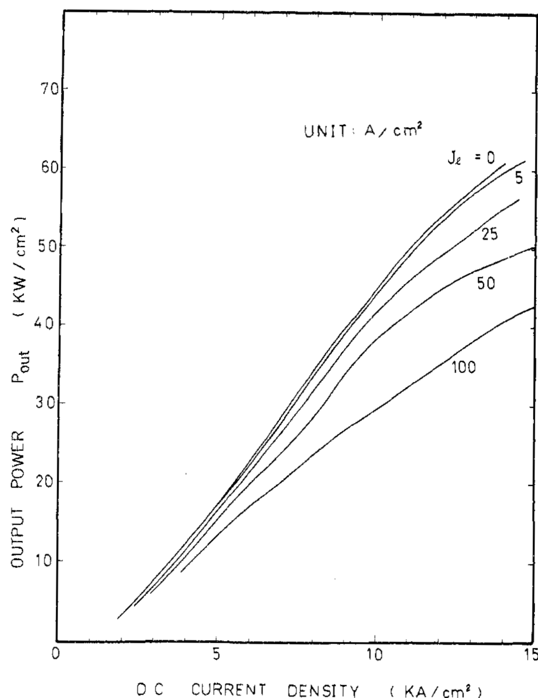

Fig. 5. Diode output power as a function of dc current density for various leakage current levels at 50 GHz. V_{ac} = 12 V.

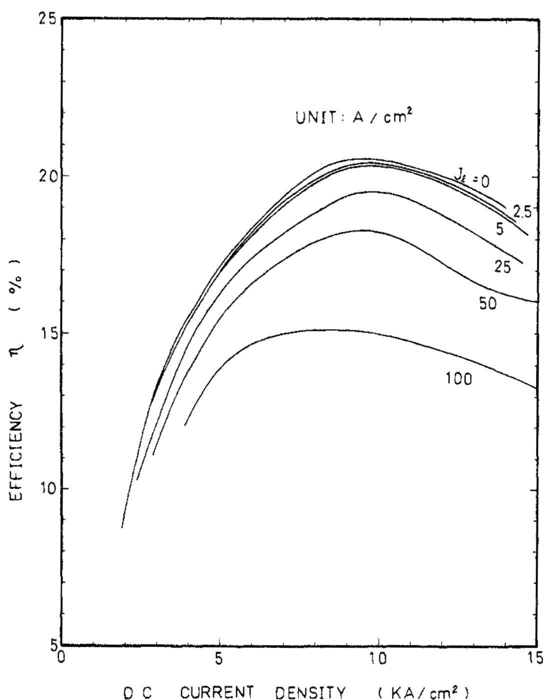

Fig. 6. Diode efficiency as a function of dc current density for various leakage current levels at 50 GHz. V_{ac} = 12 V.

The efficiencies obtained from the static calculation [1], [10] and the large-signal analysis are quite consistent. Furthermore, large-signal calculations show that the 50-GHz device can have output power of 1.1 W and efficiency of 20 percent for a device area of 2×10^{-5} cm^2, with a dc biasing current density at 12 kA/cm^2 and ac voltage amplitude of 12 V. In comparing with Seidel's [11] experimental results of p-n junction DD structure which has a maximum output power of 1 W and maximum efficiency of 14.2 percent at 50 GHz, we conclude that lo-hi-lo DD structure may have higher efficiency value and comparable output power. Thus lo-hi-lo DD IMPATT diodes are useful for high-power solid-state microwave applications.

Finally, parasitic series resistance and thermal dissipation are not considered in this simulation. The presence of parasitic series resistance will reduce the net negative resistance and, thus, cause a reduction in output power. The dc power dissipation in the diode will increase the junction temperature. This induces several effects such as an increase in thermal emission (leakage) current and breakdown voltage [12], and a reduction in ionization rates [6] and carrier drift velocities [5] to modify the output power values obtained in this simulation.

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