small difference between the two curves is due to the change of the electron mobility caused by the impurities. Furthermore τ_ϵ is almost constant ($\simeq$0.45 ps.) in the range of the electric field from 10^4 V · cm^{-1} to 10^5 V · cm^{-1}.

In conclusion, Monte Carlo calculations have been performed on the effect of ionized impurities on high-field electron transport properties at room temperature in silicon. We found that for concentration higher that 10^{18} cm^{-3} the impurity effects on drift velocity and mean energy are still present at field strength as high as 10^5 V · cm^{-1}. At the highest impurity concentrations a superohmic behavior of $v_d(E)$ is found, and no saturation of v_d is attained.

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Shifting of the Peak Generation Rate in Double-Drift Silicon IMPATT Diodes

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***Abstract*—In double-drift (DD) silicon IMPATT diodes, it is observed that the peak generation rates of both carriers (electrons and holes) lie within the n side. The shifting is due to the unequal ionization rates for electrons and holes in silicon. By neglecting the reverse saturation current, a simple analytical expression for the location where the peak generation occurs is derived. This simple result may be useful for the design of double-drift as well as complementary single-drift IMPATT diodes.**

The central avalanche region is worth noting in the design consideration of DD IMPATT diodes because the ionization process produces the greatest generation of electrons and holes in this region. Especially in millimeter-wave diodes, the depletion region is very narrow and the transit-time delay for both the electron and hole particle currents (space-charge waves) must be made equal to assure efficient operation.

Consider a reverse-biased symmetrical DD silicon IMPATT diode, shown in Fig. 1(a); the avalanche region width is defined as [1]

$$I_n(x_1) - I_n(x_2) = 0.95 I_{dc}. \tag{1}$$

The avalanche region width $x_A = x_2 - x_1$ must be minimized under the constraint [2]

$$-dI_n/dx = \alpha I_n + \beta I_p = dI_p/dx \tag{2}$$

is largest as shown in Fig. 2, where I_n and I_p are electron and hole particle currents, respectively, and α and β are ionization rates for electrons and holes, respectively.

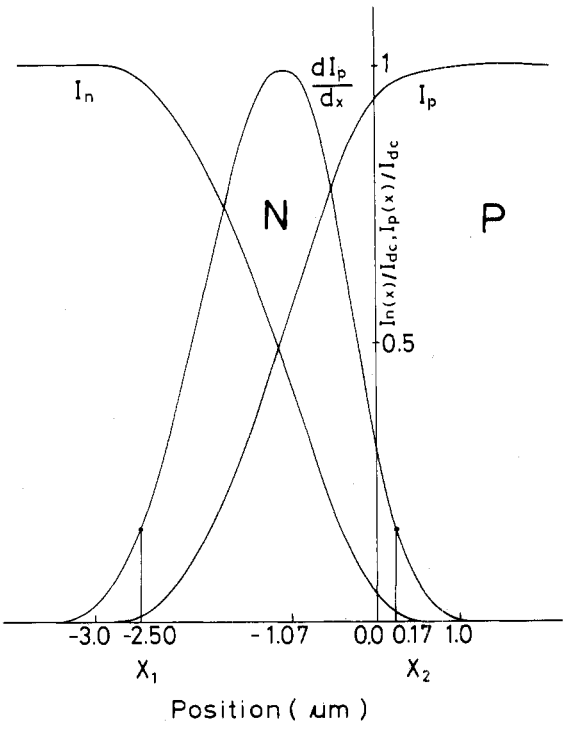
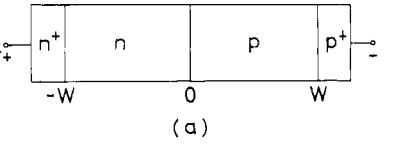


Fig. 1. (a) Structure of a DD IMPATT diode biased at breakdown voltage. (b) The electric field profile corresponds to Fig. 1 (a).



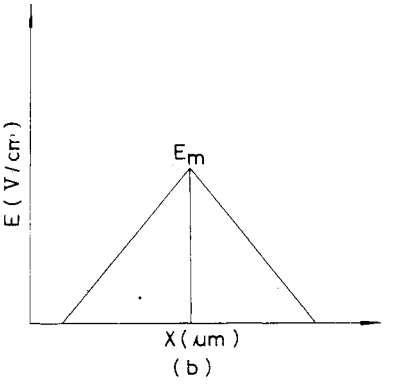


Fig. 2. The profiles of the electron and hole particle currents I_n and I_p associated with their ionization rates, dI_p/dx are sketched for the diode having the structure shown in Fig. 1 (a). The diode is operated at 6 GHz with the depletion width $W = 5.5$ μm, doping concentration $N_B = 4.7 \times 10^{15}$ cm^{-3}, maximum field $E_m = 3.97 \times 10^5$ V/cm.

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For the two symmetrical positions $-x_0$ and $x_0/(x_0 > 0)$,

$$dI_p(x_0)/dx - dI_p(-x_0)/dx = [I_p(x_0) - I_p(-x_0)][\beta - \alpha] < 0 \tag{3}$$

i.e., the generation rate is larger in the n side than in the p side.

Neglecting the reverse saturation current, the hole and electron particle currents can be expressed as [3]

$$I_p(x)/I_{dc} = 1 - \left[1 - \int_{-W}^{x} \langle\beta\rangle\, dx'\right][\beta/\langle\beta\rangle] \tag{4a}$$

$$I_n(x)/I_{dc} = 1 - \left[1 - \int_{x}^{W} \langle\alpha\rangle\, dx'\right][\alpha/\langle\alpha\rangle] \tag{4b}$$

where

$$\langle\alpha\rangle = \alpha \exp\left[\int_{W}^{x} (\alpha - \beta)\, dx'\right]$$

$$\langle\beta\rangle = \beta \exp\left[\int_{-W}^{x} (\alpha - \beta)\, dx'\right].$$

The generation rates are

$$dI_p(x)/I_{dc}dx = + \left[(\alpha/\beta)\langle\beta\rangle - (\alpha - \beta)\int_{-W}^{x} (\alpha/\beta)\langle\beta\rangle\, dx'\right][\beta/\langle\beta\rangle] \tag{5a}$$

$$dI_n(x)/I_{dc}dx = - \left[(\beta/\alpha)\langle\alpha\rangle - (\alpha - \beta)\int_{W}^{x} (\beta/\alpha)\langle\alpha\rangle\, dx'\right][\alpha/\langle\alpha\rangle]. \tag{5b}$$

The peak generation rate occurs when

$$d^2[I_p(x)/I_{dc}]/dx^2 = 0$$

i.e.,

$$[(\alpha - \beta)^2 - d(\alpha - \beta)/dx]\left(\int_{-W}^{x} \alpha[\langle\beta\rangle/\beta]\, dx'\right) - [\alpha(\alpha - \beta) - d\alpha/dx][\langle\beta\rangle/\beta] = 0 \tag{6a}$$

or

$$d^2I_n(x)/I_{dc}dx^2 = 0$$

i.e.,

$$[(\alpha - \beta)^2 - d(\alpha - \beta)/dx]\left(1 - \int_{x}^{W} \langle\alpha\rangle\, dx'\right) - [\alpha(\alpha - \beta) - d\alpha/dx][\langle\alpha\rangle/\alpha] = 0. \tag{6b}$$

If we assume [4]

$$\alpha(E) = A_1 \exp[-(b_1/E)]$$

$$\beta(E) = A_2 \exp[-(b_2/E)]$$

then

$$d\alpha/dx = (\alpha b_1/E^2)(dE/dx) \qquad d\beta/dx = (\beta b_2/E^2)(dE/dx)$$

usually $\alpha \approx 10\beta$, $b_2 \approx 1.5b_1$ in the vicinity where the electric field is about 3×10^5 V/cm.

To the first-order approximation, both (6a) and (6b) reduce to the same equation:

$$d\alpha/dx = \alpha(\alpha - \beta) > 0 \tag{7}$$

which indicates that the peak generation is within the n side. For the diode structure depicted in Fig. 1(a), (7) can be reduced to

$$E^2(x)[\alpha(x) - \beta(x)] = (qN_B/\epsilon)b_1 \tag{8}$$

where N_B is the doping concentration and $x < 0$.

Numerical calculation has shown that the position predicted by (8) deviates from the exact peak generation position within an error of 0.5 percent of the total depletion width.

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Determination of Dopant Profiles by Voltage Measurements

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***Abstract*—The dopant profile in the channel of a double-gated J-FET with uniformly doped channel and substrate is determined from measurements of gate voltage pairs at pinchoff. This procedure offers advantages over the *C–V* method in cases of imprecisely known gate area, or in the presence of significant stray capacitance.**

The *C–V* method for determining impurity concentration profiles near p-n junctions [1], [2], Schottky barrier [3] and MOS contacts [4], [5] requires accurate knowledge of the junction area, which enters quadratically in the equation for impurity concentration and linearly in the equation for position. The junction area is, however, not well defined in certain functional devices. Buried channel and peristaltic charge-coupled devices [6], [7], for example, use a narrow "channel stop" p^+ gate to an epitaxial n layer on a p substrate. When the width of the p^+ gate is not very large compared to the depth of the p^+ layer, the resulting junction curvature causes an imprecisely defined junction area. Moreover, when the junction area is small, stray capacitance can introduce a serious error in the capacitance determination. Also, the interpretation of *C–V* data is complicated when the channel is almost pinched off [8], [9].

In this note we describe a method for determination of the impurity distribution by means of voltage measurements and without requiring capacitance measurements. This method provides the nonuniform dopant profile in an n layer between two p^+ gates with the same limitations for rapidly varying profiles as the *C–V* method [10]. The uniform concentrations of p-substrate and n-channel dopants, and the n-cchannel height between a p^+ gate and a p substrate can be obtained by our method, as will be demonstrated.

We measure corresponding pairs of channel stop voltage V_c and substrate voltage V_s with n channel grounded and just pinched off. For any given V_c, a corresponding V_s is determined by the intercept of the extrapolated square root of the channel saturation current with the zero current axis, as shown by the dashed lines in Fig. 1. The deviation of the dashed line extrapo-

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