the voltage at which successive ramps start and their slope. The latter needs to be maintained at a level consistent with the requirement for a half triangle which is symmetrical about the zero line, i.e. with a time-averaged value of zero. An integrator may be used to generate the ramp as before, but only a single current generator will be required.

In order that the two intermediate waveforms give a low-distortion triangle when summed, it is necessary that their edges be very fast. This can be accomplished by using high-speed switching devices to switch an output buffer from the integrator voltage to ground at the end of each ramp. Thus very sharp edges can be obtained, while allowing a whole halfcycle for the integrator to be reset to any required offset voltage from which successive ramps will start. Of the two parameters mentioned above, the former can be implemented by a static offset voltage applied to the integrator, and only the latter needs to be controlled by a feedback loop.

A complete system is now described which makes use of two identical half-triangle generators operating in antiphase, the triangle being produced from a subtraction of their two outputs. This is shown in Fig. 2.

Two antiphase square-wave signals swinging between 5 V negative and zero are generated from the input signal and fed to the inputs of two half-triangle generators. The outputs of these are fed into a differential amplifier to produce a triangle wave, or into the differential inputs of a piecewise-linear circuit to give a sinusoid output. The half-triangle generator used is shown schematically in Fig. 3, and its operation is as follows:

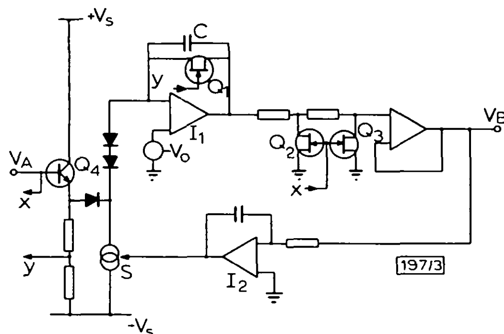

Fig. 3 *Half-triangle generator*

Transistors Q_1, Q_2 and Q_3 form switches which are supplied with appropriate control voltages derived from V_A. While V_A is in its negative state, Q_1, Q_2 and Q_3 are made nonconducting, thereby causing integrator I_1 to ramp up under the control of the current source S, the ramp output voltage V_B following the integrator. When V_A returns to zero, Q_1, Q_2 and Q_3 are made to conduct, Q_2 and Q_3 forcing V_B to zero, and Q_1 discharging the capacitor C. The integrator is thus returned to the bias voltage $-V_0$ (typically about 2 V negative) and the output current of S now flows through Q_4. The same bias voltage is applied to the corresponding integrator in the other half-triangle generator, thus ensuring that the waveforms produced will be of the same amplitude.

Thus, on each downward transition of V_A, the output voltage V_B is returned to $-V_0$ and then rises at a constant rate determined by S. When V_A returns to zero, V_B follows and is held at zero until the next downwards transition.

Now, it is required that V_B shall have risen to exactly $+V_0$ at the instant V_A returns to zero, and this is ensured by making the current supplied by S dependent on the output voltage of a second integrator I_2, which monitors V_B. If S is supplying current at the correct rate, V_B follows a half triangle which is symmetrical about the zero line, so having a time-averaged value of zero. The output voltage of I_2 thus remains constant and S continues to supply current at this rate. In fact, there will also be an alternating component superimposed on this output voltage, which must remain negligible throughout the range of operation of the system if the distortion is to be kept minimal; this is discussed in the next paragraph. If S supplies current at any other rate, the output waveform will be such that V_B has a net time-averaged value. The output direct voltage level of I_2 is thus incrementally shifted on each cycle until it attains the correct value.

The integrating time of I_2 must be chosen for a given frequency range to give low distortion, i.e. by making the integrating time sufficiently large so as to ensure that the alternating component on the output of I_2 is small, and a reasonably high slew rate, which is inversely proportional to the integrating time. Obviously, a particular value of the integrating time allows only reasonable values of these over a limited frequency range, and to overcome this we normally incorporate a suitably connected diode to switch the integrating capacitor to a larger value when the output of I_2 is below a certain d.c. level, corresponding to when the system is operating below a particular frequency.

In a particular application, such a system was used in conjunction with a 6-segment piecewise-linear network to produce a sinusoid which exhibited a distortion figure of typically 0·2% over a frequency range of 2 Hz–25 kHz. A frequency sweep rate, i.e. the maximum rate at which frequency could be swept without significant distortion, of $40\% s^{-1}$ was obtained in the upper frequency régime (above about 150 Hz) and about a twentieth of this in the lower régime. The slew-rate, which is a measure of how quickly the system recovers after the frequency of the input signal is switched, was about 1 decade second in the upper régime and 0·06 in the lower régime. The acquisition time we define as being the time between the application of an input signal and the emergence of a low-distortion sinusoid, and this had a constant value of 4 s in the upper régime, and was frequency dependent in the lower régime, being 25 s at 5 Hz and 14 s at 50 Hz, for example. Phase jitter was less than 0·0003 rad.

The lowest frequency of operation was extendable to 0·2 Hz, giving an overall range of more than 10^5 Hz, by external switching of the value of integrating capacitor used in the lower régime, with subsequent degradation of the sweep and slew rates for this régime and of the acquisition time of the system as a whole.

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NEW V-GROOVE INTEGRATED INJECTION LOGIC

Indexing term: Integrated injection logic

A new V-groove integrated injection logic (v.i.i.l.) is proposed which combines the V-groove technology and the double-diffused bipolar technology. The fabrication processes are qualitatively described. The lateral *p–n–p* transistor of the i.i.l. is located on the vertical V-shape surface, and the effective base width is controlled by the combination of the vertical diffusion process and the V-groove etching rate. A 1-dimensional analysis is used and an approximate expression for the collector current of the lateral *p–n–p* transistor is given. The v.i.i.l. is expected to have a higher production yield than that of the ordinary i.i.l.

Recently, the integrated injection logic (i.i.l.) has caused a great deal of interest, because its low power-delay-time product and high packing density.[1,2] At about the same time, the anisotropic etching[3] of the V-groove technology was introduced to the device fabrication. The device chip density has greatly increased as a result of the V-groove technology.[4]

There are a number of problems, however, with the ordinary i.i.l. technology, as the current gains in both the lateral *p–n–p* and vertical *n–p–n* transistors in the unit cell of i.i.l. are quite low.[5] Although the current gains in both transistors may be improved by the control of the width of the neutral n^- region,[6] the base width of the lateral *p–n–p* transistor is crucially controlled by the lateral double-diffusion processes of the *p* region and the multiple collector n^+ regions of the *n–p–n* vertical transistor. As a result, the performance of

ordinary i.i.l. is not as good as expected and the production yield is still quite low.

In this letter, we propose a new V-groove integrated injection logic (v.i.i.l.), which combines bipolar and V-groove technologies. The new device eliminates some weaknesses of ordinary i.i.l. The fabrication processes of the v.i.i.l. are briefly described in the following and a qualitative analysis of the collector current in the lateral p–n–p transistor of the v.i.i.l. is given also. As with the usual V-groove technology, (100) wafers are used so that an anisotropic etch may be used.[3, 4] After the double diffusion of the p and n^+ regions, the device structure is as shown in Fig. 1, where the n^+ regions are used for both the multiple collector regions of the vertical n–p–n transistor and the isolation regions between the adjacent unit cells of the i.i.l. Some of the key fabrication

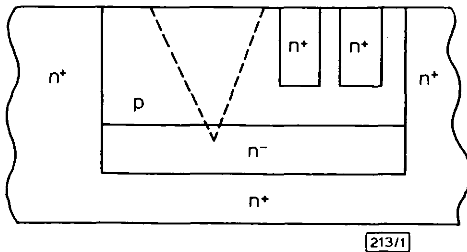

Fig. 1 *Device structure after diffusion of single p region and n⁺ regions for both isolation and multicollector areas of n–p–n vertical transistor*

The broken line is the area for the vertical etching

processes are different from those of ordinary i.i.l., however: (*a*) the unit cell contains only a single p region, instead of two, so the crucial spacing alignment between the adjacent p region of the unit cell in the ordinary i.i.l. process is avoided, (*b*) the control in the vertical width of the neutral n^- region under the p area is similar to the ordinary i.i.l., but the width will be controlled to as small as possible[6] in the better process and (*c*) the surface area of the p region is large enough for the vertical etching.

The second step in the fabrication is the same process as that of the V-groove technology.[3, 4] The vertical etching window is opened in the p diffusion surface, and the groove is etched down to the n^- regions, as indicated by the broken lines in Fig. 1.

As a consequence of these fabrication processes, the v.i.i.l. will contain all the merits of the ordinary i.i.l. Since the base width of the vertical n–p–n transistor is controlled by the planar bipolar technology, and, if the width of the neutral n^- region is reduced, the current gains in both the vertical n–p–n and lateral p–n–p transistors will be improved by the current-suppression effect.[6] Also, the effective base width of the lateral p–n–p transistor is located at the bottom portion of the vertical surface in the n^- region, and the base width will be accurately controlled by the vertical etching distance; e.g. if a slow etching rate $\simeq 10\ \mu$m/h is used,[3] the width may be well controlled up to about 0·1 μm range. By viewing the difficulties from the double-diffusion processes of the p and n^+ regions in the lateral control of the base width in the lateral p–n–p transistor of ordinary i.i.l., the production yield

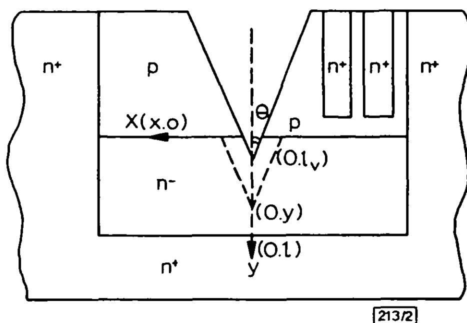

Fig. 2 *Final v.i.i.l. configuration*

l_v is the vertical etching distance in the n^- region, l is the width of the total neutral n^- region and θ is the angle of the V-groove surface makes with the vertical y-axis

of v.i.i.l. will be much higher than that of ordinary i.i.l. technology.

The collector current in the n^- base region of the p–n–p transistor of the v.i.i.l. will be a 2-dimensional flow. For physical insight, the collector current will be treated by a simple 1-dimensional analysis and a lower limit of the actual value will be found. The co-ordinate system is as shown in Fig. 2, where l_v is the vertical etching distance in the n^- region and l is the total width of the n^- region.

The collector hole currents after injection from the emitter–base p–n^- junction will travel across a V-shape base and are then collected by the base–collector junction. However, the V-shape travelling distance increases as the injection point $(x, 0)$ moves away from the V-shaped corner. The corresponding effective base width then increases as x increases.

The collector current density in the 1-dimensional analysis is given by

$$J(x, y) = \frac{qP_{n0}\, D_p \exp{(qv/kT)}}{2\sqrt{(x^2 + y^2)}}$$

and the total current I per unit length in the z direction may be expressed as

$$I = \int_{l_v}^{l} J\, dy$$

and $x = y \tan\theta$; therefore

$$I = \frac{qD_p\, P_{n0} \exp{(qv/kT)} \cos\theta}{2}\, l_n(l/l_v) \quad . \quad . \quad . \quad . \quad (1)$$

where P_{n0} is the equilibrium hole density in the n^- region, D_p is the hole diffusion constant, v is the forward-bias voltage drop across the emitter–base junction and θ is the angle between the V-groove and the vertical y-axis.

For comparison, the dimension of the vertical diffusion p region in ordinary i.i.l. will be taken to be the same as the lateral base width, so the corresponding collector current as given by eqn. 1 will be equal to $qD_p\, P_{n0} \exp{(qv/kT)}$. The neutral n^- region in ordinary i.i.l. is greater than 4 μm if the vertical etching distance l_v is controlled to 0·2 μm by a slower etching rate, and, if θ is 35°,[3] the collector current in the lateral p–n–p transistor of the v.i.i.l is slightly larger than that of ordinary i.i.l. by a factor of 1·2. If the current-suppression effect is taken into consideration, the collector current of the v.i.i.l. will tend to decrease slightly, owing to a decrease in l, whereas the current in ordinary i.i.l. will tend to increase by an increase in the vertical injection area, but, at the same time, the difficulties in control of the lateral base width of ordinary i.i.l. are also inherently increased. Since the structure of a single p region per unit cell is used in v.i.i.l., the process step will be simpler than that of ordinary i.i.l., and, since the base of the lateral p–n–p transistor in vi.i.l. is located in the vertical V-shaped surface and the base width will be accurately controlled by the vertical slow etching rate of the well established V-groove technology, the production yield of v.i.i.l. will be much higher than that of ordinary i.i.l. technology.

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