Design Considerations of High-Efficiency Double-Drift Silicon IMPATT Diodes

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***Abstract*—High-efficiency silicon double-drift IMPATT diodes with a low–high–low doping profile structure are proposed. Devices with efficiencies of 25 percent for 12 GHz, 24 percent for 18 GHz, and 19 percent for 50 GHz, are predicted by numerical calculations.**

I. Introduction

Double-drift (DD) IMPATT diodes [1]–[2] are expected to have better efficiency and output power than their single-drift (SD) counterparts. A reliable 15-percent-efficiency silicon DD IMPATT diode at 11–13 GHz has been obtained by Lekholm *et al.* [4]. An efficiency of 21 percent was predicted by Seidel *et al.* [3] for a silicon DD Readlike diode at X band.

In this investigation, high-efficiency silicon DD IMPATT diodes with a low–high–low doping profile structure are designed. Starting from the simple p-n-abrupt-junction structure, the device operation efficiencies were calculated numerically, and noise measures were compared. Finally, the shift of the avalanche center from the metallurgical junction was discussed, and used to correct the optimum depletion widths.

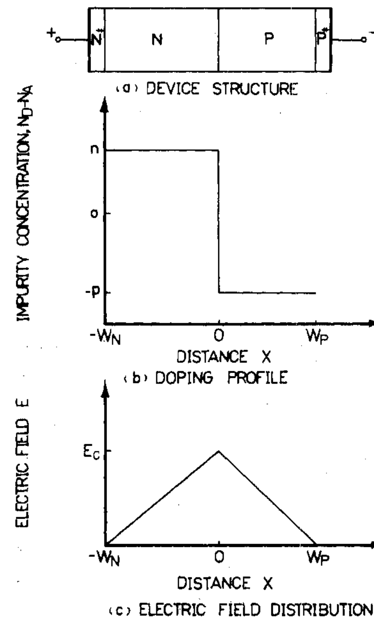

Fig. 1. p-n-abrupt-junction DD IMPATT diode.

II. Efficiency

Two types of DD IMPATT diodes are studied: a) the p-n-abrupt-junction structure, and b) the low–high–low doping profile structure.

A. The p-n-Abrupt-Junction Structure

For the p-n-abrupt-junction structure (Fig. 1), the electric field distribution is

$$E(x) = \begin{cases} E_c + \dfrac{qnx}{\epsilon}, & -W_N \le x \le 0 \\ E_c - \dfrac{qpx}{\epsilon}, & 0 \le x \le W_P \end{cases} \tag{1}$$

where the critical field

$$E_c = \frac{qnW_N}{\epsilon} = \frac{qpW_P}{\epsilon} \tag{2}$$

and n and p are the n-type and p-type region doping concentrations; and W_N and W_P are the n-type and p-type region depletion widths. For a given operating frequency f, the optimum depletion widths [5] are given by $W_N = 0.37\ v_{\mathrm{sl},e}/f$ for electrons, and $W_P = 0.37\ v_{\mathrm{sl},h}/f$ for holes, where $v_{\mathrm{sl},e}$ and $v_{\mathrm{sl},h}$ are the scattering limited velocities of electrons and holes. At 430 K, $v_{\mathrm{sl},e} = 7.45\ 10^6$ cm/s, and $v_{\mathrm{sl},h} = 6.86\ 10^6$ cm/s [6].

For a set of device parameters a numerical iteration [7] is used to adjust the critical field E_c, and then determine n and p by (2), such that the avalanche breakdown conditions [5] are fulfilled. The ionization rates used here were measured by Grant [10] from photomultiplication experiments. The avalanche width is defined [8] by $X_A \triangleq$ minimum of $(x_2 - x_1)$, where x_1 and x_2 are a set of the boundaries corresponding to hole-current changes of $0.95 I_{\mathrm{dc}}$. I_{dc} is the total dc current.

The breakdown voltage V_B and the voltage drop cross the avalanche region V_A are given as

$$V_B = \frac{1}{2} E_c W \tag{3}$$

$$V_A = -\frac{1}{2} x_1 \left(2E_c + \frac{qn}{\epsilon} x_1\right) + \frac{1}{2} x_2 \left(2E_c - \frac{qp}{\epsilon} x_2\right). \tag{4}$$

The dc to microwave generating efficiency [5] is calculated by

$$\eta = \frac{1}{\pi} \frac{V_B - V_A}{V_B}. \tag{5}$$

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TABLE I
Device Parameters for
p-n-Abrupt-Junction DD IMPATT Diodes

Device parameters	12 GHz	18 GHz	50 GHz
$n_2(\times 10^{15}\ cm^{-3})$	6.30	6.84	24.4
W_N (μm)	2.33	1.56	0.56
δ (μm)	0.05	0.05	0.03
X_{BN}(μm)	0.10	0.07	0.06
$Q_{BN}(\times 10^{12}\ cm^{-2})$	2.69	4.75	4.33
V_B (v.)	55.8	30.3	16.7
η (%)	25.4	24.3	19.0
ΔNM (dB)	42.5	32.5	26.1
ΔX_c (μm)	-0.017	-0.008	-0.007

Numerical calculations are performed for 12, 18, and 50 GHz. The resultant optimum device parameters are listed in Table I. These data are used as starting points for the high-efficiency DD design in next subsection.

B. The Low–High–Low Doping Profile Structure

For the low–high–low doping profile structure (Fig. 2), the electric-field distribution is

$$E(x) = \begin{cases} \frac{qn_2}{\epsilon}(W_N + x), & -W_N \le x \le -X_{BN} \\ \frac{qn_2}{\epsilon}(W_N - X_{BN}) + \frac{qn_1}{\epsilon}(X_{BN} + x), & -X_{BN} \le x \le -(X_{BN} - \delta) \\ E_c + \frac{qn_2}{\epsilon}x, & -(X_{BN} - \delta) \le x \le 0 \\ E_c - \frac{qp_2}{\epsilon}x, & 0 \le x \le X_{BP} - \delta \\ \frac{qp_2}{\epsilon}(W_P - X_{BP}) + \frac{qp_1}{\epsilon}(X_{BP} - x), & X_{BP} - \delta \le x \le X_{BP} \\ \frac{qp_2}{\epsilon}(W_P - x), & X_{BP} \le x \le W_P \end{cases} \quad (6)$$

where the critical field

$$E_c = \frac{qn_2}{\epsilon}(W_N - \delta) + \frac{qQ_{BN}}{\epsilon} = \frac{qp_2}{\epsilon}(W_P - \delta) + \frac{qQ_{BP}}{\epsilon} \quad (7)$$

and n_2 and p_2 are the n-type and p-type background doping concentrations; X_{BN} and X_{BP} are the n-type and p-type buried positions; δ is the buried width; Q_{BN} and Q_{BP} are the n-type and p-type buried quantities; W_N and W_P are n-type and p-type depletion widths, and are the same as those in the previous subsection; and $n_1 = Q_{BN}/\delta$ and $p_1 = Q_{BP}/\delta$.

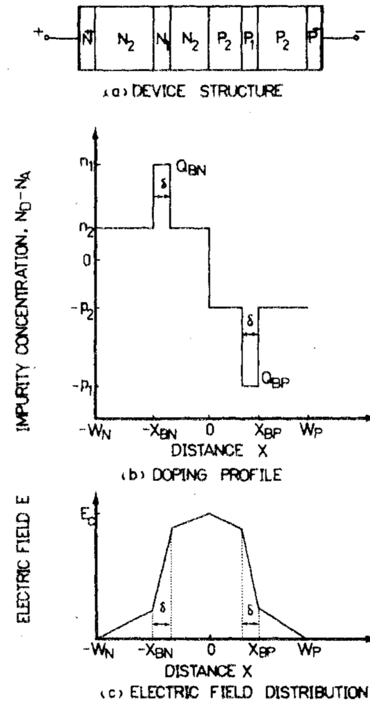

Fig. 2. Low–high–low doping-profile DD IMPATT diode.

TABLE II
Device Parameters for
Low–High–Low Doping Profile DD IMPATT Diodes

Device parameter	12 GHz	18 GHz	50 GHz
$n(\times 10^{15}\ cm^{-3})$	10.5	17.1	60.9
$p(\times 10^{15}\ cm^{-3})$	11.5	18.9	67.0
W_N (μm)	2.33	1.56	0.56
W_P (μm)	2.12	1.41	0.51
V_B (v.)	83.6	60.7	27.9
η (%)	13.3	13.0	10.5
ΔX_c^* (μm)	-0.16	-0.11	-0.03

*ΔX_c is the shift of avalanche center measured from the metallurgical junction, the negative sign indicated that the shift is toward the N-type side.

Efficiency calculations are carried out by a method similar to the one used in the previous subsection. The background doping concentration n_2 are varied as 20, 40, 60, and 80 percent of the doping concentration n of the p-n-abrupt-junction structure. The buried positions are related as $X_{BP} = X_{BN}/\lambda$, the buried quantities as $Q_{BP} = Q_{BN} + \delta n_2(\lambda - 1)$, and the background doping concentrations as $p_2 = \lambda n_2$, where $\lambda = v_{sl,e}/v_{sl,h}$. Typical numerical results for 18 GHz are plotted in Fig. 3. From this chart, it is clear that the efficiencies can be improved significantly if the background doping n_2 are in the range of 40–60 percent of n. The device parameters with the highest efficiencies obtained are summarized in Table II.

III. Noise Measure

The inherent noise in IMPATT diodes is mainly due to the statistical fluctuation in the avalanche process. The

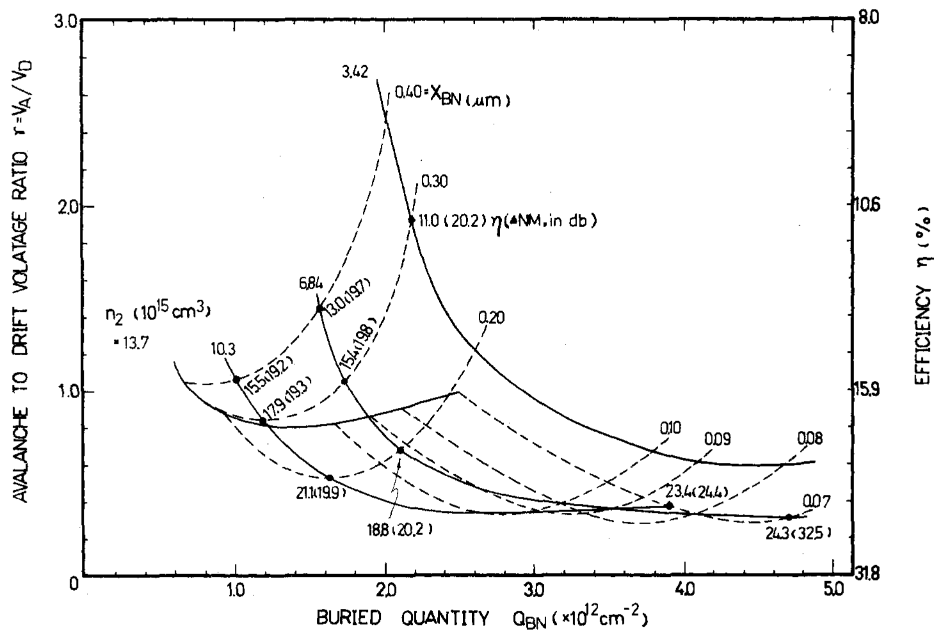

Fig. 3. Low–high–low doping-structure DD IMPATT diode at 18 GHz.

noise measure is the same as [9, eq. (4)], except that $\alpha' = \min\{d\alpha_n/dE, d\alpha_p/dE\}$ at the maximum field.

The incremental noise measure ΔNM in decibels of a low–high–low doping DD IMPATT diode as compared to their p-n-abrupt-junction DD counterpart is defined by

$$\Delta NM = NM\text{ (low–high–low doping DD)} - NM\text{(p-n-junction DD)}. \quad (8)$$

The results are presented in Table II and Fig. 3. The incremental noise measure ΔNM increases when efficiency increases. Therefore, there are tradeoffs between efficiency and noise.

IV. Discussions

Due to the shift of avalanche center, defined as the point X_c, where $I_P(X_c) = I_n(X_c)$, from the metallurgical junction toward the n-type side, the optimum depletion widths should be corrected to have the same drift lengths measured from the avalanche center for holes and electrons. For low-frequency and large-avalanche-width devices, the corrections are more important.

For device fabrication, there is considerable technological difficulty in realizing such an optimized design. However, for high-frequency devices, e.g., $f \geq 30$ GHz, ion implantation technique could be used to form the buried layers.

Since DD IMPATT diodes have more output power than their SD counterparts, the high-efficiency DD IMPATT diodes, proposed in this correspondence, are excellent candidates for high-power solid-state microwave oscillators.

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