Wide duty cycle range synchronous mirror delay designs

D. Sheng, C.-C. Chung and C.-Y. Lee

A wide duty cycle range and small static phase error synchronous mirror delay (SMD) for system-on-chip (SoC) applications is presented. The conventional SMD accepts only the pulsed clock signal and has large static phase error. The proposed SMD uses the edge-trigger mirror delay cell to enlarge the input duty cycle range and the blocking edge-trigger scheme to ensure functionality and performance. Moreover, phase error can be reduced by the proposed delay-matching structure and fine-tuning delay line with a high-resolution delay cell. Simulation results of SMD show that the input clock duty cycle range is from 20 to 80% and the worst static phase error under different process, voltage, and temperature conditions can achieve 18 ps at 400 MHz.

Introduction: As the operating frequency of electronic systems increases, de-skew clock circuits have been widely used for clock synchronisation in system-on-chip (SoC) applications. In contrast to phase-locked loop (PLL) and delay-locked loop (DLL), synchronous mirror delay (SMD) is more suitable for applications that require fast locking and low power consumption, because of its simple circuit structure [1–4]. However, the static phase error between the input and the output clock is hard to reduce in conventional SMD, owing to low delay resolution. Many SMDs have been proposed to reduce static error, including an interleaved type [2] and a phase blending type [3], but it is still hard to achieve high delay resolution and there is the penalty of increased circuit complexity and power consumption. Besides, conventional SMD accepts only the pulsed clock signal to ensure functionality, implying the input clock needs to be modulated if the duty cycle is not suitable. An arbitrary duty cycle SMD [4] can accept a wide input duty cycle range, but signal conflict may occur when the high frequency clock propagates through the long delay line. In this Letter, the proposed SMD utilises the edge-trigger mirror delay cell (EMDC) and blocking edge-trigger scheme to increase input duty cycle range and avoid signal conflict. Furthermore, the proposed fine-tuning delay line (FTDL) and delay-matching structure can reduce overall static phase error. As a result, the proposed SMD not only can achieve the wide input duty cycle range but also keep the small phase error at the same time.

Conventional SMD: Fig. 1 shows the schematic diagram of the conventional SMD. It consists of an input buffer (IB) with delay $Td1$, a clock driver (CD) with delay $Td2$, a forward delay line (FDL), a backward delay line (BDL), and a mirror control circuit (MCC). A pulsed clock propagates forward for the time of $Tck - Td1 - Td2$ through the FDL, and then propagates backward through the BDL as the opposite direction of FDL, where Tck is the input clock cycle time. As a result, total delay time is $Td1 + (Td1 + Td2) + (Tck - Td1 - Td2) + (Tck - Td1 - Td2) + Td2 = 2Tck$. So that the NAND type mirror delay cell (MDC) in MCC can perform accurately, the input clock should be modulated to a narrow-pulse clock to ensure the two inputs of MDC will not be overlapped at logic high within the first input clock cycle. The accuracy of phase alignment of SMD is dominated by the delay resolution of the delay cell in FDL and BDL. Besides, because the gate delay of MDC is neglected in the delay formula, it will further increase the phase error of SMD after two clock cycles.

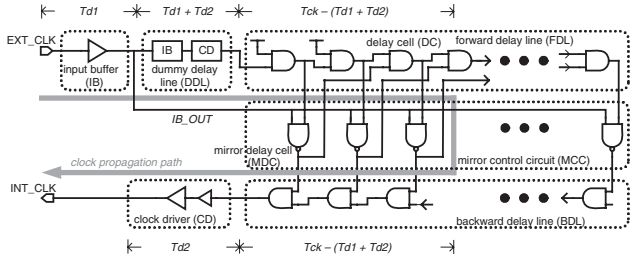

Fig. 1 *Architecture of conventional SMD*

Proposed SMD: Fig. 2*a* illustrates the architecture of the proposed SMD which consists of several major functional blocks: a dummy delay line (DDL), a FDL, a MCC, a BDL, a FTDL, a phase detector, and a timing controller, and the circuit of EMDC is shown in Fig. 2*b*. Compared with the conventional SMD, a DDL of the proposed delay-matching structure SMD contains an EMDC and a FTDL to compensate the delay of EMDC and FTDL. As a result, the total delay time is $Td1 + (Td1 + Td2 + Td3 + Td4) + (Tck - Td1 - Td2 - Td3 - Td4) + Td2 + (Tck - Td1 - Td2 - Td3 - Td4) + Td3 + Td4 = 2Tck$. The locking procedure is divided into coarse and fine locking. The coarse locking takes two clock cycles, the same as the conventional design, and the maximum phase error is the delay resolution of FDL and BDL. The remaining phase error is further reduced by FTDL controlled by a 3-bit fine-tuning control code (FTC). In the fine locking, the FTC is changed every two clock cycles by the timing controller based on UP/DN from the phase detector to control the delay of FTDL to align the phase between the external clock (EXT_CLK) and internal clock (INT_CLK). As a result, the entire locking procedure takes 10 clock cycles ($2 + 2 \times 4$). Typically, the delay resolution of FDL is one AND gate delay which is about several hundred picoseconds depending on the technology. To achieve high delay resolution, the proposed FTDL employs a digitally-controlled varactor (DCV) the gate capacitance of which can be changed slightly by the FTC to change the delay of FTDL under different output loading of the driving buffer as shown in Fig. 3 [5]. As a result, the overall delay resolution of SMD can be improved from several hundred picoseconds to 10 picoseconds. To increase input duty cycle range, the proposed SMD utilises the EMDC to detect the level changing of the outputs of the successive delay cells in FDL [4]. However, based on the system requirements, the length of FDL and BDL may need to increase to achieve the wide operating frequency range. But, it will induce more than one outputs of the EMDCs at logic low as the high-frequency clock propagates through the long FDL, implying SMD operation is unstable, as shown in Fig. 4*a*. The proposed blocking edge-trigger scheme uses the blocking signal (BLK), which is set to low level at the second rising edge of IB_OUT to block the clock propagation in FDL to avoid signal conflict in MCC and ensure SMD functionality as shown in Fig. 4*b*.

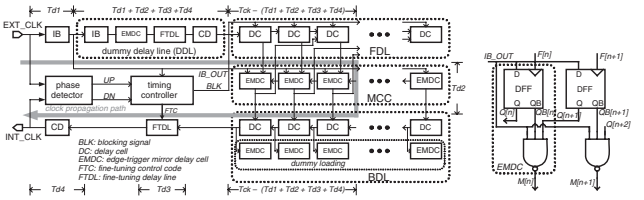

Fig. 2 *Architecture of proposed SMD and circuit of EMDC*

a Architecture of proposed SMD
b Circuit of EMDC

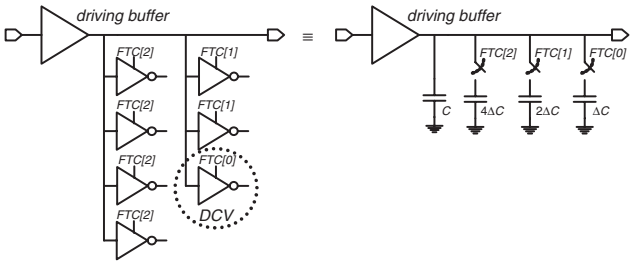

Fig. 3 *Block diagram and equivalent circuit of DCV*

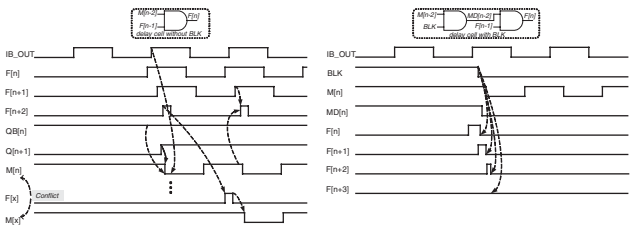

Fig. 4 *Timing waveform without and with blocking scheme*

a Without blocking scheme
b With blocking scheme

Implementation and simulation results: A test chip of the proposed SMD was in 0.18 μm CMOS process (Fig. 5 shows the chip microphotograph). The proposed design is verified by post-layout simulation using HSPICE. Fig. 6*a* shows the entire locking process takes 10 clock cycles, and the total propagation delay of SMD is adjusted by the FTC every two clock cycles, making the phase error reduce to 15 ps at 400 MHz. Table 1 lists the verification results of phase error under different PVT conditions and input clock frequencies. The proposed SMD can accept a wide input duty cycle from 20 to 80% at different input clock frequencies, as shown in Fig. 6*b*. The performance characteristics of the proposed SMD are summarised in Table 2.

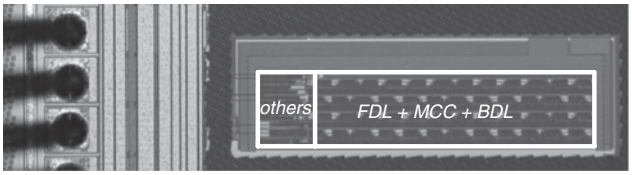

Fig. 5 *Microphotograph of SMD test chip*

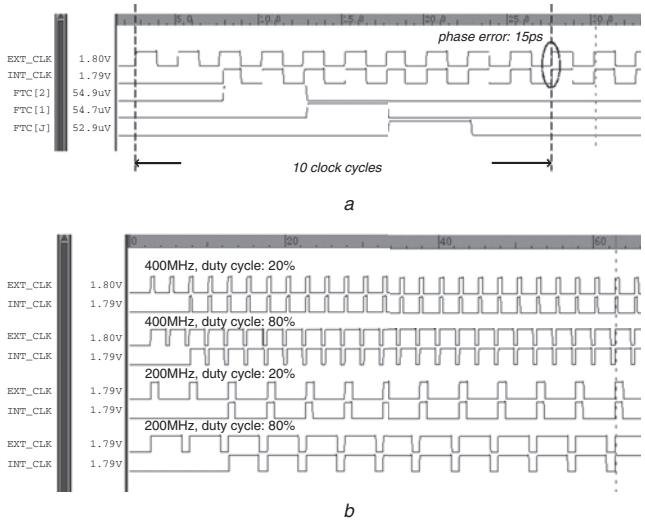

Fig. 6 *Timing diagram of proposed SMD and acceptable input duty cycle under different frequencies*

a Timing diagram
b Acceptable input duty cycle

Table 1: Phase error under different PVT conditions

	SS, 1.62 V, 125°	TT, 1.8 V, 25°	FF, 1.98 V, −40°
200 MHz	6 ps	11 ps	16 ps
400 MHz	16 ps	15 ps	18 ps

Table 2: Performance summary

Process	0.18 μm CMOS
Supply voltage (V)	1.8
Operation range (MHz)	200–400
Input duty cycle range (%)	20–80
Delay resolution (ps)	10
Phase error (ps)	18
Lock time (clock cycles)	10
Power consumption (mW)	8.7 at 400 MHz
Area (mm^2)	0.08

Conclusion: The performance and application scope of the conventional SMD are limited by low accuracy phase alignment and narrow-pulse clock demand. In this Letter, three important design concepts of the proposed SMD are proposed: a high-resolution delay line, a delay-matching structure, and a blocking edge-trigger scheme. The proposed high-resolution delay line and delay-matching structure reduce phase error between the external and internal clock, and the proposed blocking edge-trigger scheme extends input duty cycle range without delay line length limitation. As a result, the proposed SMD can achieve a wide duty cycle range and keep small static phase error compared with conventional designs, making it suitable for clock synchronisation in SoC applications.

29 October 2009
doi: 10.1049/el.2010.3047

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