The proximity of the strain induced effect to improve the electron mobility in a silicon-carbon source-drain structure of n-channel metal-oxide-semiconductor field-effect transistors

E. R. Hsieh and Steve S. Chung

Articles you may be interested in

Rare-earth oxide/TiN gate stacks on high mobility strained silicon on insulator for fully depleted metal-oxide-semiconductor field-effect transistors
J. Vac. Sci. Technol. B **29**, 01A903 (2011); 10.1116/1.3533760

Carrier transport in strained N-channel field effect transistors with channel proximate silicon-carbon source/drain stressors
Appl. Phys. Lett. **97**, 032111 (2010); 10.1063/1.3465661

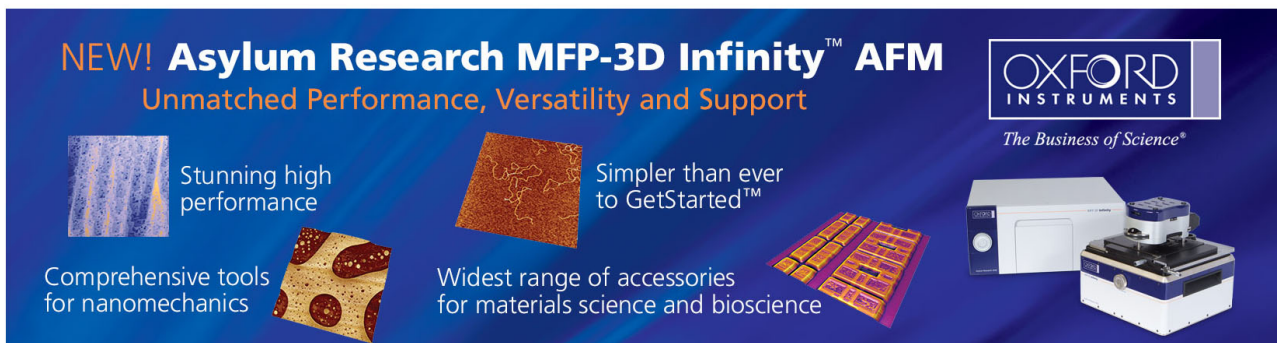Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors
J. Appl. Phys. **97**, 011101 (2005); 10.1063/1.1819976

Secondary ion mass spectrometry characterization of source/drain junctions for strained silicon channel metal–oxide–semiconductor field-effect transistors
J. Vac. Sci. Technol. B **22**, 327 (2004); 10.1116/1.1640659

Electron mobility enhancement in strained SiGe vertical n-type metal–oxide–semiconductor field-effect transistors
Appl. Phys. Lett. **78**, 377 (2001); 10.1063/1.1342038

The proximity of the strain induced effect to improve the electron mobility in a silicon-carbon source-drain structure of n-channel metal-oxide-semiconductor field-effect transistors

E. R. Hsieh and Steve S. Chung[a)]

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

The source/drain in an n-channel metal-oxide-semiconductor field-effect transistor (nMOSFET) with solid phase epitaxial (SPE) implanted Si:C *before* the spacer formation is proposed. Compared to the conventional nMOSFET with SPE implanted Si:C *after* the spacer formation, it brings in proximity to the device channel and shows great improvement of electron mobility via the *stronger* tensile strain effect. Experimental measurements showed that the electron mobility in the proposed process is increased by 105% over that of the control devices. At a gate length of 40 nm, an increase of more than 67% for the drain current, comparing to those of the conventional Si:C source/drain nMOSFET, has been achieved. © *2010 American Institute of Physics.* [doi:10.1063/1.3340926]

In order to extend the scaling of complementary metal-oxide semiconductor (CMOS) transistors while keeping good performance,[1,2] the enhancement of carrier mobility making utilization of strain-induced effect is one of the promising approaches.[3] In more recent years, different techniques have been employed for n- and p-channel metal-oxide-semiconductor field-effect transistor (nMOSFET/pMOSFET), with an attempt to provide flexible tuning of the strain effects in terms of design and manufacturing purposes.[4–10] In p-MOSFET, hole mobility can be boosted by the usage of silicon-germanium (SiGe) stressor in the source/drain (S/D),[4–7] which induces uniaxial compressive-strain effect into the channel, via the lattice-mismatch induced strain between the interface of SiGe S/D and silicon channel regions. On the other hand, in nMOSFET, silicon-carbon (Si:C) in S/D with an induced tensile-strain effect becomes feasible as a counter part of pMOSFET in the CMOS structures.[4,8–10]

More recently, there are three mainstream technologies to adopt the carbon-dopant to form the Si:C in the S/D, including solid phase epitaxy (SPE),[11] SPE implantation,[12,13] and *in situ* doping.[14] The electron mobility, μ_{eff}, enhancement based on embedded Si:C in the S/D structure is highly dependent on the carbon concentration (C%) of Si:C and the strength of tensile strain in the channel. As a result of the low solid dissolubility of carbon in silicon, many groups paid a lot of efforts on how to increase C% of Si:C,[11–14] however, the improvement would be limited by the carbon out-diffusion since it makes the device reliability worse for a high dopant.[8] In the aforementioned processes, SPE process shows lower substitutional carbon concentration (e.g., about ~1%).[2] SPE implantation shows higher C% of 1.65%;[9] in addition, the position and concentration of C% in this process are more adjustable than the others. However, the annealing steps are involved after carbon implantation, which could release the tensile strain in the channel and adversely degrade the performance. In order to avoid this strain-released effect, *in situ* doping process was demonstrated.[13] It

shows C% of 2.1%, but the consequence is the concern of carbon out-diffusion.

In this work, by using the SPE implantation, Si:C in the S/D extension region was prepared. Before spacer formation, S/D region was shallowly recessed with dry etching. Then, Si:C epilayer was selectively formed in the S/D region with 1.15×10^{15} cm^{-2} of carbon, implanted together with Arsenic doping. Si:C was completed by using a low temperature (950 °C) SPE process, and meanwhile, dopant was also activated at the same SPE step. Since SPE process is a low temperature process, the lateral diffusion of S/D extension during anneal is very limited comparing to the conventional activation process, in which the latter tends to give longer lateral diffusion as a result of high temperature thermal budget using either laser spike anneal or rapid thermal process that has been commonly used for the annealing of S/D. The substitutional carbon concentration (C%) of Si:C, 1.1%, is examined by the x-ray diffraction (XRD) spectrum as shown in Fig. 1(a), in which the lower concentration (1.1%) is
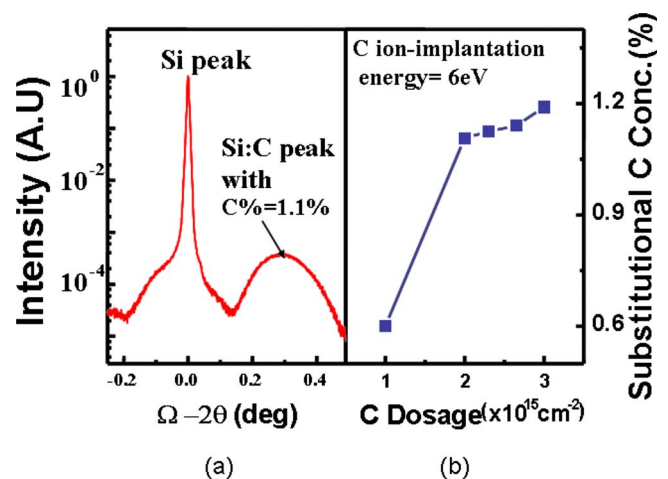

FIG. 1. (Color online) (a) The XRD measurement of the Si:C films. The effective substitutional C dopant concentration is 1.1%. (b) The ion-implanted C condition: C%=1.1% at C dosage=2×10^{15} cm^{-2} and energy =6 keV. Note that the substitutional C dopant tends to saturate with increasing carbon dosage.

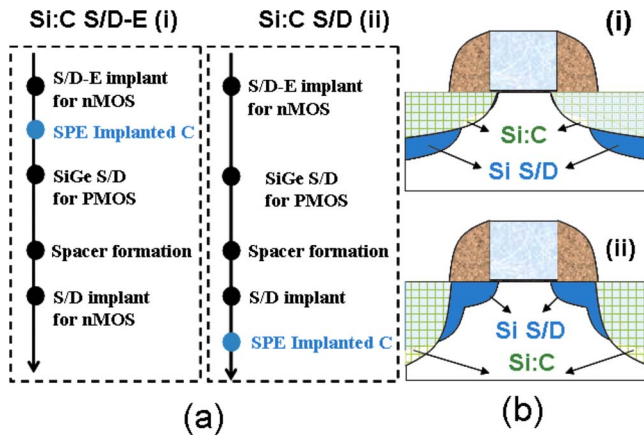[a)]Electronic mail: schung@cc.nctu.edu.tw.

FIG. 2. (Color online) Key process sequences for the fabrication of strained nMOS devices. (a) New process (i) SPE implanted C before the spacer formation for nMOSFET with Si:C in the S/D extension region, and conventional process (ii) SPE implanted C after the spacer formation for nMOSFET with SiC in S/D region. (b) The cross sectional views for process (i) and process (ii) in (a). The differences are the formation of SiC before and after the spacer formation.
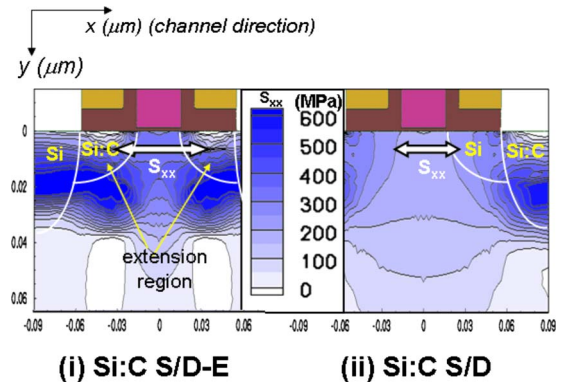

FIG. 3. (Color online) The simulated longitudinal stress (S_{xx}) along the channel direction, for (i) Si:C S/D-E devices and (ii) Si:C S/D process. It can be clearly seen that the intensity of the strain in (i) Si:C S/D-E process is higher and more close to the channel (darker area) in comparison to the conventional Si:C S/D ones (ii).

resulting from the annealing steps after carbon ion-implantation. To improve the C% of Si:C and to achieve abrupt carbon profile, low temperature and ultrashort annealing temperatures were employed (temperature=950 °C and time <1 ms). The condition of substitutional carbon concentrations dependent on ion-implanted carbon impurities is also demonstrated in Fig. 1(b). It was observed that the substitutional carbon concentration tends to saturate when ion-implanted carbon dosage is larger than 2×10^{15} cm^{-2}, as a result of the very low solid dissolubility of carbon in the silicon. As a consequence, we faced the difficulties to increase C% further because when annealing temperature is raised to increase C%, the tensile strain will be released; when the carbon dosage is increased, the C% is easy to be saturated. Therefore, it is hard to increase the dopants (C%) of Si:C further.

To enhance the tensile-strain effect into the channel and to avoid the dilemma as described above, the SPE implantation of the carbon impurity is introduced into the S/D extension region (S/D-E) instead of that in the S/D region. Figure 2(a) shows major steps of the fabrication process. Figure 2(b) shows the cross sections with two different structures, namely, (i) Si:C in the S/D extension region, and (ii) Si:C in the S/D region. First, active regions with threshold-voltage (V_{th}) tuning are defined, and then polysilicon gate, oxynitride gate insulator, S/D extension implantation, silicon nitride spacer, and S/D implantation are formed in sequence. For both processes, carbon impurity ion-implantation and annealing steps are utilized to form Si:C, since the SPE implantation could be integrated easily into S/D-E (or S/D) before (or after) the spacer formation. The processing steps (i) in Fig. 1(a) provide the modified SPE implantation process with Si:C stressor in the S/D-E region, and steps (ii) are the standard[12] SPE implantation process with Si:C stressor in the S/D region.

The strength of the strain in the channel is very sensitive to the geometry effect and the manufacturing process, so the simulation needs to consider these factors. The simulation work was performed by Synopsys Sentaurus TCAD (Technology Computer Aided Design) software,[15] in which those stress mechanisms associated with the materials, i.e., stresses induced by the growth of materials, densification, thermal mismatch, and lattice mismatch, were used. For a Si:C S/D uniaxial stressor in n-channel transistor, S_{xx} is required to be tensile strain to enhance the electron mobility.[1,4] Figures 3(a) and 3(b) show the simulated profiles of longitudinal tensile stress (S_{xx}) for the conventional Si:C in S/D region (Si:C S/D device) and the Si:C in S/D extension region (Si:C S/D-E device). These simulated results considered all device integration processes (including thermal activation processes) and took into account the integration between carbon and S/D (or S/D-E) dopants. The strength of S_{xx} is larger in the proximity of the stressor and decreases far away from the stressor along the channel direction; thus, the smallest intensity exists in the middle of the channel. It is because the lattice-mismatch on the interface of Si:C and silicon will release the strain which decays with the increasing distance. As a result, in order to enlarge the magnitude of S_{xx}, we have to bring the proximity of strain effect through the stressor more close to the channel. For the comparison in Fig. 3, it can be seen that S_{xx} for the Si:C S/D-E process introduces strain effect more close to the channel (the darker area showing a higher strain effect), comparing to the conventional Si:C S/D ones. Additionally, the substitutional carbon concentration (C%) of Si:C S/D-E process is higher than that of Si:C S/D process thanks to a lighter dopant interference in the area below the S/D extension junction, where the concentration of S/D dopant is low.

Figure 4(a) shows the calculated effective mobility, μ_{eff}, versus the effective electric field characteristics for the Si:C S/D-E device, Si:C S/D device, and the control device, respectively. It reveals a fairly large improvement in the mobility enhancement of 105% for the Si:C S/D-E device in comparison to that of the control device. The larger the strength of tensile-strain in channel is, the more enhancement of mobility for the carriers in the channel becomes. This proposed structure has the merit of inducing more strain to the channel while keeping a low C% of Si:C effectively. In short, with the improvement of longitudinal tensile stress (S_{xx}) in the channel, the effective mass and the scattering events of electrons have been reduced, which gives rise to a higher effective mobility in Si:C S/D-E structures. Results in Fig. 4(b) show the I_{DS}-V_{DS} characteristics of nMOSFET with a gate length of 40 nm for both Si:C S/D-E device, SiC S/D device, and the control device at the same operating bias.
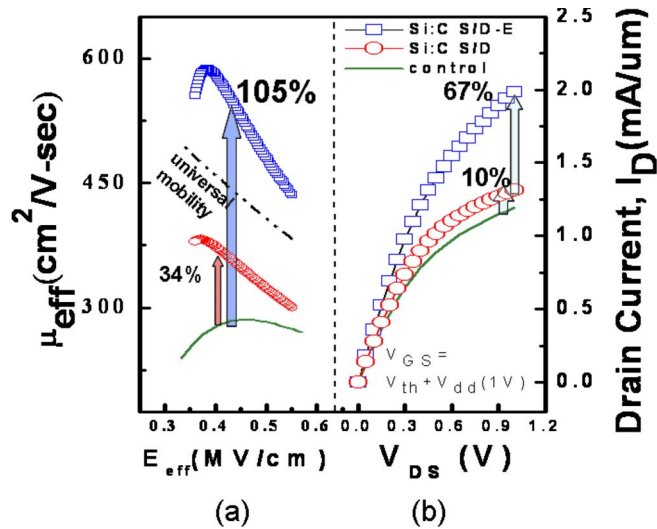
FIG. 4. (Color online) (a) Plot of the effective mobility vs effective electric field which shows an increase of 105% for SiC S/D-E device over the control device. (b) Plot of I_D vs V_{GS} for gate length=40 nm, showing the enhancement of driving currents with over 67% increase in Si:C S/D-E device over the control device, while conventional Si:C S/D just shows an increase of 10%.

$V_{DD}=1V+V_{th}$. The Si:C S/D-E device shows $I_{D,sat}$ (at $V_{DS}=V_{DD}+V_{th}$) improvement of 67% over that of the control device.

In conclusion, to have a trade-off between the carbon out-diffusion and the strength of the tensile strain in the channel for a certain design of Si:C S/D structure, the use of Si:C underneath the gate-drain overlap region is an excellent candidate for fabricating high electron mobility nMOSFETs. The induced tensile-strain has been in proximity to the channel which results in a higher electron mobility. Experimental measurements showed that the electron mobility in the proposed process is increased by ~105% over that of the control devices, and the I_{DS}-V_{DS} characteristics show the benefit of 67% over that of the control devices at the same operating bias. In addition, the Si:C S/D-E process still keeps low C%, which can reduce thermal budget and prevent the carbon out diffusion which might hurt the device reliability.

[1]S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, IEEE Trans. Electron Devices **53**, 1010 (2006).
[2]S. E. Thompson and S. Parthasarathy, Mater. Today **9**, 20 (2006).
[3]Y. Sun, S. E. Thompson, and T. Nishida, J. Appl. Phys. **101**, 104503 (2007).
[4]K.-W. Ang, K.-J. Chui, V. Bliznetsov, C.-H. Tung, A. Du, N. Balasubramaniam, G. Samudra, M. F. Li, and Y.-C. Yeo, Appl. Phys. Lett. **86**, 093102 (2005).
[5]P. R. Chidambaram, C. Bowen, S. Chakravathi, C. Machala, and R. Wise, IEEE Trans. Electron Devices **53**, 944 (2006).
[6]K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson, and M. Bohr, Dig. Tech. Pap. - Symp. VLSI Technol. **2004**, 50.
[7]S. S. Chung, D. C. Huang, Y. J. Tsai, C. S. Lai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, Tech. Dig. - Int. Electron Devices Meet. **2006**, 325.
[8]S. S. Chung, E. R. Hsieh, D. C. Huang, C. S. Lai, C. H. Tsai, P. W. Liu, Y. H. Lin, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, Tech. Dig. - Int. Electron Devices Meet. **2008**, 435.
[9]K.-W. Ang, K.-J. Chui, V. Bliznetsov, A. Du, N. Balasubramaniam, G. Samudra, M. F. Li, and Y.-C. Yeo, Tech. Dig. - Int. Electron Devices Meet. **2004**, 1069.
[10]S. S. Chung, E. R. Hsieh, P. W. Liu, W. T. Chiang, S. H. Tsai, T. L. Tsai, R. M. Huang, C. H. Tsai, W. Y. Teng, C. I. Li, T. F. Kuo, Y. R. Wang, C. L. Yang, C. T. Tsai, G. H. Ma, S. C. Chien, and S. W. Sun, Dig. Tech. Pap. - Symp. VLSI Technol. **2009**, 158.
[11]Y.-C. Liu, O. Gluschenkov, J.-H. Li, A. Madan, A. Ozcan, B. Kim, T. Dyer, A. Chakravarti, K. Chan, C. Lavoie, I. Popova, T. Pinto, N. Rovedo, Z. Luo, R. Loesing, W. Henson, and K. Rim, Dig. Tech. Pap. - Symp. VLSI Technol. **2007**, 44.
[12]Z. Ren, G. Pei, J. Li, B. Yang, R. Takalkat, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, J. Miller, A. Dube, L. Black, J. W. Weijtmans, B. Yang, E. Harley, A. Chakravarti, T. Kanarsky, R. Pal, I. Lauer, D.-G. Park, and D. Sadana, Dig. Tech. Pap. - Symp. VLSI Technol. **2008**, 172.
[13]B. Yang, R. Takalkar, Z. Ren, L. Black, A. Dube, J. W. Weijtmans, J. Li, J. B. Johnson, J. Faltermeier, A. Madan, Z. Zhu, A. Turansky, G. Xia, A. Chakravarti, R. Pal, K. Chan, A. Reznicek, T. N. Adam, B. Yang, J. P. de Souza, E. C. T. Hariey, B. Greene, A. Gehring, M. Cai, D. Aime, S. Sun, H. Meer, J. Holt, D. Theodore, S. Zollner, P. Grudowski, D. Sadana, D. G. Park, D. Mocuta, D. Schepis, E. Maciejewski, S. Luning, J. Pellerin, and E. Leobandung, Tech. Dig. - Int. Electron Devices Meet. **2008**, 51.
[14]H.-S. Wong, K.-W. Ang, L. Chan, K.-M. Hoe, C.-H. Tung, N. Balasubramanian, D. Weeks, M. Bauer, J. Spear, S. G. Thomas, G. Samudra, and Y.-C. Yeo, IEEE Electron Device Lett. **29**, 460 (2008).
[15]TCAD Sentaurus user manual (Synopsys, Version C, 2009).