# Investigation and Analysis of Mismatching Properties for Nanoscale Strained MOSFETs

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*Abstract*—This paper investigates and analyzes the matching properties of nanoscale strained MOSFETs under various bias conditions. Through a comprehensive comparison between coprocessed strained and unstrained PMOSFETs, the impact of process-induced uniaxial strain on the matching performance of MOS devices has been assessed and analyzed. Our examination indicates that, in the low-gate-voltage-overdrive ($|V_{gst}|$) regime, the normalized drain current mismatch ($\sigma(\Delta I_{\rm d})/I_{\rm d}$) of the strained device is almost the same as that of the unstrained one at a given transconductance to drain current ratio ($g_m/I_{\rm d}$). In the high $|V_{gst}|$ linear regime, the $\sigma(\Delta I_{\rm d})/I_{\rm d}$ for the strained device is smaller than that of the unstrained one because of its smaller normalized current factor mismatch. In the high $|V_{gst}|$ saturation regime, the improvement in the $\sigma(\Delta I_{\rm d})/I_{\rm d}$ for the strained device is further enhanced because of the reduced critical electric field at which the carrier velocity becomes saturated.

*Index Terms*—Fluctuation, mismatch, transconductance to drain current ratio, uniaxial strained silicon, variation.
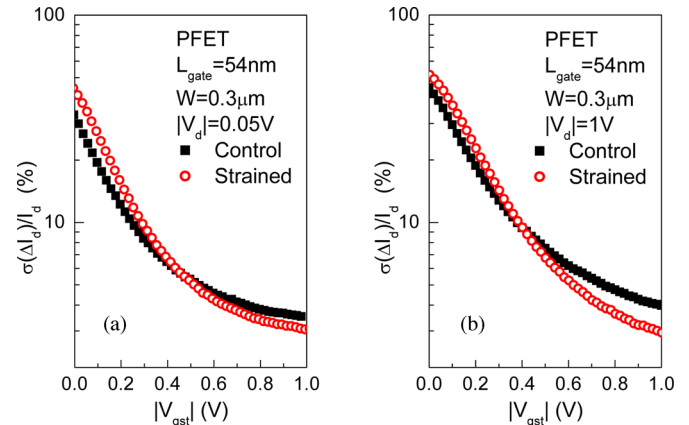


Fig. 1. Comparison of $\sigma(\Delta I_{\rm d})/I_{\rm d}$ versus $|V_{gst}|$ for strained and unstrained devices at (a) $|V_{\rm d}| = 0.05$ V, and (b) $|V_{\rm d}| = 1$ V, respectively.

## I. Introduction

**W**ITH the scaling of device dimensions [1], [2], the device mismatching that stems from stochastic fluctuations is becoming a concern for nanoscale MOSFETs [1]–[4]. Device mismatch may limit the achievable accuracy in analog applications such as multiplexed analog systems, digital-to-analog converters, reference source, and the synchronous RAM (SRAM), etc. [1]–[4]. Since strained silicon is widely used in state-of-the-art CMOS technologies to enable the mobility scaling [1], [7]–[15], a comprehensive study regarding the impact of strain on device mismatch is needed. Through a comparison between strained and unstrained devices, this study investigates and analyzes the mismatching properties of nanoscale strained MOSFETs.

This paper is organized as follows. Section II introduces the devices and measurement used in this study. In Sections III and IV, we examine the impact of strain on the matching performance for devices biased in the low-gate-voltage-overdrive regime and high-gate-voltage-overdrive regime, respectively. Section V draws the conclusion.

## II. Devices and Measurement

The devices used in this study were fabricated by state-of-the-art process-induced uniaxial strained-silicon technology. Coprocessed strained and unstrained PMOSFETs were investigated [16] (with channel direction $\langle 1\,1\,0 \rangle$ on $(1\,0\,0)$ silicon substrate). The strained device features compressive uniaxial contact etch stop layer (CESL) and SiGe source/drain. For the transistors with gate length $L_{\rm gate} = 54$ nm, the saturated drain current ($I_{\rm dsat}$) of the strained device is improved more than 100% as compared with its control counterpart [16].

The mismatching properties of strained and unstrained devices were measured from identical devices in a matching pair configuration on 60 dies. Statistics on the mismatch in drain current ($\Delta I_{\rm d}$), threshold voltage, and current factor ($\Delta \beta$) in the linear and saturation regions were analyzed. The threshold voltage ($V_{\rm th}$) was measured by the constant-current method and $\beta$ was determined by the maximum slope method [17].

## III. Matching Performance in the Low $|V_{gst}|$ Regime

Fig. 1(a) and (b) shows the $V_g$ dependence of the extracted standard deviations of normalized drain current mismatch ($\sigma(\Delta I_{\rm d})/I_{\rm d}$) for strained and control devices with $L_{\rm gate} = 54$ nm and gate width ($W$) $= 0.3$ $\mu$m in the linear region ($|V_{\rm d}| = 0.05$ V) and saturation region ($|V_{\rm d}| = 1$ V), respectively. It can be seen that, for gate voltage overdrive ($|V_{gst}| = |V_g| - |V_{\rm th}|$) below 0.4 V, the $\sigma(\Delta I_{\rm d})/I_{\rm d}$ of the strained device is larger than that of the unstrained one. On the other hand, for $|V_{gst}|$ above 0.4 V, the $\sigma(\Delta I_{\rm d})/I_{\rm d}$ of the strained device is smaller than that of the unstrained one.
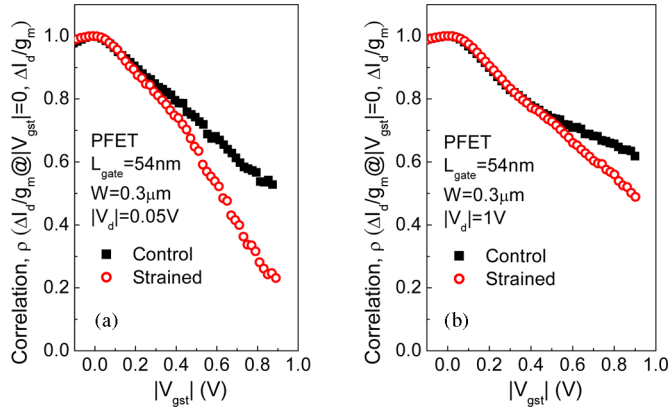
Fig. 2.  Correlation between $(\Delta I_\mathrm{d})/g_m$ at $|V_{gst}| = 0$ and $(\Delta I_\mathrm{d})/g_m$ at other $|V_{gst}|$ at (a) $|V_\mathrm{d}| = 0.05$ V, and (b) $|V_\mathrm{d}| = 1$ V, respectively.



Fig. 4.  $g_m/I_\mathrm{d}$ for the strained device is enhanced in the low $|V_{gst}|$ regime at $|V_\mathrm{d}| = 0.05$ and 1 V.



Fig. 3.  Pelgrom plot of $\sigma(\Delta I_\mathrm{d})/I_\mathrm{d}$ showing larger $(\Delta I_\mathrm{d})/I_\mathrm{d}$ for the strained device at $|V_{gst}| = 0.2$ V with $|V_\mathrm{d}| = 0.05$ and 1 V.



Fig. 5.  Extracted carrier mobility versus $|V_{gst}|$ showing that the strained device has larger $V_g$ sensitivity in the low $|V_{gst}|$ regime.

The normalized drain current mismatch in the low $|V_{gst}|$ regime (e.g., $|V_{gst}| < 0.4$ V) is dominated by the threshold voltage mismatch [17], and can be expressed as [18]

$$\frac{\Delta I_\mathrm{d}}{I_\mathrm{d}} = -\frac{g_m}{I_\mathrm{d}} \times (\Delta V_\mathrm{th}) \qquad (1)$$

where $g_m$ is the transconductance. To verify the relevance of $\Delta V_\mathrm{th}$ to $\Delta I_\mathrm{d}/I_\mathrm{d}$ [17], (1) can be rewritten as $(\Delta I_\mathrm{d})/g_m = -\Delta V_\mathrm{th}$ and the correlation ($\rho$) between $(\Delta I_\mathrm{d})/g_m$ at $|V_{gst}| = 0$ and $(\Delta I_\mathrm{d})/g_m$ at other $|V_{gst}|$ is shown in Fig. 2. It can be seen from Fig. 2 that the correlation lies between 70% and 100% for both strained and control devices for $|V_{gst}| < 0.4$ V. This ensures that the threshold voltage mismatch is the dominant mechanism that determines the normalized drain current mismatch in the low $|V_{gst}|$ linear regime.

Fig. 3 shows the Pelgrom plot of $\sigma(\Delta I_\mathrm{d})/I_\mathrm{d}$ at $|V_{gst}| = 0.2$ V. The geometries of the devices in Fig. 3 are $W/L_\mathrm{gate} = 1\,\mu\mathrm{m}/54$ nm, $0.3\,\mu\mathrm{m}/54$ nm, and $0.12\,\mu\mathrm{m}/54$ nm. Note that the $L_\mathrm{gate}$ of the strained device needs to be the same in order to keep similar strain in the channel. This is because the channel strain is gate-length dependent in process-induced strain silicon
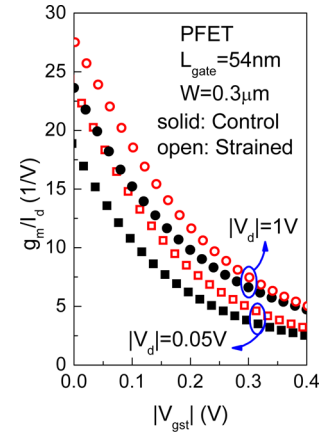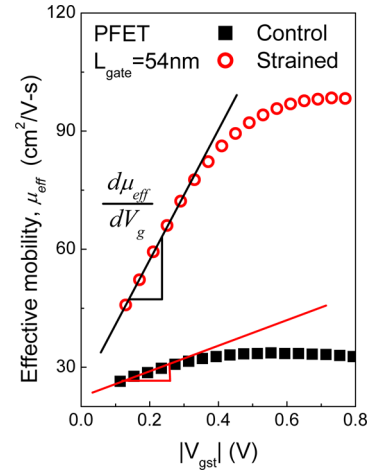
devices [10]–[13]. From Fig. 3, it can be seen that $\sigma(\Delta I_\mathrm{d})/I_\mathrm{d}$ of the strained device is larger than that of the control device.

Fig. 4 shows that the $g_m/I_\mathrm{d}$ of the strained device is significantly larger than the control device. It is the enhanced $g_m/I_\mathrm{d}$ that increases the drain current mismatch in the low $|V_{gst}|$ regime [see (1)]. The $g_m/I_\mathrm{d}$ in the linear region and saturation region can be modeled by (2) and (3), respectively, derived from Berkeley Short-channel IGFET Model (BSIM) [19]:

$$\frac{g_m}{I_\mathrm{d}} = \frac{1}{V_{gst} - V_\mathrm{d}/2} + \frac{\partial \mu_\mathrm{eff}/\partial V_g}{\mu_\mathrm{eff}} \qquad (2)$$

$$\frac{g_m}{I_\mathrm{d}} = \frac{1}{V_{gst}}\left[\frac{V_{gst} + 2E_\mathrm{sat}L_\mathrm{eff}}{V_{gst} + E_\mathrm{sat}L_\mathrm{eff}}\right] + \frac{E_\mathrm{sat}L_\mathrm{eff}}{V_{gst} + E_\mathrm{sat}L_\mathrm{eff}}\frac{\partial \mu_\mathrm{eff}/\partial V_g}{\mu_\mathrm{eff}} \qquad (3)$$

where $L_\mathrm{eff}$ and $E_\mathrm{sat}$ denote the effective channel length and the critical electric field at which the carrier velocity becomes saturated, respectively. The $g_m/I_\mathrm{d}$ for the strained device is higher than its control counterpart because of the higher $V_g$ sensitivity of carrier mobility ($\mu_\mathrm{eff}$) present in the strained device, as shown in Fig. 5. It can be seen from Fig. 5 that $\mu_\mathrm{eff}$ increases with $V_g$ in
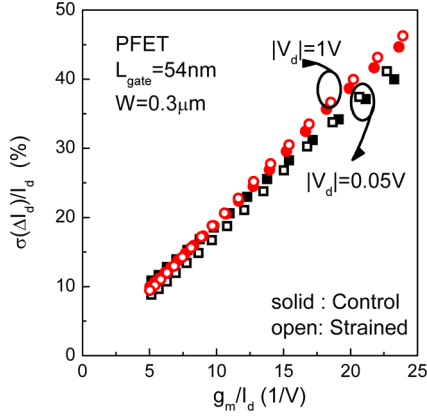
Fig. 6.    $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ versus $g_m/I_{\mathrm{d}}$ for strained and unstrained devices.
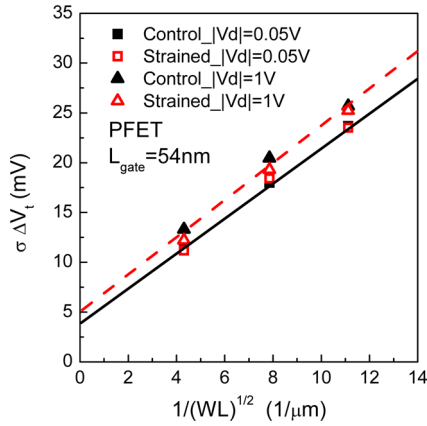


Fig. 7.    Pelgrom plot of $\Delta V_{\mathrm{th}}$ showing nearly identical $\Delta V_{\mathrm{th}}$ for the strained and unstrained devices.



Fig. 8.    Pelgrom plot of $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ shows smaller $(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained device at $|V_{gst}| = 0.8$ V with (a) $|V_{\mathrm{d}}| = 0.05$ V, and (b) $|V_{\mathrm{d}}| = 1$ V, respectively.



Fig. 9.    $\sigma^2(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ can be modeled well by (5).

the low $|V_{gst}|$ regime. This is because in the low $|V_{gst}|$ regime, the mobility is mainly determined by Coulombic scattering [20]. The mobile carrier screening makes $\mu_{\mathrm{eff}}$ increases with $V_g$. The larger slope of the mobility for the strained device is responsible for the higher $g_m/I_{\mathrm{d}}$, as observed in Fig. 4.

Nevertheless, for a given $g_m/I_{\mathrm{d}}$, the $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained and control devices are nearly identical, as shown in Fig. 6. In other words, the $V_{\mathrm{th}}$ mismatch for the strained and control devices are nearly the same, as demonstrated in Fig. 7. Note that a linear dependence of $\sigma(\Delta V_{\mathrm{th}})$ on $1/(W L_{\mathrm{gate}})^{-1/2}$ in the Pelgrom plot indicates a random-dopant-fluctuations origin of $V_{\mathrm{th}}$ mismatch [21]. Moreover, the increase of $\sigma(\Delta V_{\mathrm{th}})$ with increasing $|V_{\mathrm{d}}|$ due to drain-induced barrier lowering (DIBL) can also be observed in Fig. 7 [22].

## IV. MATCHING PERFORMANCE IN THE HIGH $|V_{gst}|$ REGIME

In the high $|V_{gst}|$ regime (e.g., $|V_{gst}| > 0.4$ V), Fig. 1(a) and (b) shows smaller $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained device as compared with the unstrained one. The Pelgrom plot of $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ at $|V_{gst}| = 0.8$ V in Fig. 8 also shows a smaller $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained device. Furthermore, the correlation between $(\Delta I_{\mathrm{d}})/g_m$ at $V_{gst} = 0$ and $(\Delta I_{\mathrm{d}})/g_m$ at other $V_{gst}$ shown in Fig. 2 implies that $\Delta V_{\mathrm{th}}$ is not the only dominant mechanism

in the high $|V_{gst}|$ regime. In other words, the current factor mismatch ($\Delta\beta$) should be included in the following normalized drain current mismatch expression as [6]:

$$\frac{\Delta I_{\mathrm{d}}}{I_{\mathrm{d}}} = -\frac{g_m}{I_{\mathrm{d}}} \times (\Delta V_{\mathrm{th}}) + \frac{\Delta\beta}{\beta}. \qquad (4)$$

The variance of the normalized drain current mismatch is [23], [24]:

$$\sigma^2\left(\frac{\Delta I_{\mathrm{d}}}{I_{\mathrm{d}}}\right) = \left(\frac{g_m}{I_{\mathrm{d}}}\right)^2 \times \sigma^2(\Delta V_{\mathrm{th}}) + \sigma^2\left(\frac{\Delta\beta}{\beta}\right). \qquad (5)$$

### A. Linear Region

Fig. 9 shows a comparison of the measured $\sigma^2(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ with (5) at $|V_{\mathrm{d}}| = 0.05$ V. It can be seen that the $\sigma^2(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ can be modeled well by considering the contribution from both $\Delta V_{\mathrm{th}}$ and $\Delta\beta$. Moreover, Fig. 9 indicates that the normalized linear
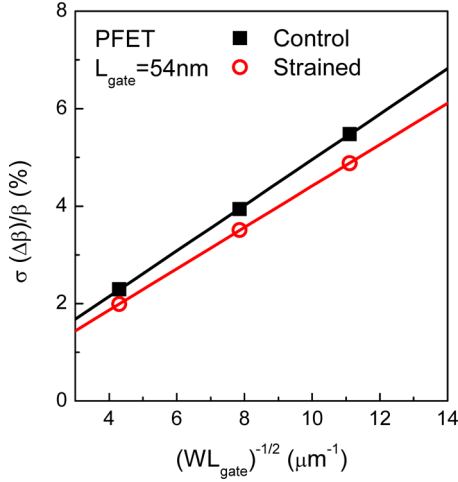
Fig. 10. Pelgrom plot of $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ showing smaller $\sigma(\Delta\beta)/\beta$ for the strained device.
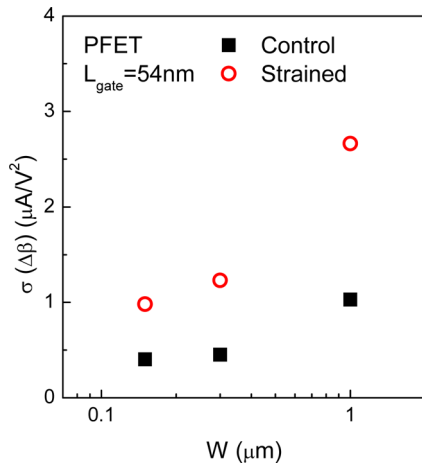


Fig. 11. $\sigma(\Delta\beta)$ versus gate width showing larger $\sigma(\Delta\beta)$ for the strained device.



Fig. 12. Hooge parameter versus $|V_{gst}|$ showing larger degree of mobility fluctuations for the strained device.



Fig. 13. $\sigma^2(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ in saturation region ($|V_{\mathrm{d}}| = 1$ V) showing the importance of the $V_{\mathrm{th}}$ mismatch in the high $|V_{gst}|$ (e.g., $|V_{gst}| = 0.8$ V) regime.

drain current mismatch in the high $|V_{gst}|$ regime is dominated by $\Delta\beta/\beta$.

The smaller $\sigma(\Delta\beta)/\beta$ for the strained device shown in Fig. 10 further demonstrates that it is the reduced $\sigma(\Delta\beta)/\beta$ that reduces the linear drain current mismatch in the high $|V_{gst}|$ regime. It should be noted that although the $\sigma(\Delta\beta)/\beta$ of the strained device is smaller than that of the unstrained one, the $\sigma(\Delta\beta)$ is actually larger for the strained device, as shown in Fig. 11. This implies that the improvement of $\sigma(\Delta\beta)/\beta$ for the strained device results from the increased $\beta$. The increased $\beta$ can be attributed to the strain-enhanced carrier mobility.

In order to further understand the enhanced $\sigma(\Delta\beta)$ in the strained device, we have performed low-frequency noise measurements. This is because carrier mobility fluctuations show their presence in the low-frequency noise characteristics. Through a careful extraction, we found that the Hooge parameter, which represents the degree of mobility fluctuations [25], is significantly larger for the strained device as compared with the unstrained one (see Fig. 12). It is plausible that the increased $\sigma(\Delta\beta)$ results from the strain enhanced mobility fluctuation.
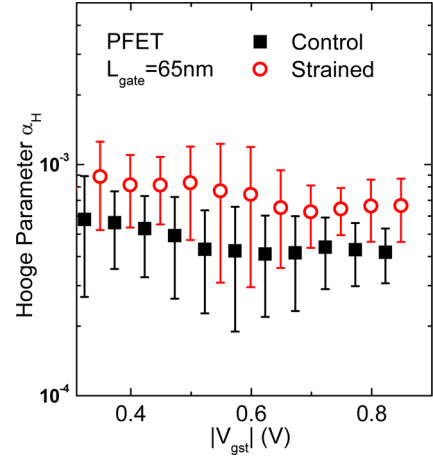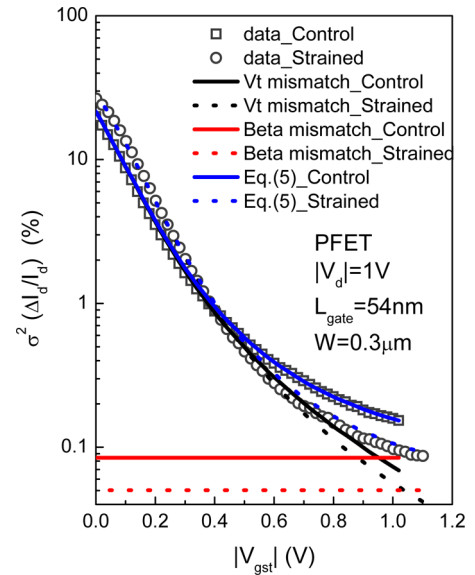
### B. Saturation Region

As compared with Fig. 8(a), Fig. 8(b) shows larger discrepancies in $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ between strained and unstrained devices. In other words, the improvement in $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained device is further enhanced in saturation region. Both Figs. 2(b) and 13 indicate that the $V_{\mathrm{th}}$ mismatch is still relevant to the overall $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ in the high $|V_{gst}|$ saturation region. In other words, the excess improvement of $\sigma(\Delta I_{\mathrm{d}})/I_{\mathrm{d}}$ for the strained device in saturation region results from the reduced $V_{\mathrm{th}}$ mismatch. The reduced $V_{\mathrm{th}}$ mismatch can be explained by the strain-reduced $g_m/I_{\mathrm{d}}$ in the high $|V_{gst}|$ saturation region (e.g., $|V_{\mathrm{d}}| = 1$ V), as shown in Fig. 14.

The reduced $g_m/I_{\mathrm{d}}$ in the high $|V_{gst}|$ saturation region for the strained device can be attributed to the strain-reduced $E_{\mathrm{sat}}$ [26] [see the first term in (3)]. The strain-reduced $E_{\mathrm{sat}}$ results from the enhanced carrier mobility in the strained device. The
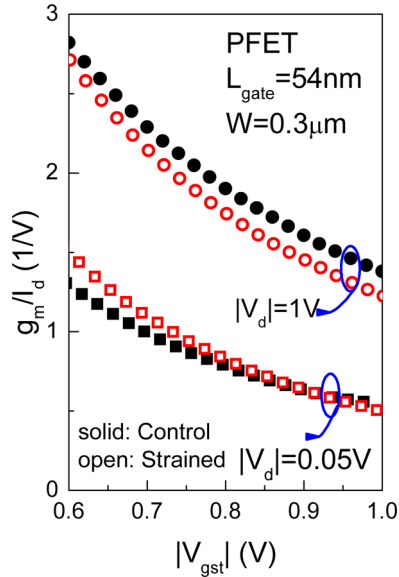
Fig. 14. The $g_m/I_d$ for the strained device in the high $|V_{gst}|$ saturation regime ($|V_d| = 1$ V) is smaller than the control counterpart.
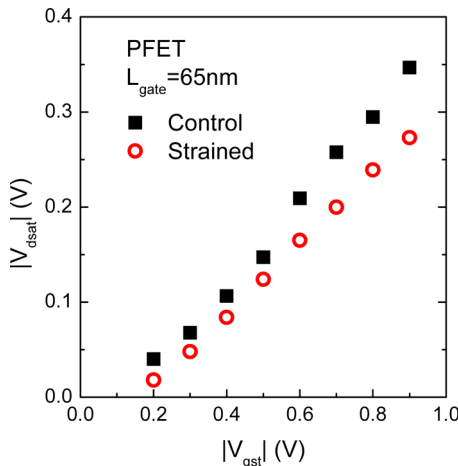


Fig. 15. $|V_{dsat}|$ versus $|V_{gst}|$ indicating a smaller $E_{sat}$ for the strained device.

enhancement in carrier mobility corresponds to an increase in slope of the carrier velocity versus lateral field characteristic and a reduction in the critical field ($E_{sat}$) for velocity saturation [26]. The strain-reduced $E_{sat}$ can be verified by the extracted drain saturation voltage ($V_{dsat}$) [26], which is essentially determined by $E_{sat}$ in the high $|V_{gst}|$ regime [27]. The extracted $V_{dsat}$ shown in Fig. 15 implies a smaller $E_{sat}$ for the strained device. It is the reduced $E_{sat}$ that results in a smaller $g_m/I_d$, and thus, further enhances the $\sigma(\Delta I_d)/I_d$ improvement for the strained device in the high $|V_{gst}|$ saturation region shown in Fig. 8(b).

## V. CONCLUSION

We have investigated and analyzed the mismatching properties of nanoscale strained PMOSFETs under various bias conditions. In the low $|V_{gst}|$ regime, the $\sigma(\Delta I_d)/I_d$ for the strained device is enhanced while the threshold voltage mismatch of the strained device is nearly identical to that of the control one. The

increased $\sigma(\Delta I_d)/I_d$ for the strained device can be attributed to the enhanced $g_m/I_d$. In other words, the $\sigma(\Delta I_d)/I_d$ of the strained device is almost the same as the unstrained one at a given $g_m/I_d$. In the high $|V_{gst}|$ linear region, the smaller $\sigma(\Delta I_d)/I_d$ for the strained device results from its smaller $\sigma(\Delta \beta)/\beta$, albeit the $\sigma(\Delta \beta)$ for the strained device is larger than that of the unstrained one. In the high $|V_{gst}|$ saturation regime, the improvement in $\sigma(\Delta I_d)/I_d$ for the strained device is further enhanced because of the strain-reduced $E_{sat}$.

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