A Nonvolatile InGaZnO Charge-Trapping-Engineered Flash Memory With Good Retention Characteristics

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***Abstract*—We report an amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor nonvolatile memory (NVM). This NVM shows a large 1.2-V extrapolated ten-year memory window, along with low 10-V/−12-V program/erase voltage, fast 1-ms/100-μs speed, and good endurance. This was achieved using a charge-trap-engineered structure and high-κ layers.**

***Index Terms*—Charge-trapping-engineered Flash (CTEF), high-κ, InGaZnO, metal–oxide–nitride–oxide–semiconductor (MONOS), nonvolatile memory (NVM).**

I. Introduction

Amorphous InGaZnO (IGZO) thin-film transistors (TFTs) have unique advantages of good uniformity like amorphous-Si TFTs and high mobility similar to poly-Si devices. The IGZO TFT is free from high-temperature crystallization and source–drain dopant activation procedure, where such a low-temperature process is vital for flexible display, RFID, and smart cards. For System-on-Panel (SoP) applications, an IGZO-based nonvolatile memory (NVM) is required [1], [2], but the retention loss and cycling decay are the challenges. This is due to the degraded dielectric quality at low process temperatures. In this letter, we have fabricated the charge-trapping Flash of metal–oxide–nitride–oxide–semiconductor (MONOS) [3]–[7] NVM devices on IGZO. Unfortunately, a similar fast retention loss was found. To further improve the memory window and retention, we added a thin SiO_2 layer on both tunnel and blocking layers and formed the charge-trapping-engineered Flash (CTEF) structure [6]. This NVM displays a large extrapolated ten-year memory window of 1.2 V at 25 °C or 0.6 V at 60 °C and good endurance, along with a low 10-V/ −12-V program/erase (P/E) voltage and fast 1-ms/100-μs speed. To our best knowledge, this is the best reported IGZO-based NVM device, and that is due to the low defect and large bandgap SiO_2 in CTEF [6] for both retention and erase saturation improvements.

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II. Experimental Details

We used bottom-gate IGZO TFT NVM devices [7], [8]. A 500-nm wet oxide was grown on a 4-in Si wafer to mimic the glasslike insulator substrate [9]. A 50-nm TaN gate electrode was formed by physical vapor deposition (PVD) and patterning, followed by a NH_3^+ treatment to improve the metal-gate/high-κ interface [10], [11]. For the MONOS structure, the 20-nm HfLaO, 20-nm HfON, and 6-nm HfLaO were deposited by PVD as the blocking, trapping, and tunnel layers, respectively. For the CTEF device, double 2.5-nm-SiO_2/12-nm-HfLaO blocking oxides, double 5-nm-Si_3N_4/5-nm-HfON trapping layers, and double 4-nm-HfLaO/2.5-nm-SiO_2 tunnel oxides were fabricated by PVD at room temperature. The gate dielectrics were improved by a 400 °C postdeposition anneal in an O_2 ambient. After that, a 40-nm IGZO active channel layer was deposited by RF sputtering using ceramic IGZO target $(Ga_2O_3 : In_2O_3 : ZnO = 1 : 1 : 1)$ in a 5% O_2/Ar ambient. Finally, 300 nm of Al electrodes was deposited on top of IGZO to form the source/drain contact. The fabricated TFT NVM has a gate length and width of 50 and 500 μm, respectively. The formed devices were characterized by different P/E tests, retention and cycling experiments in the dark, and an air ambient.

III. Results and Discussion

Fig. 1 shows the transfer hysteresis characteristics of an IGZO TFT MONOS device at $V_d = 1$ V, under very low voltage (±8–10 V) and fast (1–10 ms) P/E. The initial device shows a reasonably good I_{ON}/I_{OFF} of 5×10^5 and a subthreshold swing of 128 mV/dec. The I_d–V_g curve shifts toward the positive direction when a V_g of 8 V was applied for 10 ms and shifts back to the negative direction after a V_g of -10 V was applied for 10 ms.

Fig. 2(a) and (b) shows the program-and-erase characteristics of IGZO MONOS and CTEF devices. During program, V_t increases with increasing voltage and time, and the electrons were injected from the n-type IGZO channel through the tunnel oxide. The larger memory window in CTEF is due to the lower ΔE_C in $HfLaO/SiO_2$ for better electron tunneling [6]. Nevertheless, the erase function is more difficult. An erase saturation that is due to trap-assisted gate leakage was found.

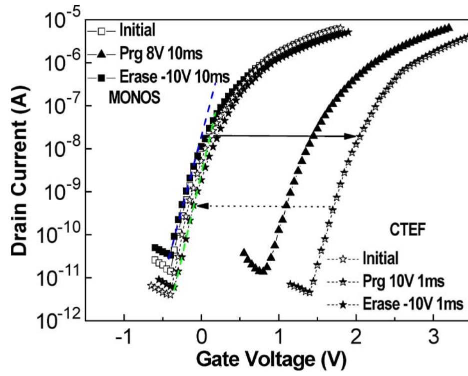
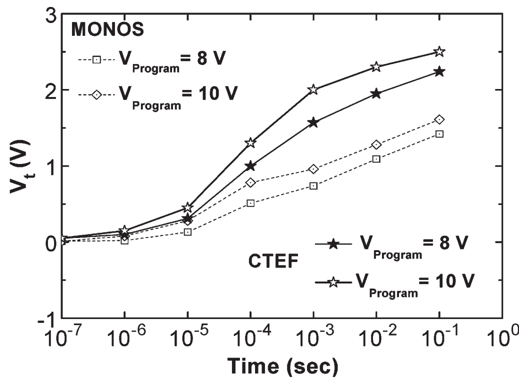
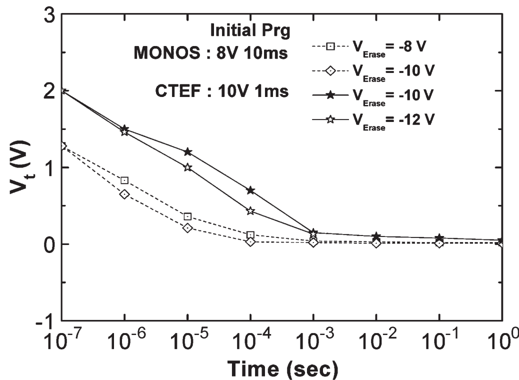


Fig. 1. I_d–V_g curves of IGZO MONOS and CTEF NVM devices under P/E.



(a)



(b)

Fig. 2. (a) Program and (b) erase characteristics of IGZO MONOS and CTEF NVM devices under different voltages and times.

However, this is inevitable even for high-temperature-formed high-κ blocking oxide [5], [6] and becomes worse at lower temperature [7]. During erase, the trapped electrons need to be removed over the tunnel oxide to lower V_t; alternatively, the minority holes in the depleted IGZO can tunnel into the trapping layer and annihilate the trapped electrons. However, the latter case is less effective due to the wide bandgap of IGZO. From the continuity equation, the lower κ SiO_2 in the $HfLaO/SiO_2$ tunnel layer of CTEF has a higher electric field which benefits the erase.

Fig. 3 shows the retention characteristics. The IGZO MONOS device shows a memory window of an initial 1.1 V, which decreased rapidly at the first 10^3-s retention and became gradually stable at longer time. Similar phenomena were also found in low-temperature-formed MONOS devices on pentacene [7], which was possibly due to the trap-assisted tunneling via low energy defects in tunnel oxide. In sharp contrast, a good initial memory window of 1.6 V and an extrapolated ten-year window of 1.2 V occurred for the IGZO CTEF device at 10-V/−12-V 1-ms/100-μs P/E. Still, a large extrapolated ten-year window of 0.6 V is reached at 60 °C retention. The good retention is due to the small bandgap HfON trapping layer, double $HfLaO-SiO_2$ energy barriers [12], and higher barrier height and lower defects in SiO_2 than a single high-κ layer in MONOS devices [6]. The low P/E voltage reflects the high gate capacitance using high-κ layers.

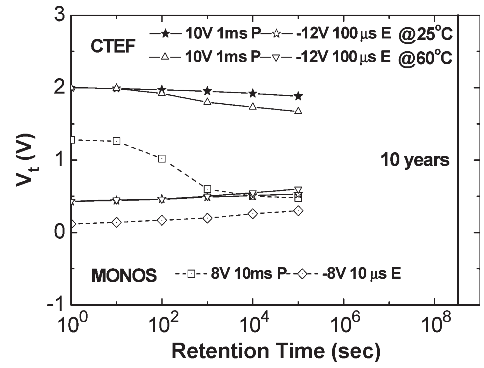


Fig. 3. Retention characteristics of the IGZO MONOS and CTEF NVM devices.

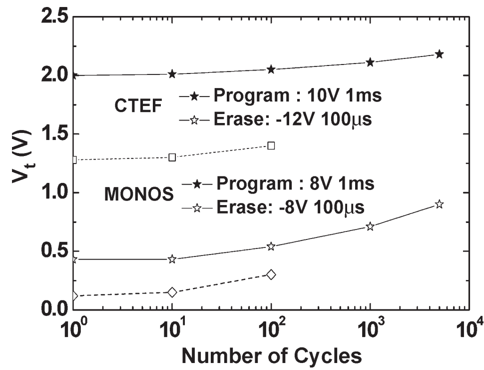


Fig. 4. Endurance characteristics of the IGZO MONOS and CTEF NVM devices.

The endurance characteristics of IGZO NVM devices are shown in Fig. 4. The endurance for the CTEF device is significantly better than the MONOS counterpart. The MONOS device failed after 100 cycles but the CTEF can last up to 5000 cycles. The improved cycling characteristics in the CTEF is attributed to the lower energy barrier in the double $HfLaO-SiO_2$ tunnel layer. Moreover, the excellent endurance of the CTEF device occurs with a small 12% degradation after 10^3 P/E cycles, owing to the fast P/E speed not overstressing the tunnel oxide. To the best of our knowledge, these results are the best reported data for low-temperature-processed NVM devices on IGZO [1], [2].

IV. Conclusion

We have successfully developed a long-retention and good-endurance IGZO NVM device. This is achieved by using a

CTEF device that has a large 1.2-V extrapolated ten-year memory window, along with low 10-V/-12-V P/E voltage, fast 1-ms/100-μs speed, good endurance, and compatible with TFT for SoP application.

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