Electric-Field Enhancement of a Gate-All-Around Nanowire Thin-Film Transistor Memory

Po-Chun Huang, Lu-An Chen, and Jeng-Tzong Sheu

***Abstract*—A high-performance gate-all-around (GAA) poly-Si nanowire (NW) SONOS-type memory thin-film transistor (TFT) is presented. The presence of the corners of the GAA structure resulted in the program speed and memory window of this device being superior to those of a planar poly-Si TFT device. When erasing, planar devices exhibit a threshold-voltage shift resulting from gate injection; the GAA device was immune to this behavior. The presence of a nonuniform electric field in the channel region during programming and erasing was confirmed through simulation. The device also exhibited superior endurance and data-retention behavior.**

***Index Terms*—Field enhancement, gate-all-around (GAA), gate injection, nanowire (NW), SONOS, thin-film transistor (TFT).**

I. INTRODUCTION

POLYSILICON thin-film transistors (poly-Si TFTs) have been studied for many years because of their application in active-matrix liquid-crystal displays (LCDs) [1]. To develop LCDs that are more compact, more reliable, and cheaper, system-on-panel (SOP) products, with functional devices (e.g., controller [2] or memory [3] functions) integrated on the LCD panel, have been proposed as a new development in display technology. Moreover, when embedding memory functions into SOPs, the power consumption of the system can be decreased dramatically [4], [5]. There are, however, several critical issues relating to SOPs incorporating traditional TFT memory functions, such as low memory speeds and poor device properties, induced by grain-boundary trap states in channels and serious short-channel effects (SCEs) [6]. Recently, multiple-gate devices that exhibit fully controlled surface potentials in their channel regions and suppressed SCEs have been prepared [7], [8]. Moreover, the additional electric field implies that more electrons tunnel into the storage layer over the channel, revealing that multiple-gate memory devices possess larger memory windows and superior programming/erasing (P/E) efficiencies. On the other hand, optimizing the stacking layer is another way to further improve the P/E efficiency and utilizing lower operation voltage. Nevertheless, the reduced control oxide thickness during scaling down results in serious gate injection currents during memory operation [9]. Optimization of the oxide/nitride/oxide stack layers therefore remains critical [10].

In a previous study [11], we found that a gate-all-around (GAA) poly-Si nanowire (NW) TFT provided excellent gate control as a result of electric-field enhancement by its gate-all-around structure. To obtain high-performance poly-Si TFT memories, in this letter, we prepared GAA poly-Si NW SONOS-TFT memory. The electric-field enhancement in the corner regions improved the channel controllability, enhanced the program speed, and increased the memory window. In addition, the nonuniform electric field across the channel region was proved to prevent the gate injection during erasing without modification of the thickness of the stack layers, and still, few papers discuss this issue in multiple-gate memory devices. This behavior was also confirmed via ISE TCAD simulations.

II. DEVICE FABRICATION

As described in a previous study, the 1-μm-long multiple (20) channels of poly-Si NWs were fabricated using a spacer-patterning technique [11]. Solid-phase crystallization was then performed at 600 °C for 24 h in nitrogen ambient to turn α-Si into a polycrystalline-Si structure. The sidewall spacers served as hard masks in the following poly-Si etching process. By controlling the RIE conditions and the thickness of the SiN_x film, the feature size of the SiN_X spacer could be reduced to the nanoscale without using any advanced photolithographic techniques. Utilizing the nitride spacer as a hard mask, 1-μm-long multiple channels of poly-Si NWs having a channel width (W_{ch}) of approximately 40 nm were formed. After wet etching in diluted (1:100) HF solution to remove 70–80 nm of the BOX layer, the poly-Si NWs were released from the BOX substrate. Next, sequential conformal deposition of a dielectric of ONO stacks (TEOS/nitride/TEOS = 5 nm/4.3 nm/7.7 nm) and LPCVD deposition of 200-nm *in situ* N^+ poly-Si were performed to surround the channels. After transferring the gate pattern, self-aligned phosphorus ion implantation was performed at a dose of 5×10^{15} cm^{-2}, followed by thermal activation at 600 °C for 6 h. After depositing a 300-nm-thick TEOS passivation layer through LPCVD, the contacts of all the devices were defined, followed by Al metallization. Finally, the devices were sintered at 400 °C in N_2 ambient for 30 min.

III. RESULTS AND DISCUSSION

Fig. 1(a) and (b) shows a top-view scanning electron microscopy (SEM) image of a GAA NW SONOS-TFT memory device and a transmission electron microscopy (TEM) image

Manuscript received October 26, 2009. First published February 5, 2010; current version published February 24, 2010. This work was supported in part by the National Science Council and in part by the MOE-ATU Program in Taiwan. The review of this letter was arranged by Editor A. Nathan.

P.-C. Huang is with the Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: ginjel@gmail.com).

L.-A. Chen and J.-T. Sheu are with the Institute of Nanotechnology, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: kamidochen@hotmail.com; jtsheu@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2038177

0741-3106/$26.00 © 2010 IEEE

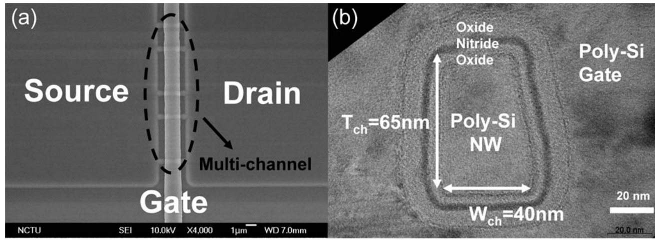

Fig. 1. (a) Top-view SEM image of a GAA poly-Si NW SONOS-type TFT memory device. (b) TEM image of a SONOS TFT possessing a GAA structure. The NW channel was surrounded by ONO stacks (TEOS/nitride/TEOS = 5 nm/4.3 nm/7.7 nm) and a poly-Si gate with a channel width of 40 nm and a thickness of 65 nm.

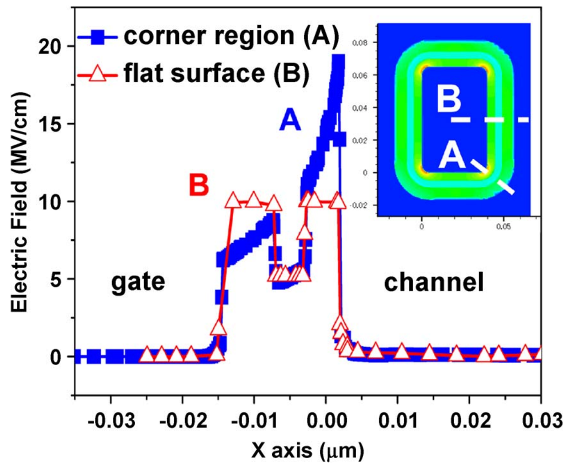

Fig. 2. ISE TCAD simulation of the electric-field distributions in the corner region and on the flat surface under a gate bias of −16 V. The inset shows that the maximum electric field is concentrated near the corners. The peak value of electric field is estimated to be 19 MV/cm at the corner region.

of a NW channel possessing a GAA structure surrounded by ONO layers, respectively. The proposed devices have a nominal channel length (L) of 1 μm, a channel width $(W_{\rm ch})$ of approximately 40 nm, a channel thickness $(T_{\rm ch})$ of 65 nm, and an effective channel width $(W_{\rm eff})$ of 4.2 μm $[20 \times 2 \times (W_{\rm ch} + T_{\rm ch})]$. For comparison, we also fabricated conventional planar devices having a channel width of 4.13 μm and a channel length of 1 μm.

Fig. 2 shows the results of ISE TCAD simulation analysis of electric field under a gate bias of -16 V for the proposed device. We observe that the maximum electric field is concentrated near the corners. Because the aspect ratio $(T_{\rm ch}/W_{\rm ch} = 1.6)$ is greater than that of the conventional planar TFT $(T_{\rm ch}/W_{\rm ch} \ll 0.1)$, we expected the device characteristics to be improved as a result of corner effects [12]. Because the oxide thickness was approximately 5 nm, the tunneling current was dominated by Fowler–Nordheim (FN) tunneling under an operating bias [13]. We estimated the peak value of electric field to be 19 MV/cm at the corners. As a result, the tunneling current was expected to be larger at the corners than that in the flat areas; therefore, the system is predicted to exhibit improved memory characteristics [14]. Fig. 3 shows the P/E characteristics of the GAA NW SONOS-TFT memory. An FN tunneling mechanism was employed to characterize the transient memory performance of the cell by grounding the source and drain and stressing the gate. Moreover, the relatively

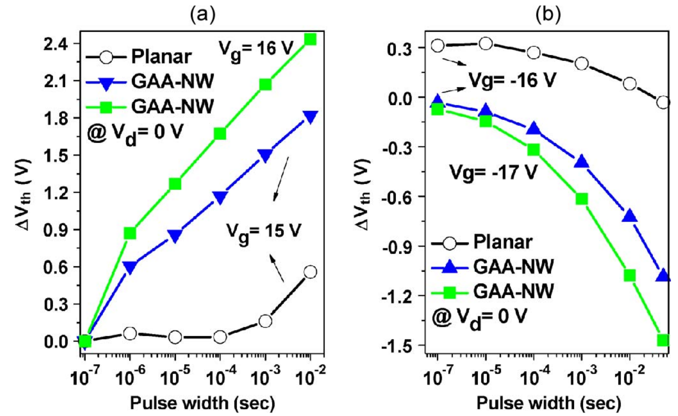

Fig. 3. Comparisons of the (a) program efficiencies and (b) erase characteristics of the GAA multiple NW channel device and the conventional planar device. Due to gate injection, the threshold voltage underwent a positive shift in the planar device.

fast programming $(t = 10\ \mu\text{s}, V_g = 16\ \text{V})$ and erasing $(t = 1\ \text{ms}, V_g = -17\ \text{V})$ achieved threshold-voltage shifts of 1.27 and 0.6 V, respectively. To demonstrate the contribution to the electric-field enhancement due to corner effects, Fig. 3(a) and (b) compare the memory characteristics with those of the planar device. Because the electric field across the dielectric has a dramatic influence on the FN tunneling current, the tunneling current in the GAA multiple-channel device was increased significantly as a result of the large electric fields at the corner regions. Greater band bending occurred at the corner regions where more electrons were injected into the storage layer in the GAA device. The GAA NW SONOS-TFT memory exhibited a larger $V_{\rm th}$ shift (1.5 V) at a pulse of 15 V and 1 ms on the gate. Under the same conditions, the planar device provided a threshold-voltage shift of only 0.2 V. In addition, decomposing the microchannel into the GAA multiple NW channel structure increased the number of corners and led to a higher efficiency device as a result of the corner effect. After performing the erase operation, as shown in Fig. 3(b), however, we found that the threshold voltage $(V_{\rm th})$ underwent a positive shift in the planar device and a negative shift in the GAA device. The value of $V_{\rm th}$ of the erase state is determined by the charge balance between the gate injection and detrapping out of the ONO layer [15]. The gate injection causing the injection of electrons from the gate to the storage layer during the erasing operation led to inefficient erasing and positive threshold-voltage shift and is related to the electric field under biasing. Fig. 2 also shows that the channel corner region had a larger electric field; the electric fields were not uniform across the ONO layer between the gate and the channel in the GAA device. As a result, more electrons detrapped from the nitride film to the channel than were injected from the gate to the nitride layer. Moreover, according to Gauss' law, the electric field in the control oxide of a corner region will be less than that in a flat surface, thereby resulting in a reducing gate injection current. This electric-field enhancement effect may be useful for scaling down the oxide thickness without introducing a new material (e.g., a high-k top dielectric) [9]. In addition, further optimizing the ONO stack layer might expand the memory window and reduce the operating voltage [10]. To demonstrate the reliability of our proposed device, Fig. 4(a)

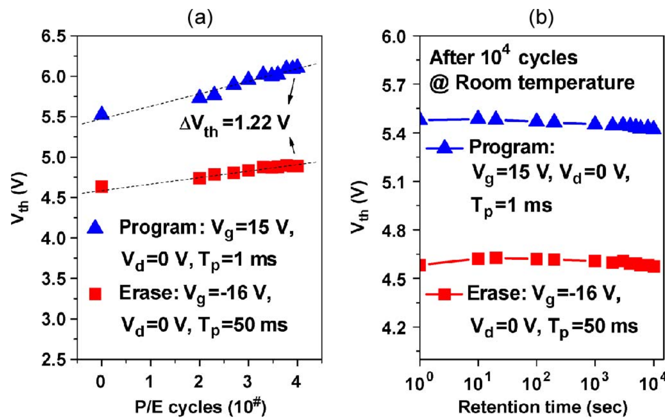

Fig. 4. (a) Endurance of the GAA NW SONOS-TFT memory device featuring TEOS/nitride/TEOS layer thicknesses of 5, 4.3, and 7.7 nm, respectively. (b) Retention behavior of the GAA NW SONOS-TFT memory device operated at room temperature after 10^4 P/E stress cycles.

shows the endurance characteristics of a GAA NW SONOS-TFT device subjected to a programming bias of 15 V for 1 ms and an erasing bias of −16 V for 50 ms. Because the oxide positive trap charge accumulated upon increasing the number of P/E cycles, the threshold voltage increased slightly. Nevertheless, the GAA NW SONOS-TFT device maintained a memory window of 1.22 V over an endurance test of 10^4 P/E cycles. Fig. 4(b) shows the data retention measured at room temperature after 10^4 endurance cycles; the proposed GAA NW SONOS-TFT memory device maintained a memory window at 0.85 V during the measurement process.

IV. Conclusion

In summary, we have developed a GAA poly-Si NW SONOS-TFT memory device featuring multiple channels. Because of its GAA structure, this NW device exhibited superior memory characteristics relative to those of a planar device. In addition, a simulation of electric field revealed that the enhancement in P/E efficiency arose mainly as a result of the large number of corners $(80 = 20 \times 4)$, where the strongest electric field was induced. With a larger electric field present at the corners during the erasing process, the GAA NW SONOS TFT did not experience the positive threshold-voltage shift commonly caused by gate injection.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories for the facility utilization.

References

[1] T. Aoyama, K. Ogawa, Y. Mochizuki, and N. Konishi, “Inverse staggered poly-Si and amorphous Si double structure TFTs for LCD panels with peripheral driver circuits integration,” *IEEE Trans. Electron Devices*, vol. 43, no. 5, pp. 701–705, May 1996.

[2] K. Yoneda, R. Yokoyama, and T. Yamada, “Development trends of LTPS TFT LCDs for mobile applications,” in *VLSI Symp. Tech. Dig.*, 2001, pp. 85–86.

[3] H. Kimura, T. Maeda, T. Tsunashima, T. Morita, H. Murata, S. Hirota, and H. Sato, “A 2.15 inch QCIF reflective color TFT-LCD with digital memory on glass (DMOG),” in *Proc. SID Int. Symp. Dig. Tech. Papers*, 2001, pp. 268–271.

[4] Y. Nakajima, Y. Kida, M. Murase, Y. Toyoshima, H. Murata, and Y. Maki, “Latest development of system-on-glass display with low temperature poly-Si TFT,” in *Proc. SID Int. Symp. Dig. Tech. Papers*, 2004, pp. 864–867.

[5] A. J. Walker, S. Nallamothu, E.-H. Chen, M. Mahajani, S. B. Herner, M. Clark, J. M. Cleeves, S. V. Dunton, V. L. Eckert, J. Gu, S. Hu, J. Knall, M. Konevechi, C. Petti, S. Radigan, U. Raghuram, J. Vienna, and M. A. Vyvoda, “3-D TFT-SONOS memory cell for ultra-high density file storage applications,” in *VLSI Symp. Tech. Dig.*, 2003, pp. 29–30.

[6] J. Li, A. Bansal, and K. Roy, “Poly-Si thin-film transistors: An efficient and low-cost option for digital operation,” *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2918–2929, Nov. 2007.

[7] M. Im, J. W. Han, H. Lee, L. E. Yu, S. Kim, C. H. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y. K. Choi, “Multiple-gate CMOS thin-film transistor with polysilicon nanowire,” *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102–105, Jan. 2008.

[8] C. J. Su, H. C. Lin, H. H. Tsai, H. H. Hsu, T. M. Wang, T. Y. Huang, and W. X. Ni, “Operations of poly-Si nanowire thin-film transistors with a multiple-gated configuration,” *Nanotechnology*, vol. 18, no. 21, pp. 215 205–215 211, May 2007.

[9] P. H. Tsai, K. S. Chang-Liao, D. W. Yang, Y. B. Cung, T. K. Wang, P. J. Tzeng, C. H. Lin, and L. S. Lee, “Crucial integration of high work-function metal gate and high-k blocking oxide on charge-trapping type flash memory device,” *Appl. Phys. Lett.*, vol. 93, no. 25, pp. 252 902–252 904, Dec. 2008.

[10] N. Goel, D. C. Gilmer, H. Park, V. Diaz, Y. Sun, J. Price, C. Park, P. Pianetta, P. D. Kirsch, and R. Jammy, “Erase and retention improvements in charge trap flash through engineered charge storage layer,” *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 216–218, Mar. 2009.

[11] J. T. Sheu, P. C. Huang, T. S. Sheu, C. C. Chen, and L. A. Chen, “Characteristics of gate-all-around twin poly-Si nanowire thin-film transistors,” *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 139–141, Feb. 2009.

[12] J. W. Yang and J. G. Fossum, “On the feasibility of nanoscale triple-gate CMOS transistors,” *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1159–1164, Jun. 2005.

[13] E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, “Modeled tunnel currents for high dielectric constant dielectrics,” *IEEE Trans. Electron Devices*, vol. 45, no. 6, pp. 1350–1355, Jun. 1998.

[14] G. Fiori, G. Iannaccone, G. Molas, and B. De Salvo, “Dependence of the programming window of silicon-on-insulator nanocrystal memories on channel width,” *Appl. Phys. Lett.*, vol. 86, no. 11, pp. 113 502–113 504, Mar. 2005.

[15] Y. H. Shih, H. T. Lue, K. Y. Hsieh, R. Liu, and C. Y. Lu, “A novel 2-bit/cell nitride storage flash memory with greater than 1M P/E-cycle endurance,” in *IEDM Tech. Dig.*, 2004, pp. 881–884.