A DVS Embedded Power Management for High Efficiency Integrated SoC in UWB System

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***Abstract*—The proposed power management module with a typical 1.2 V low-voltage PWM (LV-PWM) controller and dynamic voltage scaling (DVS) function is designed using 65 nm technology for integration with the ultra-wide band (UWB) system. The on-chip pre-regulator with a power conditioning circuit can provide a regulated supply voltage to the LV-controller. Moreover, the proposed handover technique can achieve the self-biasing mechanism to further reduce power dissipation. To operate in low voltage, the proposed compensation enhancement multistage amplifier (CEMA) can achieve high loop gain and ensure system stability without using any external compensation component. The fabricated power management module occupies 0.356 mm^2 silicon area with an excellent line/load transient response. Owing to the DVS function, the proposed power management can meet the power requirement in the UWB system and other RF transceiver systems.**

***Index Terms*—DC-DC converter, dynamic voltage scaling, low-voltage operation, power conversion efficiency, power management, transient response, UWB system.**

I. Introduction

VARIOUS multimedia and portable devices claim low power consumption, high performance, compactness, and robustness all at the same time. These claims force IC designers to encounter several challenges that must be overcome in system-on-chip (SoC) integration, especially in power management. There are two important issues in the conventional design of power management module [1]–[6] for portable communication SoC applications such as ultra-wideband (UWB). One is low power consumption for extending battery lifetime [7], and the other is a demanding requirement in both steady state and transient response. The SoC design follows the trend of integrating an embedded power management module [8], [9] in order to reduce print-circuit-board (PCB) area and enhance power conversion efficiency. Recently, the new integrated technique for SRAM of Sub-V_t microcontroller in 65 nm technology tailored for very high digital density and mixed-signal integration applications was presented in [10] with a switched-capacitor structure. However, in contrast to the inductor-based structure, switched-capacitor structure with low driving capability is not suitable for UWB system applications [11], [12]. The inductor-based structure in the conventional power management module [1]–[6] has good driving capability. To further reduce the silicon area and attain a compact integration size with the UWB system, the proposed power management module, which is fabricated by 65 nm technology, adopts low-voltage core devices in the controller design under low-voltage operation. Inevitably, the implementation of deep-submicron devices for analog circuit results in more design challenges.

As conceptually illustrated in Fig. 1, the embedded power management module in the UWB system contains two individual power sources, $V_{\rm out1}$ and $V_{\rm out2}$, to supply radio frequency (RF) and digital circuits, respectively. This proposed architecture minimizes the demand for high-voltage I/O devices by means of a low-voltage PWM (LV-PWM) controller with an on-chip compensation method. Moreover, a self-biasing mechanism is implemented in the proposed power management module to effectively improve efficiency and extend battery life. Furthermore, a linear regulator is adopted in the power source of RF circuits to suppress the switching noise from DC-DC converter. For the consideration of performance and layout flexibility, the linear regulator for RF blocks is not included in this power management.

Dynamic voltage scaling (DVS) function is an effective solution to reduce the power consumption of the digital systems especially in the low-power circuit design or the SoC integration [13]–[15]. In the UWB system, if the throughput constraint is cycling between different operating modes, then dynamically adjusting the supply voltage can achieve efficient power saving. As reported in [15], the silent mode and the transmission mode of the wireless sensor node and SRAM need the DVS function. In UWB system operation depicted in Fig. 2, there is no data in the vacant transmission time slot during the data transmission procedure. The DVS function can lower down the supply voltage to minimize power consumption and return it to the standard value before data transmission. Thus, the DVS embedded power management is a good solution to achieve the different power request from the UWB system and consequently derive a suitable power source. The specifications of the power management for UWB system is illustrated in Table I.

In this paper, the structure of the proposed power management module with the LV-PWM controller is described in

Manuscript received January 25, 2010; revised March 08, 2010; accepted June 01, 2010. Date of current version October 22, 2010. This paper was approved by Guest Editor Mototsugu Hamada.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2010.2063610

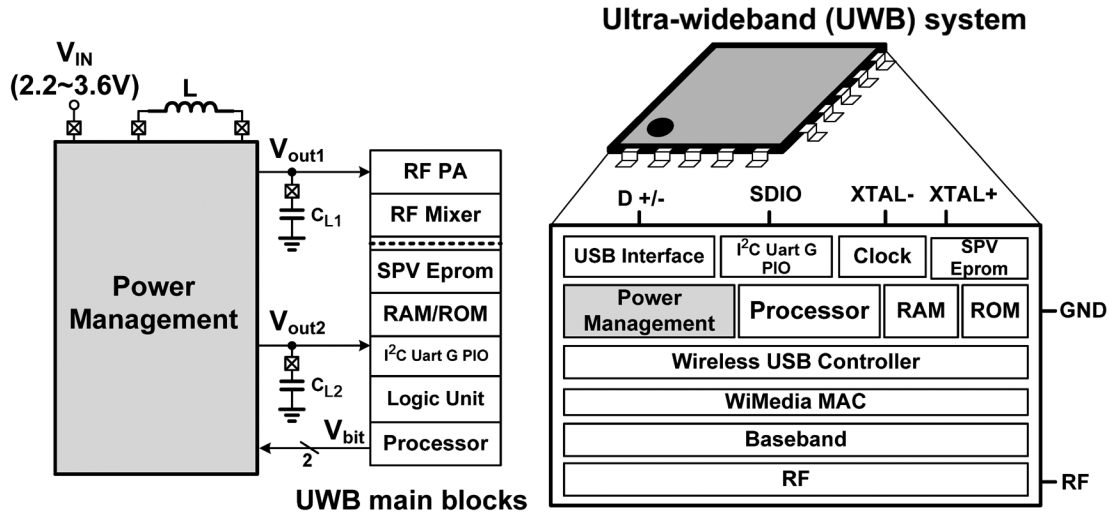

Fig. 1. The architecture of the proposed embedded power management module in UWB systems.

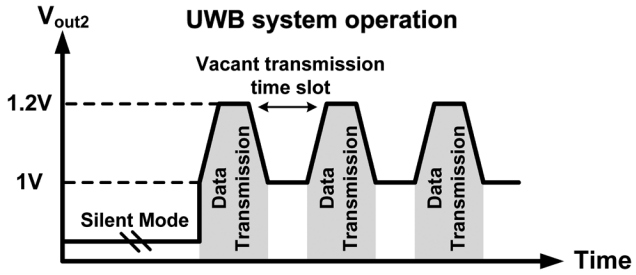

Fig. 2. The DVS function in UWB system operation.

Section II. The detailed circuit implementation of the proposed power management module is shown in Section III. Experimental results and the chip prototype are presented in Section IV. Finally, a conclusion of the proposed power management module is given in Section V.

II. Power Management Module With the Low-Voltage PWM Controller

The proposed power management module is shown in Fig. 3. It contains the pre-regulator, the low-voltage PWM (LV-PWM) controller, the dynamic voltage scaling (DVS) function and the post-regulator. In this proposed structure, a step-down DC-DC converter is utilized to transfer the input voltage to the first output $V_{\rm out1}$, typically 1.8 V, for RF and mixer circuit in the UWB system. In addition, the post-regulator, which is implemented with the low-dropout regulator, is placed behind the $V_{\rm out1}$ to generate the second output voltage $V_{\rm out2}$, typically 1.2 V, for digital function blocks in the UWB system.

The pre-regulator, composed of the switched-capacitor (SC) converter and a low-dropout regulator (LDO) circuit, supplies a stable, noiseless, and regulated voltage V_{core} to the LV-PWM controller from the input high voltage supply. The LV-PWM controller is implemented by core devices in the 65 nm technology and supplied by 1.2 V from the pre-regulator. Moreover, a power-efficient handover circuit in the pre-regulator can achieve the self-biasing mechanism in order to reduce power dissipation of the pre-regulator when the second output voltage $V_{\rm out2}$ is regulated after the start-up period.

The LV-PWM controller betters the embedded power management module in terms of cost and performance. A compensation enhancement multistage amplifier (CEMA) is proposed as the error amplifier to provide high gain and stabilize the closed-loop system without any external compensation component. To overcome the design difficulties due to the small voltage headroom when using low-voltage core devices, the multistage structure is adopted to derive high gain and achieve good regulation. The CEMA can replace an error amplifier in low-voltage design to obtain a performance similar to that of a cascode error amplifier under a high supply voltage. However, the cascaded structure will induce some unwilling non-dominant poles that would deteriorate the phase margin. Thus, the closed-loop compensation has to be contemplated discreetly.

DVS function in the proposed power management module can provide a suitable and competitive solution for the UWB integration. The embedded DVS function would receive the power request from the UWB processer through the two-bit signal, V_{bit}, which would indicate an adequate voltage value of $V_{\rm out2}$ from 1 V to 1.3 V in order to get superior UWB system performance.

In the system operation of the proposed power management module, the error signal V_c, which is generated by the CEMA, can reflect the load condition from the output voltage $V_{\rm out1}$ and decide the duty ratio through a comparison with the summing signal, V_{sum}, which is a summation of the current sensing signal V_s and the slope compensation V_{slope}. Additionally, the Clk signal generated by the sawtooth generator synchronizes PWM modulation in the current-mode DC-DC converter and carries out a duty ratio signal, V_{PWM}, with the comparator. The dead-time control can also avoid the occurrence of shoot-through current when the two power switches, M_P and M_N, turn on simultaneously.

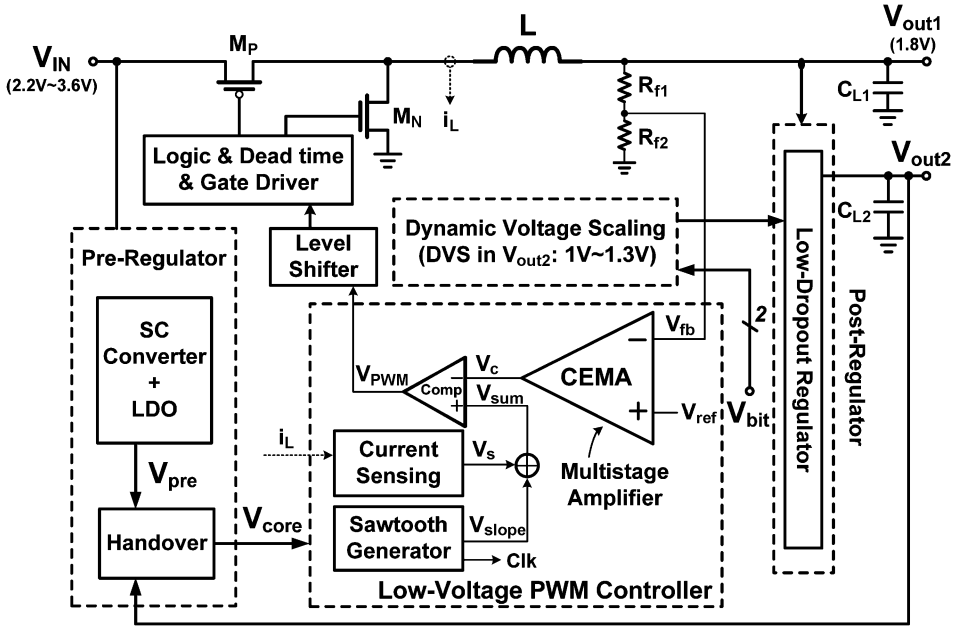

Fig. 3. Full structure of the proposed power management module.

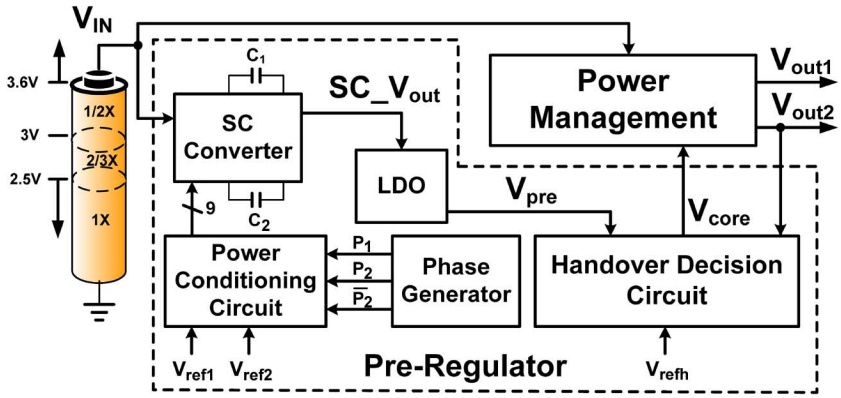

Fig. 4. The proposed pre-regulator design in power management module.

III. Circuit Implementation

A. Pre-Regulator

In the proposed power management module implemented by the 65 nm technology, the high input voltage $V_{\rm IN}$ cannot directly connect to low-voltage core devices since the reliability issue. Basically, using the high-voltage I/O device to implement the whole controller in the power management module is simple, but it occupies a large silicon area and increases cost. Therefore, an appropriate solution is to convert the high input voltage to a low voltage to drive the LV-PWM controller. To supply a regulated and noiseless power to the LV-PWM controller, a high efficiency pre-regulator is the design object.

1) The SC Converter With Cascaded LDO Circuit: In general, the pre-regulator is served by a LDO circuit. The advantages are simple structure and small silicon area, but a serious drawback is poor efficiency at low output level [16]–[18]. The SC converter can provide a large step-down conversion ratio without the need of a complicated structure for high conversion efficiency. The cascaded LDO circuit is chosen to suppress the noise generated from the SC converter in order to ensure a stable and regulated supply voltage to drive the LV-PWM controller. Fig. 4 shows the proposed pre-regulator design. The SC converter with the cascaded LDO circuit is controlled by the power conditioning circuit and the phase generator to guarantee a low output voltage $V_{\rm pre}$.

Fig. 5 illustrates the detailed configuration of the SC converter with cascaded LDO circuit controlled by the power conditioning circuit and the phase generator. In Fig. 5(a), the power conditioning circuit can decide the conversion ratio of the SC converter according to the high input voltage, $V_{\rm IN}$. R_1 and R_2 are 400 KΩ and 100 KΩ, respectively. The reference signals of $V_{\rm ref1}$ and $V_{\rm ref2}$, which are generated from the bandgap reference circuit, are 0.5 V and 0.6 V, respectively. The adaptive conversion ratio aims for high power conversion efficiency. The decoder can generate the gate control signals, $S_1 - S_9$, for the SC converter through the factor control signals, V_{T1} and V_{T0}, and the phase clocks. The phase generator generates the phase clocks that contain P_1, P_2, and $\overline{P}_2$. Owing to the power conditioning circuit, high input voltage $V_{\rm IN}$ can be scaled down

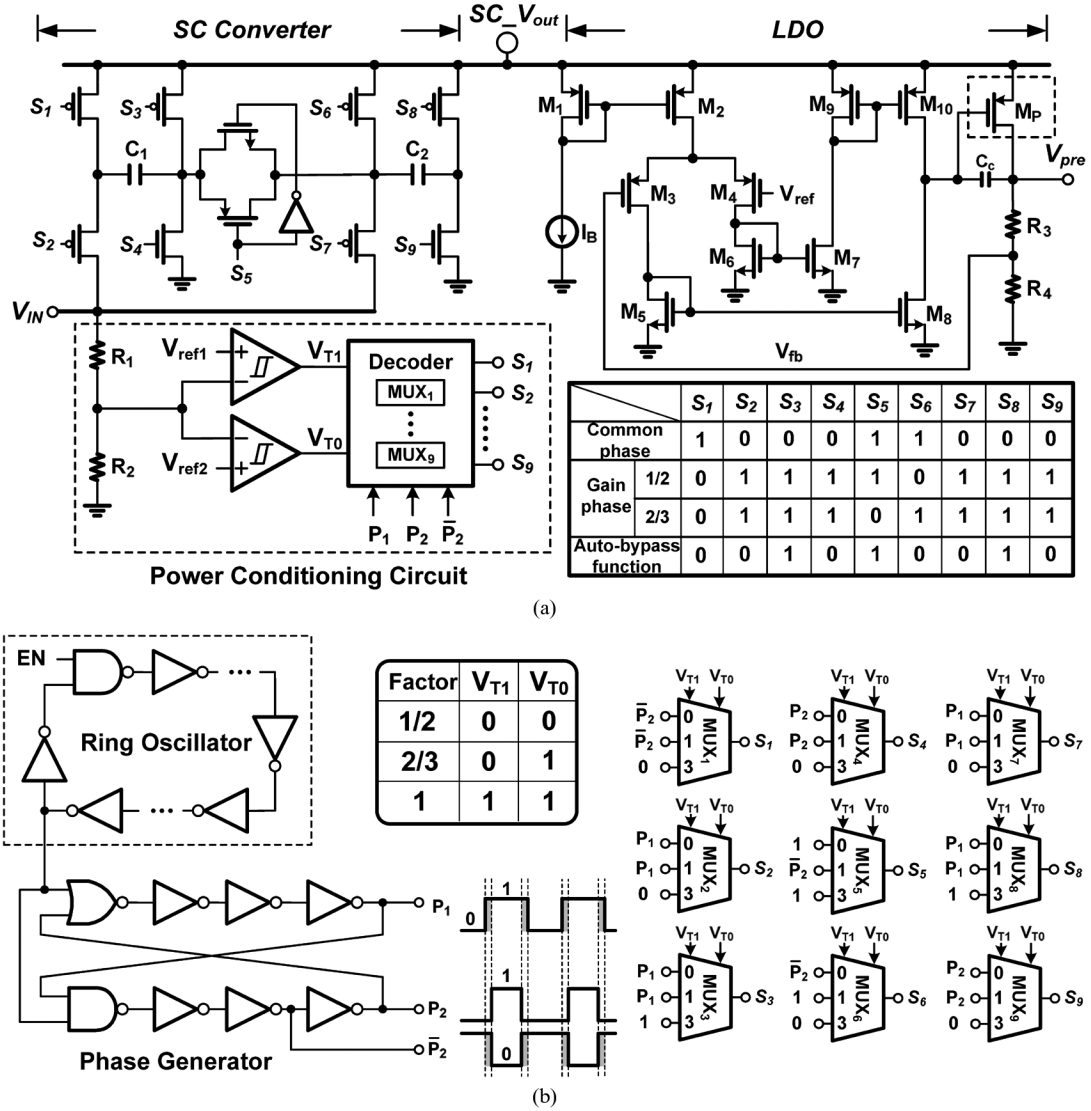

Fig. 5. (a) The structure of the SC converter with cascaded LDO circuit and the power conditioning circuit. (b) The phase generator in the pre-regulator.

to a low voltage $SC\_V_{\rm out}$ through the automatically predetermined factors of $(1/2)\times$ or $(2/3)\times$. Moreover, to maintain a high pre-regulator efficiency, the auto-bypass function would disable the SC converter and directly connect $V_{\rm IN}$ to $SC\_V_{\rm out}$ when input voltage is lower than 2.5 V. Under different conversion ratios, the table in Fig. 5(a) lists the operation of SC converter for gain and common phases. This mechanism allows the pre-regulator to enhance conversion efficiency over a wide input voltage range. The conversion efficiency of the pre-regulator can be shown in (1), where M represents the conversion ratio of the SC converter.

$$\eta_{\rm pre} = \eta_{SC} \times \eta_{\rm LDO} \approx \frac{SC\_V_{\rm out}}{M \cdot V_{\rm IN}} \times \frac{V_{\rm pre}}{SC\_V_{\rm out}} = \frac{V_{\rm pre}}{M \cdot V_{\rm IN}} \quad (1)$$

The LDO circuit in the pre-regulator is compensated with a small on-chip capacitor of 0.1 pF. It would also increase the power supply rejection (PSR) from the high input voltage for the LV-PWM controller.

The phase generator is depicted in Fig. 5(b). The phase clock generated by the ring oscillator is designed with the dead-time mechanism produced by simple logic scheme to prevent leakage in the SC converter. The multiplexer would decide the gate control signal for the switches in the SC converter by the factor control signals, V_{T1} and V_{T0}. That is, all switches in the SC converter are kept at off state to eliminate leakages of charge sharing during the phase-exchanging period. Consequently, conversion efficiency of the pre-regulator can be further enhanced.

2) Handover Technique: The proposed handover technique is activated after the second output voltage $V_{\rm out2}$ is regulated. Through the handover decision circuit in Fig. 4, $V_{\rm out2}$ would take over the job of the SC converter with cascaded LDO circuit to supply the LV-PWM controller. Accordingly, the pre-regulator can be shutdown to reduce power consumption and achieve an imperative predominance in the highly integrated SoC system.

During the start-up period, V_{core} is connected to $V_{\rm pre}$ since $V_{\rm out2}$ is still smaller than a rated value. Once $V_{\rm out2}$ is activated and regulated to supply the UWB system, the handover technique will disconnect V_{core} from $V_{\rm pre}$ and connect to $V_{\rm out2}$ through the handover decision circuit. Moreover, the pre-regulator would be fully shutdown for power saving. Fig. 6(a) shows the proposed handover decision circuit. When $V_{\rm out2}$ exceeds the

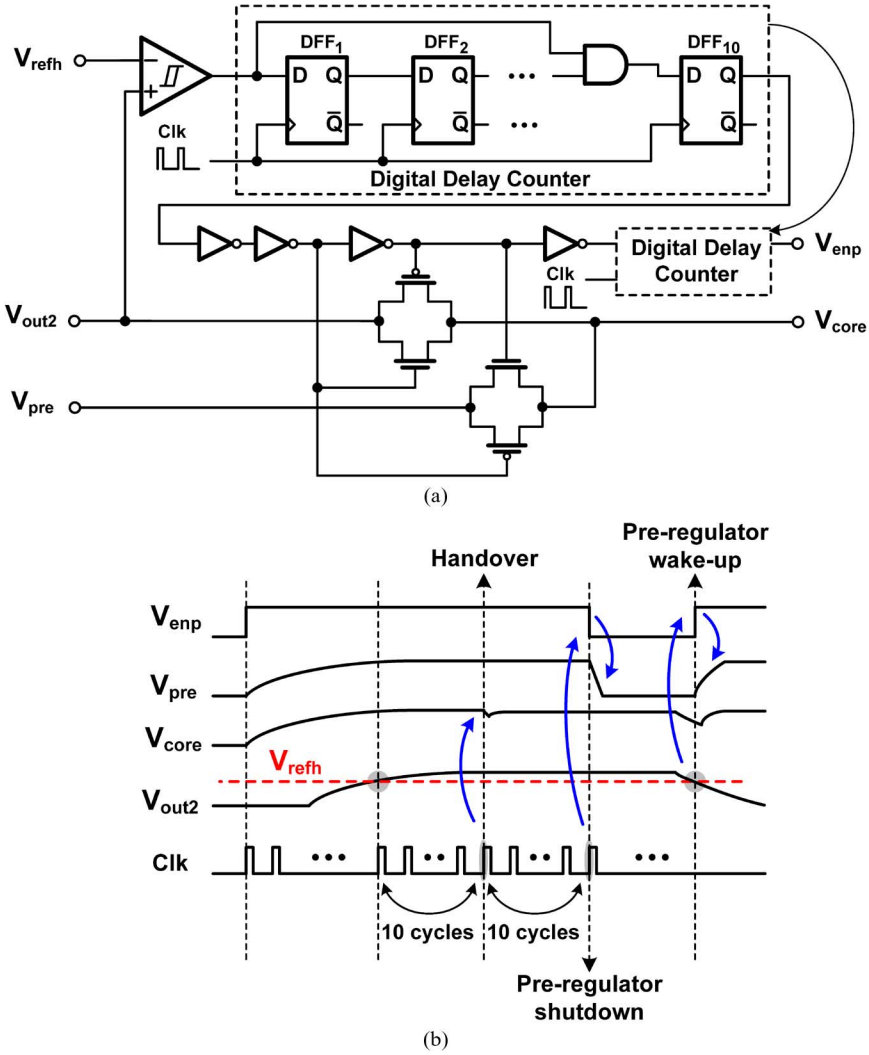

Fig. 6. (a) The handover decision circuit in the pre-regulator design. (b) Time diagram of the handover procedure.

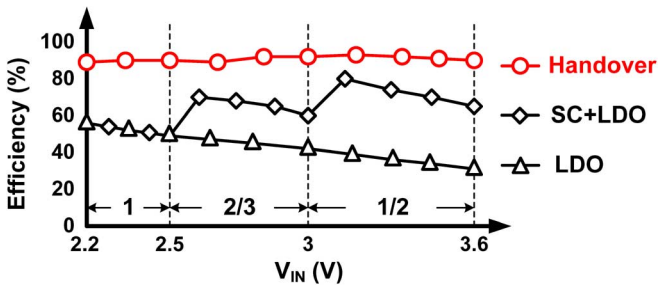

Fig. 7. The simulation results of the pre-regulator efficiency by LDO, SC converter with cascaded LDO circuit, and the handover technique.

predefined reference voltage of $V_{\rm refh}$, which is 0.9 V in this design, the handover decision circuit starts to switch the low supply voltage from $V_{\rm pre}$ to $V_{\rm out2}$ in order to activate the self-biasing mechanism. On the other hand, the digital delay counter can avoid the abnormal operation due to switching noise while the handover procedure. After a delay decided by the digital delay counter, $V_{\rm out2}$ is directly conducted to V_{core} to supply the LV-PWM controller through the transmission gate. Furthermore, the pre-regulator will be shutdown subsequent to the handover to reduce power dissipation. The time diagram of the handover procedure is illustrated in Fig. 6(b).

For safety operation, the pre-regulator needs to wake up when the UWB system enters the silent mode and disables $V_{\rm out2}$. When the UWB system enters the silent mode, the UWB processer will send a message to the power management module to inform the SC converter and the LDO circuit to supply the LV-PWM controller again. That is, the regulated voltage $V_{\rm pre}$ would supply the LV-PWM controller immediately to ensure correct operation of the power management. Fig. 7 shows the simulated efficiency comparison of the different pre-regulator designs. With automatic adjustment of the conversion factor for the SC converter, efficiency can be kept at 50% to 80%. However, the efficiency finally decreases to the same value as that of the pre-regulator implemented by only one LDO circuit. Fortunately, the handover technique can achieve the self-biasing mechanism and fully shutdown the SC converter to reduce power dissipation. Thus, efficiency can be obviously enhanced over a wide input supply voltage range.

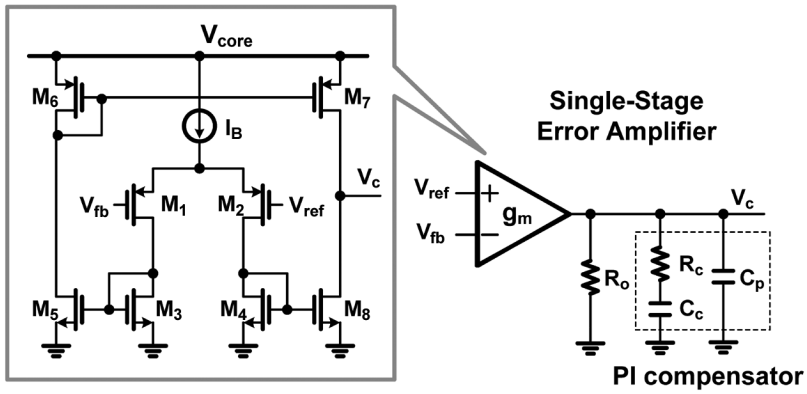

Fig. 8. The single-stage error amplifier with a PI compensator in low-voltage operation.

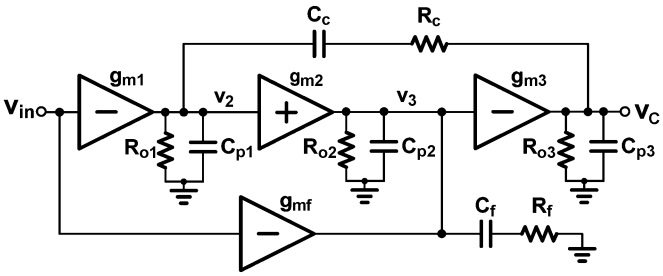

Fig. 9. The proposed CEMA structure expressed by the open loop format.

B. Compensation Enhancement Multistage Amplifier (CEMA)

The LV-PWM controller features the advantages of small silicon area and low power consumption compared to the conventional design utilizing only high-voltage I/O devices. However, there are some design challenges due to the deep-submicron devices that need to be overcome. Low supply voltage, typically 1.2 V in the core device of 65 nm technology, restricts the use of a conventional cascode structure. The cascode structure is used in a single-stage error amplifier in the conventional design under high supply voltage to increase the output impedance for high gain [2]. Thus, voltage gain of the error amplifier would be limited in low-voltage operation, which implies a deteriorated regulation performance.

Fig. 8 shows the single-stage error amplifier without the cascode structure that can be utilized under low supply voltage. The transfer function, $L_1(s)$, of the single-stage error amplifier is expressed in (2). The proportional-integral (PI) compensator can generate two poles, ω_{pL1} and ω_{phL1}, and one zero, ω_{zL1}. The low-frequency pole ω_{pL1} acts as the system dominate pole. The zero ω_{zL1} is used to cancel the effect of the output filter pole in the current programmable control DC-DC buck converter. In addition, the high-frequency pole ω_{phL1} can filter out the switching noise of the error signal. However, this single-stage structure cannot derive high gain and needs a large compensation capacitor C_c to maintain system stability. The large C_c is difficult to implement in the chip owing to the tremendous silicon cost of the advanced technology.

$$L_1(s) \approx \frac{g_m R_o (1+sC_cR_c)}{(1+sC_cR_o)(1+sC_pR_c)} = \frac{g_m R_o \left(1+\dfrac{s}{\omega_{zL1}}\right)}{\left(1+\dfrac{s}{\omega_{pL1}}\right)\left(1+\dfrac{s}{\omega_{phL1}}\right)} \tag{2}$$

Therefore, the structure of the error amplifier should be modified to achieve high voltage gain under low-voltage operation. To increase DC voltage gain of the error amplifier for further enhancing the loop gain, the proposed CEMA is utilized in Fig. 9. Owing to the cascaded structure [19], [20], voltage gain of the multistage amplifier can be increased in low-voltage operation. The structure is basically composed of three gain stages for high gain and one feed-forward gain stage for the generation of one compensation zero. The $L_2(s)$ is the transfer function of the CEMA and is expressed in (3), shown at the bottom of the page.

The open loop gain of the CEMA is increased by the multistage structure compared to the single-stage error amplifier. Moreover, the generated low-frequency pole-zero pair, ω_{pL2} and ω_{zL2}, can guarantee system stability. Following Miller's theorem, the pole, ω_{pL2}, given by (4) through the use of a

$$L_2(s) \approx \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left[1+s\left(R_cC_c+\frac{g_{mf}R_{o1}C_c}{g_{m1}g_{m2}R_{o1}+g_{mf}}+R_fC_f\right)+s^2\frac{g_{m1}g_{m2}R_{o1}R_cR_fC_cC_f}{g_{m1}g_{m2}R_{o1}+g_{mf}}\right]}{(1+sC_cg_{m2}g_{m3}R_{o1}R_{o2}R_{o3})\left[1+s\left(\frac{(C_f+C_{p2})(C_c(R_{o1}+R_{o3}+R_c)+C_{p3}R_{o3})}{C_cg_{m2}g_{m3}R_{o1}R_{o3}}+\frac{C_{p3}(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}R_{o2}}\right)+s^2\frac{C_{p3}(C_f+C_{p2})(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}}\right]}$$
$$= \frac{g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3}\left(1+\frac{s}{\omega_{zL2}}\right)\left(1+\frac{s}{\omega_{zhL2}}\right)}{\left(1+\frac{s}{\omega_{pL2}}\right)\left(1+\frac{s}{\omega_{ph1L2}}\right)\left(1+\frac{s}{\omega_{ph2L2}}\right)} \tag{3}$$

small on-chip capacitor C_c of 5 pF, is treated as the system dominant pole. The compensation zero, ω_{zL2} as expressed in (5), is generated by the feed-forward gain stage in the CEMA and the on-chip compensation resistor R_c which can further push ω_{zL2} toward low frequencies for the sake of an adequate phase margin.

$$\omega_{pL2} = \frac{1}{C_c g_{m2} g_{m3} R_{o1} R_{o2} R_3} \tag{4}$$

$$\omega_{zL2} \approx \frac{g_{m1} g_{m2}}{C_c (g_{mf} + R_c g_{m1} g_{m2})} \tag{5}$$

C_c, C_f, R_c and R_f are the compensation components of the CEMA structure in Fig. 9. According to the transfer function in (3), assuming that the flying capacitor, C_f, would not be inserted to compensate for the system, high-frequency complex poles that come from the parasitic capacitance of gain stages will cause a gain peaking to affect the stability of power management. Furthermore, the additional R_c will also further move the complex poles toward the right-half plane (RHP) when C_f is not implemented by (6), and would induce a higher gain peaking in frequency response than that in $L_2(s)$ without using C_f and R_c. Thus, system stability will worsen.

$$\frac{1}{4}\left(\frac{C_{p3}(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}R_{o2}}\right)^2 \le \frac{C_{p2}C_{p3}(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}} \tag{6}$$

As mentioned above, the utilization of C_f is necessary especially for applying the compensation resistor R_c in the proposed CEMA. The capacitor C_f of 2 pF is used to separate the high-frequency complex poles to two real poles in the frequency domain [21], [22] as illustrated in Fig. 10. Consequently, gain peaking can be eliminated by the pole-splitting result. From (3), the insertion of C_f guarantees the non-complex poles as expressed in (7). Therefore, the magnitude response with this compensated cascade amplifier, CEMA, of the DC-DC converter can approach 0 dB with a slope of only -20 dB/dec without being affected by the non-dominant poles.

$$\left(\frac{(C_f+C_{p2})\left(C_c(R_{o1}+R_{o3}+R_c)+C_{p3}R_{o3}\right)}{C_c g_{m2} g_{m3} R_{o1} R_{o3}} + \frac{C_{p3}(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}R_{o2}}\right)^2 \ge 4\frac{C_{p3}(C_f+C_{p2})(R_{o1}+R_c)}{g_{m2}g_{m3}R_{o1}} \tag{7}$$

A comparison of these three different type error amplifiers in the frequency domain is shown in Fig. 10. The $L_1(s)$ from the single-stage error amplifier has a DC voltage gain smaller than 40 dB, which cannot guarantee a regulated output driving voltage in the power management module. Meanwhile, $L_2(s)$ from the proposed CEMA due to the multistage structure can effectively provide a high voltage gain even in a low supply voltage operation of 1 V. That is, DC voltage gain can be raised higher than 80 dB to achieve good regulation performance, which is required in UWB systems. In addition, the compensation zero enhancement and the non-dominant pole splitting in CEMA are also indicated. The location of the output filter pole of DC-DC converter is also indicated in Fig. 10. The system phase margin varies from 55 to 80 degrees under different load condition.

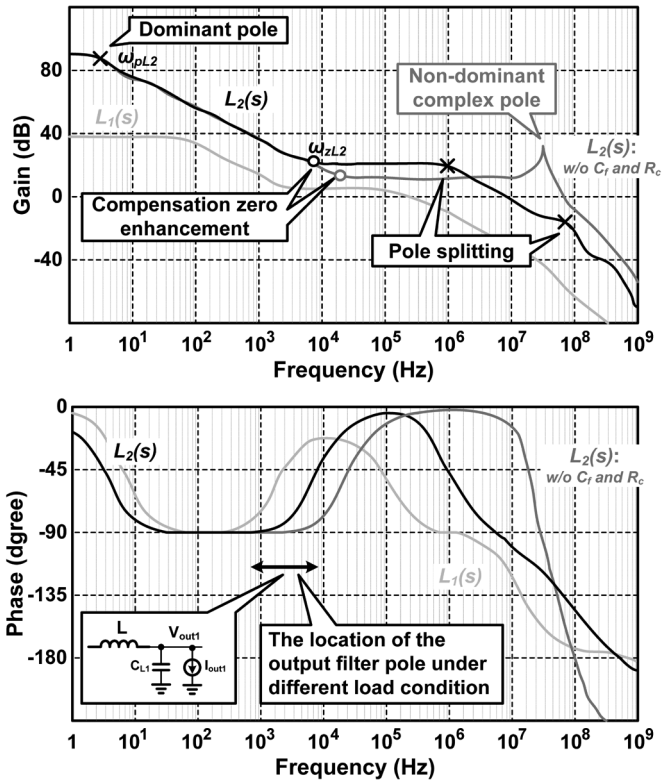

Fig. 10. The comparison of the three different error amplifiers in frequency response.

Fig. 11 depicts the schematic of the CEMA circuit. The transistors M_7 and M_8 constitute the first gain stage. The second stage is composed of the transistor M_{11} with a current mirror to obtain a positive gain. Additionally, M_{14} constitutes the third gain stage. The feed-forward stage is composed of the transistors M_{f1} and M_{f2}. The equivalent resistance R_f in Fig. 9 is composed of the diode-connected transistor M_9 and has an equivalent resistance of $1/g_{m9}$. The schematic of the CEMA is supplied by V_{core}, which is generated from $V_{\rm pre}$ or $V_{\rm out2}$ and has a wide range from 1.0 V to 1.3 V owing to the handover technique. Thus, the proposed CEMA structure operates in the low-voltage supply to overcome the small voltage headroom in analog design and achieve the on-chip compensation by utilizing two small capacitors simultaneously. Moreover, compared to the single-stage error amplifier in low-voltage operation, fast transient response and good regulation are achieved by the CEMA owing to its enhanced loop gain and optimum system compensation. This feature of the power management is suitable for the SoC applications.

C. Dynamic Voltage Scaling (DVS) and Post-Regulator

The DVS function is implemented with the post-regulator, which is a low-dropout regulator with an impedance attenuation buffer stage as shown in Fig. 12. The dominant pole of the post-regulator is at the output node due to the large output capacitor C_{L2}. The non-dominant poles, which appear at n_1 of the error amplifier output node and at n_2 of the gate of power transistor M_P, degrades the phase margin [23]. The buffer stage, which contains $M_9 - M_{13}$ and R_B, can separate the non-dominant

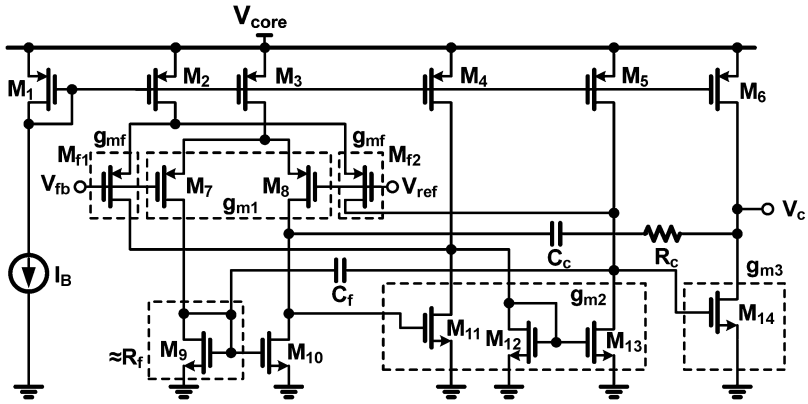

Fig. 11. Schematic of the proposed CEMA.

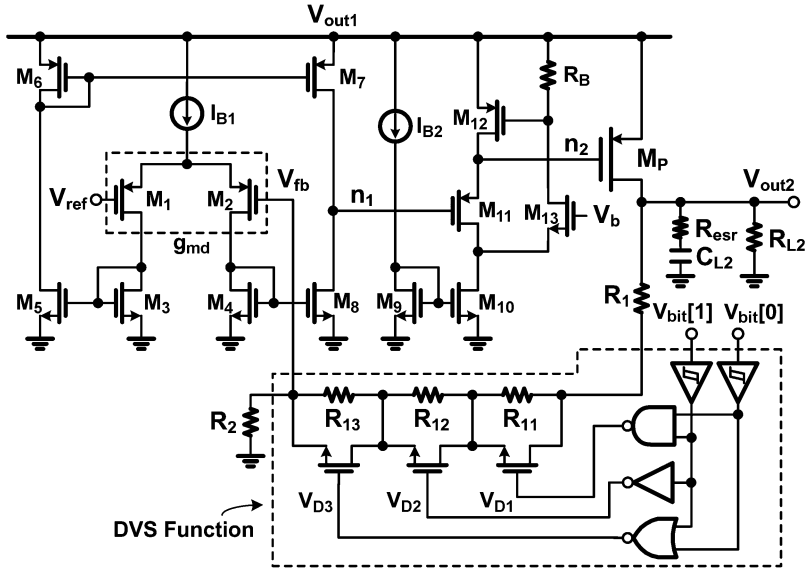

Fig. 12. The schematic of the post-regulator with DVS function.

poles by reducing the output impedance $R_{o,n2}$ at node n_2 given by (8):

$$R_{o,n2} \approx \frac{R_B}{g_{m11}r_{o11}g_{m13}r_{o13}(1+g_{m12}R_B)} \approx \frac{1}{g_{m11}g_{m12}g_{m13}r_{o11}r_{o13}}. \quad (8)$$

Owing to the flipped voltage follower structure in the buffer stage, $R_{o,n2}$ is greatly decreased [24]. The R_B is designed to achieve a correct biasing path for M_{13}. Thus, the non-dominant pole generated by the parasitic gate capacitance of power transistor M_P and $R_{o,n2}$ would be pulled to high frequency, which has no deterioration to the phase margin.

Moreover, the open-loop transfer function of the post-regulator $L_{\rm post}(s)$ is given by (9). The g_{md} is the transconductance of the error amplifier in the post-regulator, while C_{pn1} and C_{pn2} are the parasitic capacitances at node n_1 and n_2, respectively. The R_{oL} is the equivalent resistance at $V_{\rm out2}$. R_{opass} is the equivalent resistance of M_P, and R_{L2} is the load resistance of the post-regulator. Furthermore, owing to the flipped voltage follower structure in the buffer stage, the required quiescent current and the aspect ratio of M_{11} can be minimized simultaneously.

$$L_{\rm post}(s) \approx \frac{R_2}{R_1+R_2} \times \frac{g_{md}g_{mp}R_{o,n1}R_{oL}(1+sC_{L2}R_{esr})}{(1+sC_{L2}R_{oL})(1+sC_{pn1}R_{o,n1})(1+sC_{pn2}R_{o,n2})}$$
$$\text{where} \quad R_{oL} = R_{opass}\|R_{L2}\|(R_1+R_2). \quad (9)$$

$V_{\rm out2}$ is dynamically adjusted from 1 V to 1.3 V for the DVS function. The two-bit signal, V_{bit}, generated from the UWB processer indicates the power request. In the DVS operation, the processer in UWB is the master unit and the post-regulator in power management is the slave unit. The DVS function can scale down the supply voltage to minimize power consumption and return it to the standard value before data transmission. Additionally, the LV-PWM controller is designed to operate under a 1 V supply voltage since the handover technique would directly connect the supply voltage of LV-PWM controller from $V_{\rm out2}$.

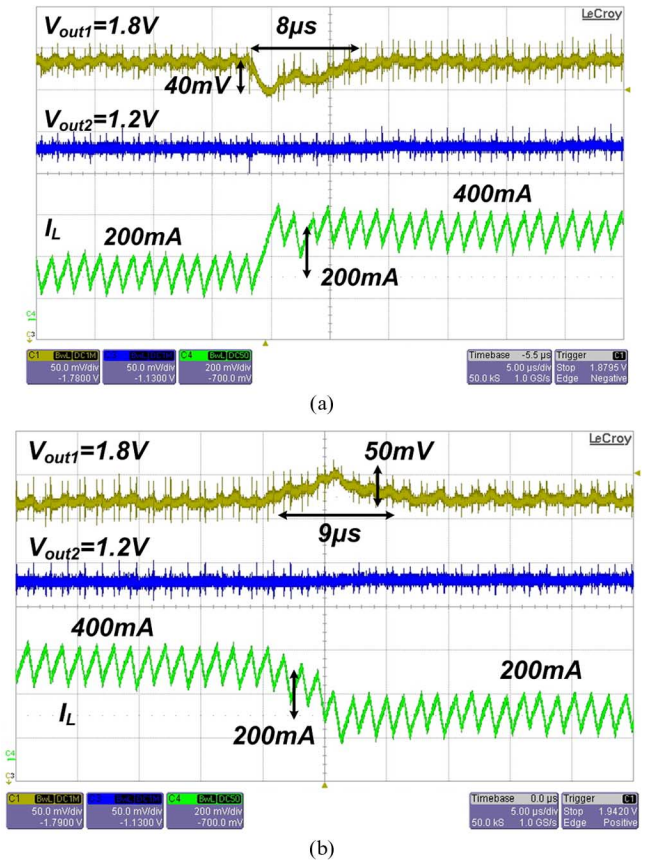

Fig. 13. Measured result of load transient response with a load step of 200 mA. (a) The load current changes from 200 mA to 400 mA. (b) The load current changes from 400 mA to 200 mA.

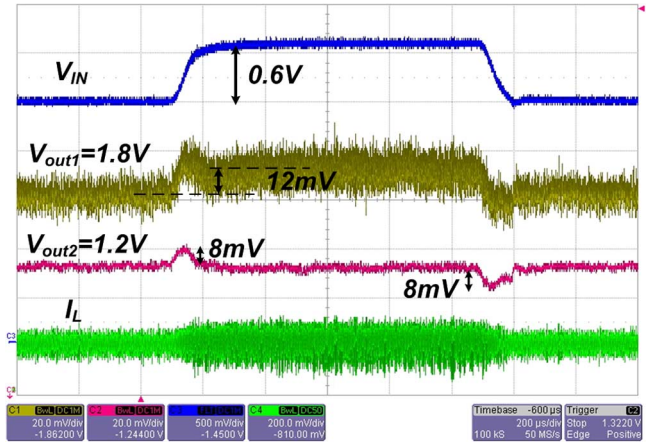

Fig. 14. Measured result of line transient response when $V_{\rm IN}$ has a 0.6 V voltage step.

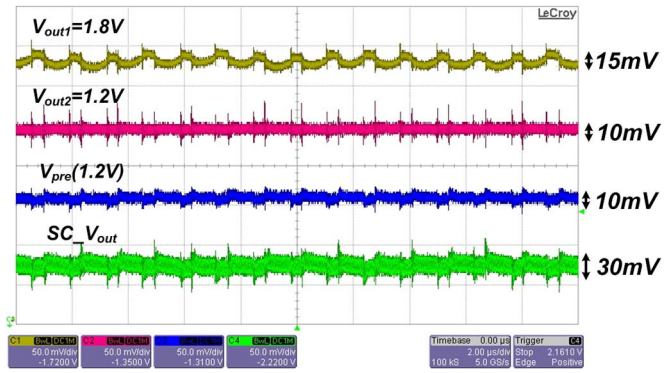

Fig. 15. Measured result of the pre-regulator: Output voltage of the SC converter, $SC\_V_{\rm out}$, and the SC converter with cascaded LDO circuit, $V_{\rm pre}$ (typically 1.2 V).

IV. Measurement Results

The proposed power management module with the LV-PWM controller was fabricated by 65 nm CMOS technology. Fig. 13 shows the load transient response from 200 mA to 400 mA and vice versa. The first output voltage $V_{\rm out1}$ is 1.8 V with the voltage ripple about 15 mV. The undershoot voltage is 40 mV (2.2%) and the recovery time is 8 μs when load current changes from 200 mA to 400 mA. On the other hand, the overshoot voltage is 50 mV (2.7%) and the recovery time is 9 μs when load current changes from 400 mA to 200 mA.

Owing to the design of CEMA, which provides high system loop gain in the low-voltage operation, the load regulation of $V_{\rm out1}$ is 25 mV/A @ $V_{\rm IN} = 3.3$ V. The internal IR voltage drop across the bond-wire and Quad Flat Non-leaded (QFN) substrate routes may also cause regulation error in test chip. Moreover, the variation of $V_{\rm out1}$ is about 12 mV when $V_{\rm IN}$ has a 0.6 V voltage step as shown in Fig. 14. The line regulation of $V_{\rm out1}$ is 20 mV/V when load current is 200 mA.

The measured output voltage of the SC converter $SC\_V_{\rm out}$ and the output voltage of the cascaded LDO circuit $V_{\rm pre}$ are shown in Fig. 15. The output ripple of the pre-regulator is suppressed to 10 mV by the LDO circuit. As a result, a nearly constant voltage of 1.2 V can supply the LV-PWM controller. In addition, the pre-regulator efficiency is always kept higher than 50% owing to the power conditioning circuit. Fig. 16 shows the handover technique. When the second output voltage $V_{\rm out2}$ is enabled from the UWB system and exceeds over the predefined voltage value of 0.9 V, the handover technique would be activated. The $V_{\rm out2}$ can be connected to the V_{core} directly to supply the LV-PWM controller for self-biasing mechanism. Meanwhile, the SC converter and the cascaded LDO circuit in the pre-regulator will be shutdown. A small output variation of 150 mV at $V_{\rm out1}$ may be induced during the handover period. On the other hand, the SC converter and the cascaded LDO circuit in the pre-regulator would be reactivated when $V_{\rm out2}$ is below 0.9 V. This indicates that the UWB system probably enters the power-saving mode and disables the second output voltage of the power management module. Thus, the handover technique can reduce power dissipation of the pre-regulator and ensure the correct operation of the integration with the UWB system.

Fig. 17 shows the measured result of the DVS function. When the UWB system sends the two bit power request message, V_{bit}, to the power management, the second output voltage $V_{\rm out2}$ can be adjusted immediately to supply the UWB system. The range of $V_{\rm out2}$ would vary from 1 V to 1.3 V. Thus, the LV-PWM controller has to ensure correct operation at 1 V supply for matching up the handover technique. This DVS function also demonstrates the high integration between the power management and the UWB system.

Fig. 18 shows the power conversion efficiency of the proposed power management module. The handover technique can

TABLE I
DESIGN SPECIFICATIONS OF UWB AND THE PROPOSED POWER MANAGEMENT MODULE

Technology		65nm CMOS process	
Input voltage		2.2 V - 3.6 V	
Inductor (off-chip)		4.7 µH	
On-chip compensation capacitor		5 pF and 2 pF	
Switching frequency		800 KHz	
Outputs		1.8 V (DC-DC converter)	1 V - 1.2 V (1.3 V Max.) (Low dropout regulator)
Capacitor (off-chip)		4.7 µF	4.7 µF
Maximum load current (UWB requirement / Measured)		300 mA / 400 mA	150 mA / 200 mA
Line regulation	UWB req.	30 mV/V @ Load = 200 mA	30 mV/V @ Load = 50 mA
	Measured	20 mV/V @ Load = 200 mA	15 mV/V @ Load = 50 mA
Load regulation	UWB req.	50 mV/A @ V_{IN} = 3.3 V	100 mV/A @ V_{out1} = 1.8 V
	Measured	25 mV/A @ V_{IN} = 3.3 V	85 mV/A @ V_{out1} = 1.8 V
Power conversion efficiency		Max. 93 %	
Proposed chip active area		734 µm x 486 µm	
DVS function (UWB requirement / Measured)			
Transient time (0.1 V step)		10 µs / 6 µs	
Silence/Wakeup time		40 µs / 32 µs	

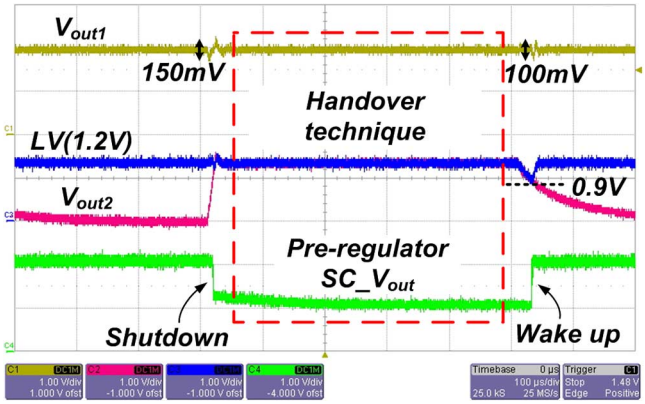

Fig. 16. Measured result of the handover technique.

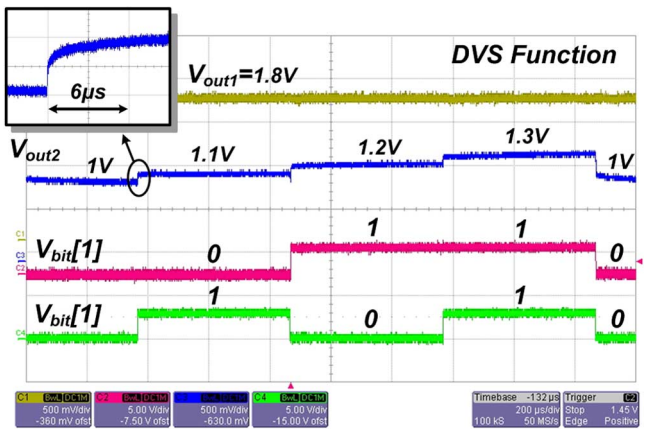

Fig. 17. Measured result of the DVS function.

enhance efficiency at all light and heavy loads. Fig. 19 shows the chip micrograph of the complete UWB system with the embedded power management module. The chip photo of the power management module is emphasized at the left side, which occupies 0.356 mm^2. The active area is effectively reduced by 30% owing to the LV-PWM controller compared to the conventional design [2] with high-voltage devices (3.3 V I/O devices)

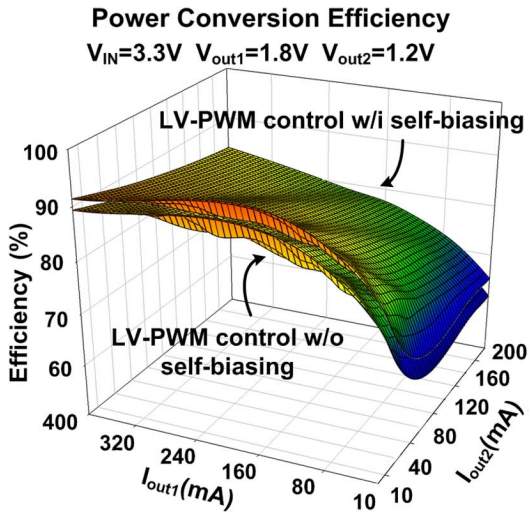

Fig. 18. The measured power conversion efficiency.

only. Besides, a LDO is placed near the RF circuit to suppress the voltage ripple from the DC-DC converter. The detailed design specification is shown in Table I.

V. CONCLUSIONS

The proposed power management module with low-voltage PWM controller and DVS function was fabricated by 65 nm CMOS technology to integrate with the UWB system. The high efficiency pre-regulator with power conditioning circuit can provide a regulated supply voltage to the LV-PWM controller, which is implemented by low-voltage core devices of 65 nm technology. Additionally, the handover technique can achieve the self-biasing mechanism to further enhance the efficiency. Even under low supply input voltage, the proposed CEMA can increase the loop gain and stabilize the system without using large external compensation components. Experimental results demonstrate the good performance of voltage regulation and transient response. Owing to the DVS function, the proposed power management can meet the UWB system's power request. The fabricated power management module

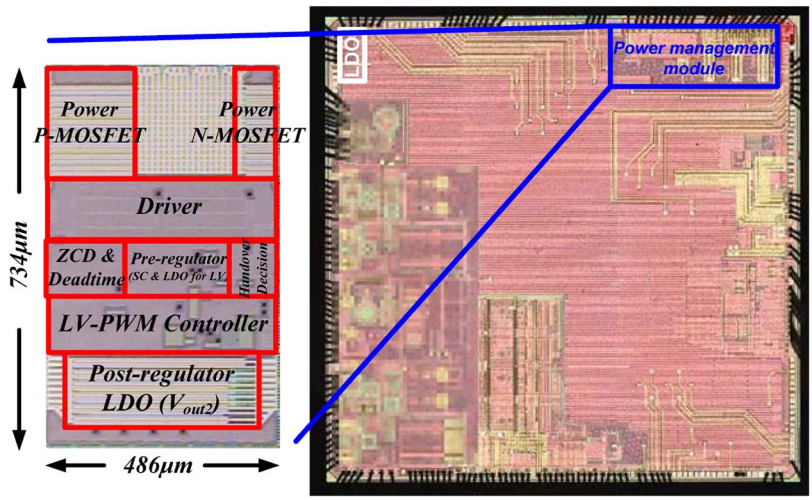

Fig. 19. Chip micrograph with the UWB system and the enlarged proposed power management module.

occupies a 0.356 mm^2 silicon area and has the qualification to be integrated in SoC applications.

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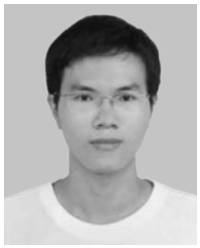

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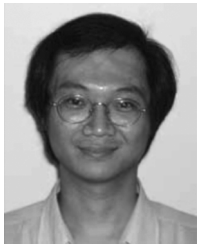

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