Self-Heating Effect on Bias-Stressed Reliability for Low-Temperature a-Si:H TFT on Flexible Substrate

Shih-Chin Kao, Hsiao-Wen Zan, Jung-Jie Huang, and Bo-Cheng Kung

***Abstract*—Hydrogenated amorphous silicon thin-film transistors on colorless polyimide substrates were successfully fabricated at a low process temperature (160 °C). The gate leakage current is as low as 10^{-13} A, while the field-effect mobility is 0.42 $cm^2V^{-1} \cdot s^{-1}$, and the subthreshold swing is 0.77 V/dec. Using bias-temperature stress on devices with different channel widths, the enhancement of self-heating effect on bias-stressed reliability is investigated for the first time. Elevated temperature due to self-heating effect is estimated either by extending the bias-stressed model or by modifying the thermal equivalent circuit model. Degradation of device reliability on a bent substrate is also significant when self-heating effect is incorporated.**

***Index Terms*—Flexible, hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT), reliability, self-heating.**

I. Introduction

HYDROGENATED amorphous silicon thin-film transistors (a-Si:H TFTs) fabricated on plastic substrates have drawn a lot of attention in the past decade [1], [2]. Compared with glass substrates, plastic substrates have advantages such as flexibility, lightness, thinness, and reduced incidences of breakage. Many reports have successfully demonstrated the fabrication of a-Si:H TFTs on plastic substrates [3], [4]. However, when plastic substrates are used, the process temperature usually has to be lower than 180 °C. Depositing low-leakage dielectric and low-defect a-Si:H layers at such a low temperature is a great challenge. Low-temperature a-Si:H TFTs on plastic substrates also exhibit more significant bias-stress-induced reliability issues than a-Si:H TFTs fabricated at standard temperature (250−300 °C) on glass substrates [5]. After prolonged gate bias stress, a pronounced threshold voltage shift (ΔV_T) was observed. The charge trapped inside the dielectric layer (silicon nitride) and the creation of dangling bonds in an a-Si:H film are two major reasons for ΔV_T. Some also reported that when gate bias stress is applied under a high temperature, dielectric-trapped charges emitted from a defective gate dielectric to an a-Si:H layer increase gate leakage current and generate abnormal ΔV_T [6].

Using plastic substrates not only limits the process temperature but also causes a serious self-heating effect. As will be discussed later in this paper, a-Si:H TFTs on plastic substrates can exhibit a more pronounced self-heating effect than those on glass substrate cans since plastic substrates usually have a larger thermal resistance than glass substrates. According to the study on self-heating effects in a-Si:H TFTs reported by Wang *et al.* [7], heat dissipation to the ambient is primarily through the gate, the source, and the drain contacts. The path through the gate contact via the gate insulator is the most effective. When heat dissipates through the gate contact, the thermal resistance of the substrate dominates the thermal dissipation from the gate contact to the ambient. We propose that using a plastic substrate instead of a glass substrate increases the thermal resistance of the substrate and, hence, enhances the self-heating effect in a-Si:H TFTs. In this paper, it is found that the heat dissipation problem, together with the defective a-Si:H film deposited at a low temperature, causes a serious self-heating-enhanced bias-stress effect for a-Si:H TFTs on a plastic substrate.

In this study, we use a colorless 18 × 18 cm^2 and 40-μm-thick polyimide (PI) substrate with transmittance of visible light ($\lambda = 400-700$ nm) of nearly 90% [2]. With a process temperature lower than 160 °C, mobility, threshold voltage, and subthreshold swing of a-Si:H TFTs are 0.42 $cm^2/V.s$, 7 V, and 0.77 V/decade, respectively. With various kinds of bias stress (gate bias stress and two-terminal bias stress in which the gate stress and drain bias stress are applied simultaneously) at temperatures ranging from 25 °C to 60 °C, a stable gate dielectric property is verified when the gate leakage current is kept as low as 10^{-13} A/cm^2. When different amounts of drain bias stress are applied on devices with different channel widths, influences of channel carrier concentration and self-heating effect on ΔV_T are investigated. Finally, the substrate bending effect on the self-heating enhanced ΔV_T is also discussed.

II. Experimental

Bottom-gate a-Si:H TFTs with a back-channel-etch structure were fabricated on clear PI substrates. First, a Ti/Al/Ti trimetal layer with a total thickness of 200 nm was deposited by radio frequency sputtering and then patterned by dry etching to form the gate electrodes. Internal stress of Ti and Al are compensated, preventing the cracking of the PI substrate. Second, SiN_x, a-Si:H, and n^+ a-Si:H films were sequentially deposited by plasma-enhanced chemical vapor deposition at 160 °C. The thicknesses of SiN_x, a-Si:H, and n^+ a-Si:H layers were 300, 200, and 50 nm, respectively. An active island was then formed by the island etching process. The source/drain metals were deposited and defined by dry etching to form the source/drain electrodes. Then, the n^+ layer region between the source and drain electrodes was etched away. Finally, a 300-nm-thick SiN_x was deposited as the passivation layer.

Gate bias stress and two-terminal bias stress were applied to devices with a channel width that varied from 10 to 80 μm

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S.-C. Kao and H.-W. Zan are with the Department of Photonics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

J.-J. Huang and B.-C. Kung are with the Display Technology Center, Industrial Technology Research Institute, Hsinchu 310, Taiwan (e-mail: hsiaowen@mail.nctu.edu.tw).

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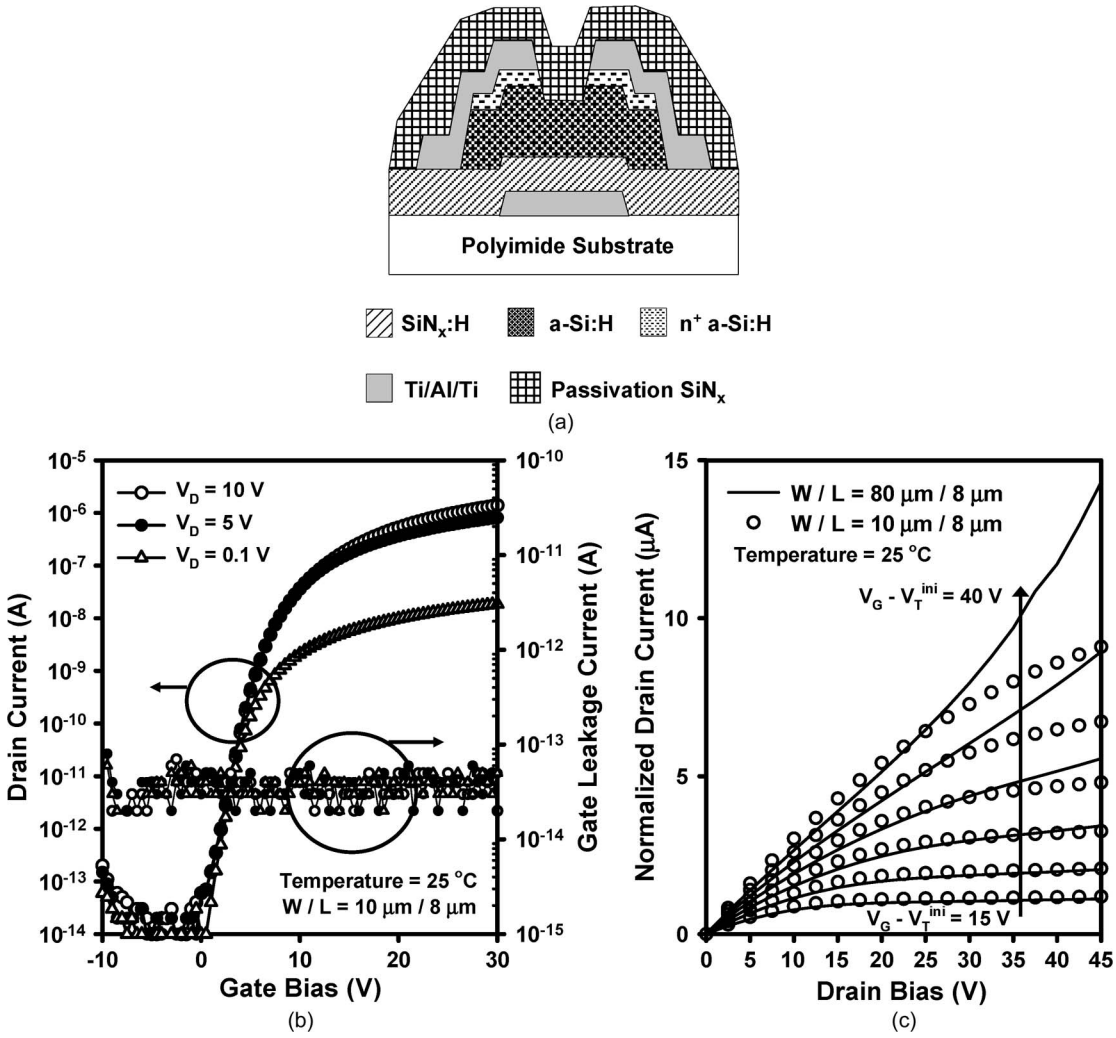

Fig. 1. (a) Schematic diagram of the bottom-gate a-Si:H TFT on a PI substrate. (b) Transfer characteristics and (c) output characteristics of the bottom-gate a-Si:H TFT fabricated at 160 °C on a PI substrate.

while channel length was fixed at 8 μm. When gate bias stress was applied, the source and the drain were connected to ground. Electron carriers are uniformly accumulated in the channel, and no current passes through the device channel. When two-terminal bias stress was used, gate bias minus threshold voltage was equal to drain bias (i.e., $V_D = V_G - V_T^{\rm ini}$) while the source was grounded, where $V_T^{\rm ini}$ is the initial threshold voltage before stress. The device enters the saturation region and causes the depletion region near the drain electrode. The electron concentration in the channel is not uniform and electron carriers pass through the device channel. Electrical characteristics of devices were measured using an HP 4156A electrical analyzer to extract $V_T^{\rm ini}$, the threshold voltage (V_T), the field-effect mobility $(\mu_{\rm FE})$, and the subthreshold slope (SS).

III. Results and Discussion

The schematic diagram of the bottom-gate a-Si:H TFT on the PI substrate is shown in Fig. 1(a). Fig. 1(b) and (c) shows the transfer and output characteristics of the fabricated devices, respectively. The ON/OFF current ratio at $V_D = 10$ V is greater than 10^7. The gate-to-source leakage current $(I_{\rm GS})$ is approximately 10^{-13} A. $\mu_{\rm FE}$ and SS are 0.42 cm^{2}V$^{-1}\cdot$s^{-1} and 0.77 V/dec, respectively. $\mu_{\rm FE}$ was extracted by using maximum linear-region transconductance (G_M). In Fig. 1(c), the normalized drain current $(I_{\rm DSN} = I_{\rm DS} \times {\rm L/W})$ of devices with channel widths of 10 and 80 μm are compared. Under small drain bias, the $I_{\rm DSN}$ values of these two devices are similar. Under large drain bias, however, devices with a large channel width exhibit much larger $I_{\rm DSN}$ than those with a small channel width. When gate bias and drain bias are increased, devices with a large channel width lose saturation characteristics. Self-heating was proposed by Wang *et al.* to explain the observed nonsaturated drain current [7].

Then, gate bias stress effects at different temperatures are studied. Fig. 2(a) and (b) shows the transfer characteristics for devices before and after stress (stress condition: $V_G - V_T^{\rm ini} =$ 25 V, $V_D = V_S = 0$ V) at 25 °C and 60 °C, respectively. Gate bias stress causes a threshold voltage shift while $I_{\rm GS}$, $\mu_{\rm FE}$, and SS are almost unchanged. When temperature increases, the threshold voltage shift becomes more pronounced. Gate leakage current is kept as low as 10^{-13} A, indicating almost unchanged gate dielectric quality.

With identical gate leakage current, the larger ΔV_T produced at higher temperature may be due to the increased defect

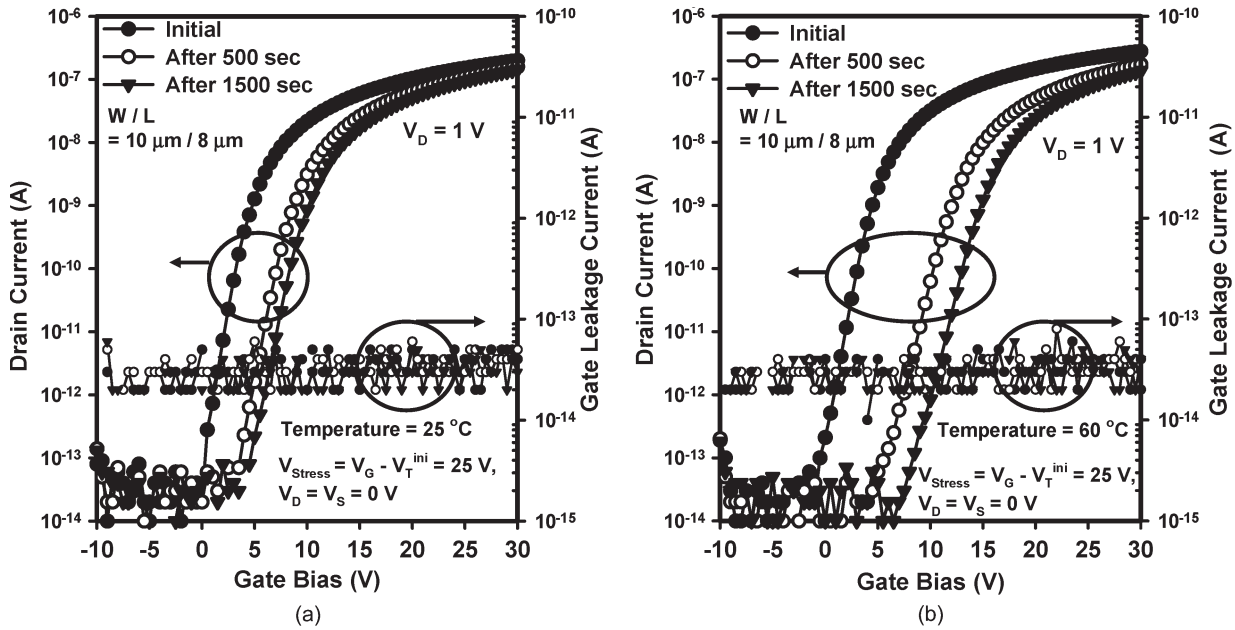

Fig. 2. Transfer characteristics of the bottom-gate a-Si:H TFT before and after applying 500- and 1500-s gate-bias stress transfer characteristics at a substrate temperature of (a) 25 °C and (b) 60 °C. Stress condition: $V_{\mathrm{Stress}} = V_G - V_T^{\mathrm{ini}} = 25$ V and $V_D = V_S = 0$ V. Gate leakage current is kept as low as 10^{-13} A.

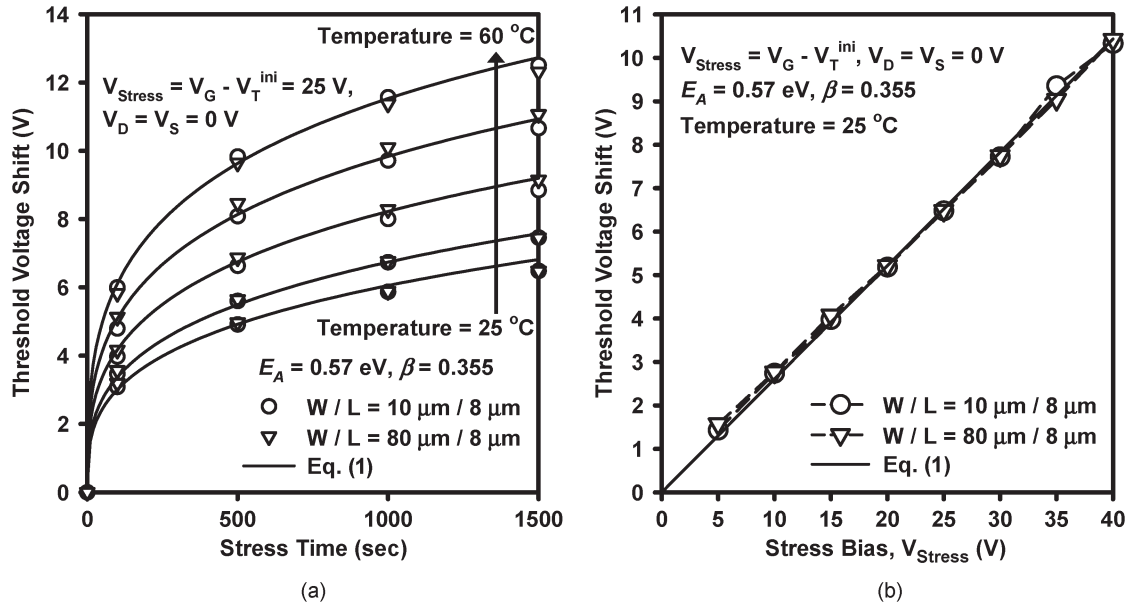

Fig. 3. (a) ΔV_T as a function of stress time at 25 °C, 30 °C, 40 °C, 50 °C, and 60 °C when $V_{\mathrm{Stress}} = V_G - V_T^{\mathrm{ini}} = 25$ V and $V_D = V_S = 0$ V. (b) ΔV_T under different stress bias $V_{\mathrm{Stress}} = V_G - V_T^{\mathrm{ini}}$ ($V_D = V_S = 0$ V) values after 1500 s at 25 °C is plotted as a function of V_{Stress}. The experimental data in Fig. 2(a) and (b) can be well explained by (1).

generation rate. According to the charged-state creation mechanism in an a-Si:H film, the defect generation rate is proportional to the carrier concentration and the effective carrier trapping time τ_t. τ_t can be expressed as $\tau_t = \nu^{-1}\exp(E_A/kT)$, where ν is an attempt to escape frequency, and E_A is the mean activation energy for the defect generation. ΔV_T, as a function of stressed gate bias and stress time, can be expressed by the following stretched exponential equation [8]:

$$V_T - V_T^{\mathrm{ini}} = \Delta V_T = \left(V_G - V_T^{\mathrm{ini}}\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\} \quad (1)$$

where V_T^{ini} is the initial threshold voltage. β is a weakly temperature-dependent dispersion parameter.

Fig. 3(a) depicts ΔV_T as a function of stress time at 25 °C, 30 °C, 40 °C, 50 °C, and 60 °C when $V_{\mathrm{Stress}} = V_G - V_T^{\mathrm{ini}} = 25$ V. Furthermore, ΔV_T under different stress bias V_{Stress} values after 1500 s at 25 °C is plotted as a function of V_{Stress} in Fig. 3(b). The experimental data in Fig. 3(a) and (b) can be well explained by (1), with E_A and β being 0.57 eV and 0.355, respectively. The constant value of β suggests that the weak temperature dependence of β can be neglected in this study. Increasing channel widths from 10 to 80 μm does not influence ΔV_T.

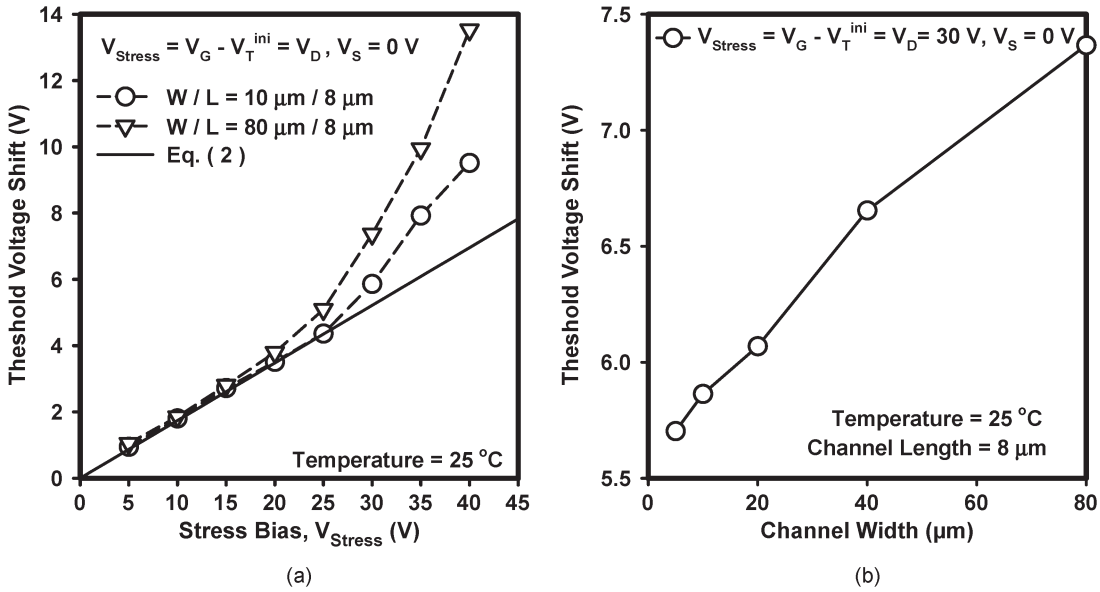

Fig. 4. (a) ΔV_T as a function of stress bias where $V_{\rm Stress} = V_G - V_T^{\rm ini} = V_D$, $V_S = 0$ V, stress time is 1500 s, and substrate temperature is 25 °C. (b) ΔV_T is plotted as a function of different channel widths.

It is also known that when ΔV_T is dominated by the state creation mechanism, drain bias modulates the average carrier concentration and influences ΔV_T [9]. If $V_{\rm Stress} = V_G - V_T^{\rm ini} = V_D$, ΔV_T can be expressed as

$$V_T - V_T^{\rm ini} = \Delta V_T = \frac{2}{3} \times \left(V_G - V_T^{\rm ini}\right) \left\{1 - \exp\left[-\left(\frac{t}{\tau_t}\right)^{\beta}\right]\right\}. \quad (2)$$

This two-terminal stress effect is observed in Fig. 4(a) by plotting ΔV_T as a function of stress bias $V_{\rm Stress}$ after stress time of 1500 s at 25 °C, where $V_{\rm Stress} = V_D = V_G - V_T^{\rm ini}$. For small $V_{\rm Stress}$, ΔV_T can be well explained by (2), verifying the influence of drain-bias-modulated carrier concentration, as in previous reports [9]. For large $V_{\rm Stress}$, however, significant deviation of ΔV_T from the theoretical curve is observed. The deviation is more pronounced when devices exhibit a larger channel width. This channel-width-enhanced ΔV_T is clearly observed when ΔV_T is plotted as a function of different channel widths, as shown in Fig. 4(b).

The above results can be explained by the following two possible reasons: 1) hot-carrier enhanced charge trapping and 2) self-heating effects. However, the generation of hot carriers is usually accompanied with a significant kink effect, although in our experiment, no obvious kink effect is observed from the device output characteristics. Additionally, when $V_{\rm Stress} = V_D = V_G - V_T^{\rm ini}$, devices are biased close to saturation points where the kink effect seldom appears. On the contrary, according to previous reports [7], self-heating is pronounced in a-Si:H TFTs due to the high resistive intrinsic a-Si:H films. The joule heat produced in a-Si:H film close to drain side increases device temperature and enlarges channel current. It is reported that heat dissipation is more effective at the channel edge than in the center region. As a result, devices with a larger channel width suffer from a severer self-heating effect [10].

To further characterize the self-heating effect, characteristic temperature ($T_{\rm ch}$) is extracted by fitting the measured ΔV_T with those calculated from (2) when we set different temperatures, as shown in Fig. 5(a). E_A and β are 0.57 eV and 0.355. In Fig. 5(b), $T_{\rm ch}$ is plotted as a function of $V_{\rm Stress}$ ($= V_D = V_G - V_T^{\rm ini}$) for devices with channel widths of 10 and 80 μm. Obviously, $T_{\rm ch}$ for both devices is 25 °C (room temperature) under low $V_{\rm Stress}$. When $V_{\rm Stress}$ is 40 V, $T_{\rm ch}$ rises up to 40 °C and 60 °C for devices with channel widths of 10 and 80 μm, respectively.

To justify the physical meaning of the characteristic temperature $T_{\rm ch}$, we calculate the increased temperature due to self-heating effect according to the physical model proposed by Wang *et al.* [7]. In their model, the temperature increase induced by self-heating effect ($\Delta T_{\rm SHE}$) can be calculated by using the thermal equivalent circuit and can be described as follows [11]:

$$\Delta T_{\rm SHE} = I_D \times V_{\rm DS} \times R_{\rm th} \quad (3)$$

where $R_{\rm total}$ is the total thermal resistance that includes the thermal resistances of different heat dissipation paths and the thermal resistance of the substrate. As aforementioned, heat dissipation is dominated by the path through the gate contact and substrate. In addition, the thermal resistance of the substrate can be given as [7]

$$R_{\rm sub} = \frac{1}{\pi k W} \ln\left(\frac{16D}{\pi L}\right) \quad (4)$$

where k and D are the thermal conductivity and the thickness of the substrate, respectively, and W and L are the channel width and length of the a-Si:H TFT, respectively. Thermal conductivity of the PI substrate is about 0.2 W $\cdot$ m^{-1}K^{-1} [12]. By using (4), the thermal resistance of the PI substrate is calculated to be 6.4×10^4 K/W when a channel width of 80 μm and a channel length of 8 μm are considered. The thermal resistance of the PI substrate is about two times higher that

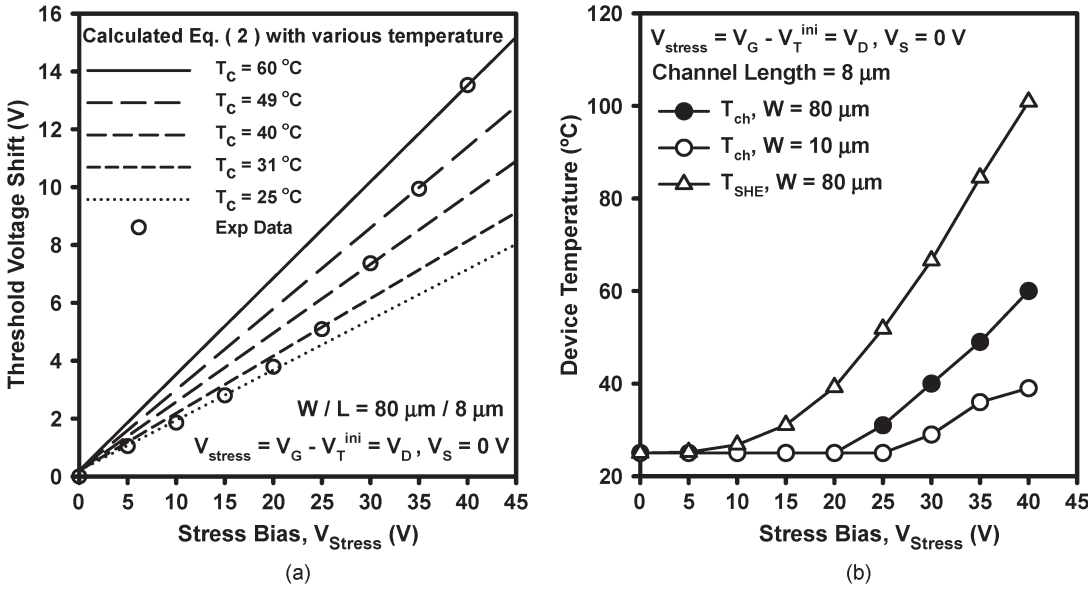

Fig. 5. (a) Characteristic temperature $(T_{\rm ch})$ extraction by fitting the measured ΔV_T with those calculated from (2). (b) Extracted $T_{\rm ch}$ as a function of stress bias for devices with channel widths of 10 and 80 μm, respectively. Temperature calculated by the modified self-heating effect model $(T_{\rm SHE})$ for devices with a channel width of 80 μm after a stress time of 1500 s is also plotted by triangular symbols. Stress bias $V_{\rm Stress} = V_G - V_T^{\rm ini} = V_D$, $V_S = 0$ V. The channel length is fixed at 8 μm.

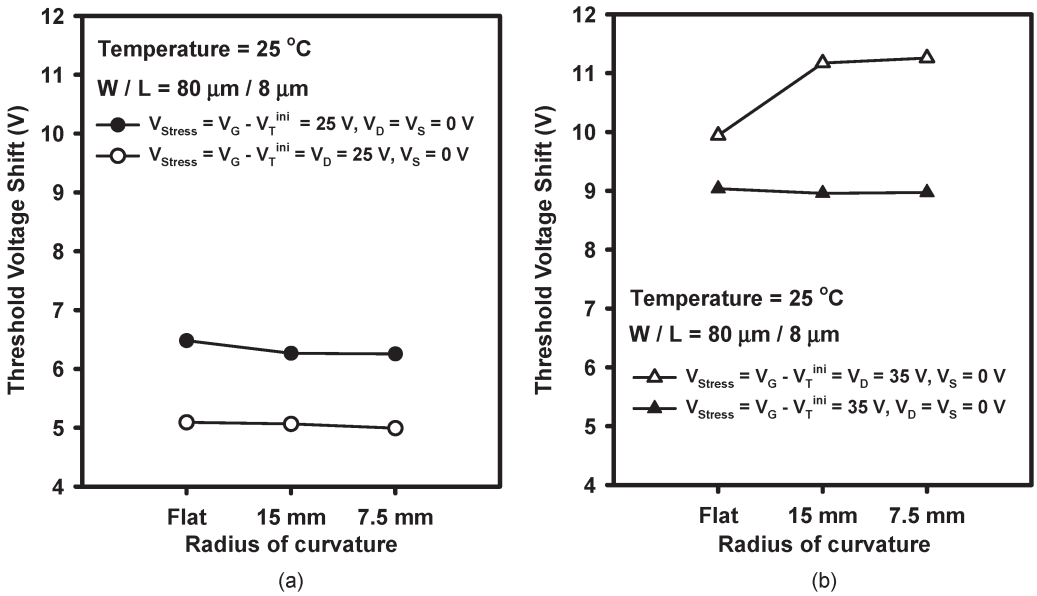

Fig. 6. Comparison of ΔV_T for a wide-channel device on flat and bent substrates when (a) $V_{\rm Stress} = V_G - V_T^{\rm ini} = V_D = 25$ V or $V_{\rm Stress} = V_G - V_T^{\rm ini} =$ 25 V and (b) $V_{\rm Stress} = V_G - V_T^{\rm ini} = V_D = 35$ V or $V_{\rm Stress} = V_G - V_T^{\rm ini} = 35$ V.

that of the conventional glass substrate. After calculating $R_{\rm sub}$, $R_{\rm total}$ can be obtained according to [7]. Then, $\Delta T_{\rm SHE}$ can be estimated. As shown by (3), $\Delta T_{\rm SHE}$ is proportional to the drain current. When constant bias is applied during stress, drain current decreases as a function of time due to the threshold voltage shift. As a result, (3) can be modified as follows to include the bias-stress effect in the self-heating effect:

$$\Delta T_{\rm SHE} = \left(\frac{V_{\rm GS} - V_T}{V_{\rm GS} - V_T^{\rm ini}}\right)^2 (I_D V_{\rm DS} R_{\rm total}) \qquad (5)$$

where $\Delta T_{\rm SHE}$ becomes a function of stress time due to the bias stress effect. With increasing stress time, the threshold voltage increases, and $\Delta T_{\rm SHE}$ decreases. The device temperature due to self-heating effect $(T_{\rm SHE})$ can then be represented by adding the calculated $\Delta T_{\rm SHE}$ to the original environmental temperature (e.g., 25 °C). In this study, $T_{\rm SHE}$ for devices with a channel width of 80 μm and a stress time of 1500 s is plotted in Fig. 5(b) using triangular symbols. Obviously, $T_{\rm SHE}$ increases with stress bias. The reason to explain the higher value of $T_{\rm SHE}$ when compared with $T_{\rm ch}$ may be because the model above neglects the heat dissipation by heat convection and radiation [10], [13]. As a result, the model overestimates the self-heating effect. The calculated $T_{\rm SHE}$ verifies the existence of a significant self-heating effect. It is noted, though, that $T_{\rm SHE}$ does not have the channel width effect since $R_{\rm sub}$ does not consider the heat dissipation at channel edge.

Finally, ΔV_T's for a wide-channel device on flat and bent substrates are studied. When stress bias is small, ΔV_T's for a wide-channel device on flat and bent substrates are compared in Fig. 6(a). Obviously, ΔV_T is unchanged for a bent substrate with a curvature radius of 15 or 7.5 mm. When stress bias is large and self-heating effect appears, ΔV_T's for a wide-channel device on flat and bent substrates are compared in Fig. 6(b). Interestingly, ΔV_T increases significantly on a bent substrate. It is known that outward bending causes tensile stress in the a-Si:H film [14]. When film temperature increases due to self-heating effect, tensile stress accompanied with elevated temperature may further accelerate the generation of defects and enlarge ΔV_T.

IV. Conclusion

In this study, a-Si:H TFTs have been successfully fabricated on colorless PI substrates at a low process temperature of 160 °C. Device reliability after bias-temperature stress are investigated. Unchanged gate leakage current of 10^{-13} A indicates that the SiN_x layer fabricated at 160 °C is stable. Using gate bias stress and two-terminal bias stress at different temperatures on devices with various channel widths, threshold voltage shift (ΔV_T) due to charged-state creation is well defined. Moreover, self-heating-enhanced ΔV_T is observed and investigated first. Increasing the channel width, drain bias, or substrate temperature enhances the self-heating effect. The increased temperature facilitates the generation of defect states and, therefore, enhances ΔV_T. The influence of substrate curvature on the self-heating enhanced ΔV_T is also demonstrated.

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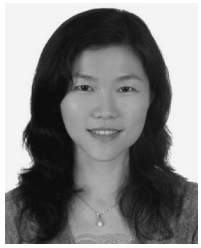
Shih-Chin Kao received the B.S. degree in 2003 from the National Tsing Hua University, Hsinchu, Taiwan, and the M.S. degree in 2005 from the National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree with the Department of Photonics and the Institute of Electro-Optical Engineering.

His main research interests include Si-based TFTs and organic polymer thin-film devices.

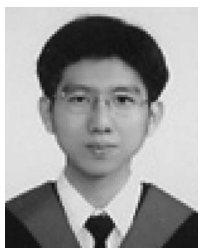


Hsiao-Wen Zan received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1997 and the M.S. and Ph.D. degrees from the National Chiao Tung University, Hsinchu, Taiwan, in 1999 and 2003, respectively.

She then joined the Department of Photonics, National Chiao Tung University, as an Assistant Professor and became an Associate Professor in 2008. She is also with the Institute of Electro-Optical Engineering, National Chiao Tung University. Her research interests include Si-based and amorphous metal oxide TFTs and circuits, organic/polymer thin-film devices, biochemical sensors, and thin-film solar cells.

Jung-Jie Huang received the Ph.D. degree in electrical engineering from the National Sun Yat-sen University, Kaohsiung, Taiwan, in 2005.

In 2006, he joined the Display Technology Center, Industrial Technology Research Institute, Hsinchu, Taiwan, as a Researcher. His current research interests include AMOLED display, flexible silicon-based thin-film transistors, and silicon thin-film solar cells.



Bo-Cheng Kung received the B.S. degree in electrical engineering from the National Sun Yat-sen University, Kaohsiung, Taiwan, in 2004 and the M.S. degree from National Cheng Kung University, Tainan, Taiwan, in 2006.

He then joined the Industrial Technology Research Institute as an Associate Engineer, where he is currently with the Display Technology Center. His current research interests include Si-based TFTs and laser crystallization technology.