Hybrid Buck–Boost Feedforward and Reduced Average Inductor Current Techniques in Fast Line Transient and High-Efficiency Buck–Boost Converter

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***Abstract*—This paper presents a buck–boost converter with high efficiency and small output ripple to extend the battery life of portable devices. Besides, the hybrid buck–boost feedforward (HBBFF) technique is integrated in this converter to achieve fast line response. The new control topology minimizes the switching and conduction losses at the same time even when four switches are used. Therefore, over a wide input voltage range, the proposed buck–boost converter with minimum switching loss like the buck or boost converter can reduce the conduction loss through the use of the reduced average inductor current (RAIC) technique. Moreover, the HBBFF technique minimizes the voltage variation at the output of error amplifier. Consequently, a fast line transient response can be achieved with small dropout voltage at the output. Especially, the converter can offer good line and load regulations to ensure a regulated output voltage without being affected by the decreasing battery voltage. Experimental results show that the output voltage is regulated over a wide battery lifetime, and the output ripple is minimized during mode transition. The peak efficiency is 97% and the transient dropout voltage can be improved substantially.**

***Index Terms*—Fast line transient response, feedforward technique, high efficiency, noninverting buck–boost converter, smooth transition.**

I. Introduction

With increasing low-voltage portable devices and growing requirements of functionalities embedded into these devices, efficient power management techniques are required to extend battery life [1]–[3]. In order to effectively use the remaining capacity of the battery, the design of dc–dc converters needs to supply the portable devices a regulated voltage over a wide battery voltage [4], [5]. The limitations of standard analog pulsewidth modulator (PWM) causes uncontrolled pulse skipping and significantly increased output voltage ripples when the converter operates in the transition region of the buck and boost modes [6]. That is, a buffer region, which is buck–boost mode, is required to provide a smooth and stable transition between two modes [7], [8]. As shown in Fig. 1, the converter can operate in buck, buck–boost, and boost modes when the battery voltage decreases. Since the dc–dc converter has different operation modes, the system stability, the output ripple, and the accuracy of the regulated output voltage during mode transition need to be guaranteed.

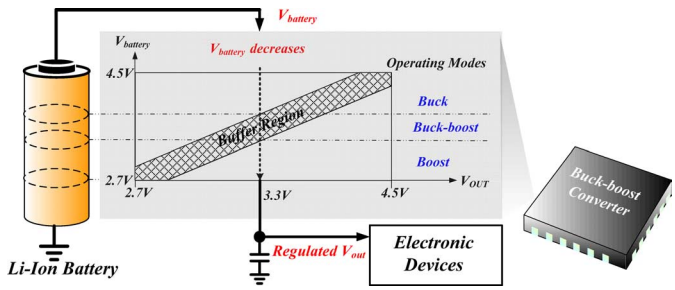

Fig. 1. Regulated output voltage versus the decreasing battery voltage.

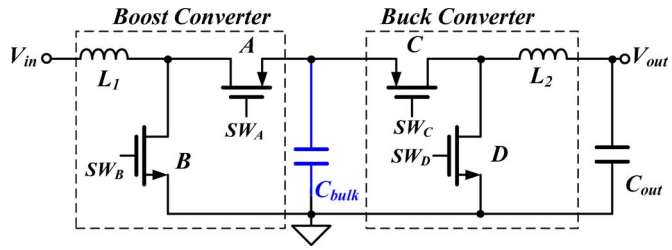

Fig. 2. Buck–boost converter implemented by discrete components contains two dc–dc converters.

As shown in Fig. 2, the buck–boost converter implemented by discrete components contains two dc–dc converters. Consequently, there is twice the power loss associated with the topology that contains only one converter. Besides, the number of external components is large and the complexity of two PWM control loops is hard to design. Certainly, the middle bulk capacitor that needs to absorb the pulsating current from both buck and boost stages has large value and volume. According to the design requirment, this topology causes the design of buck–boost converter hard to be implemented by the integrated chip. In order to overcome the drawbacks, the topology of H-bridge shown in Fig. 3(a) is widely used in the design of buck–boost converter [9]–[14]. The energy delivering path and the inductor current waveform of conventional buck–boost converter is depicted in Fig. 3(b). During phase I, switches *A* and *C* turns on to store energy in the inductor. During phase II, switches *B* and *D* turns on to deliver the energy to the output. According to voltage-second method [15], the average inductor current is

Manuscript received May 5, 2009; revised July 15, 2009. Current version published April 2, 2010. This work was supported by the National Science Council, Taiwan, under Grant NSC 97-2221-E-009-172. Recommended for publication by Associate Editor D. Maksimovic.

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Digital Object Identifier 10.1109/TPEL.2009.2031803

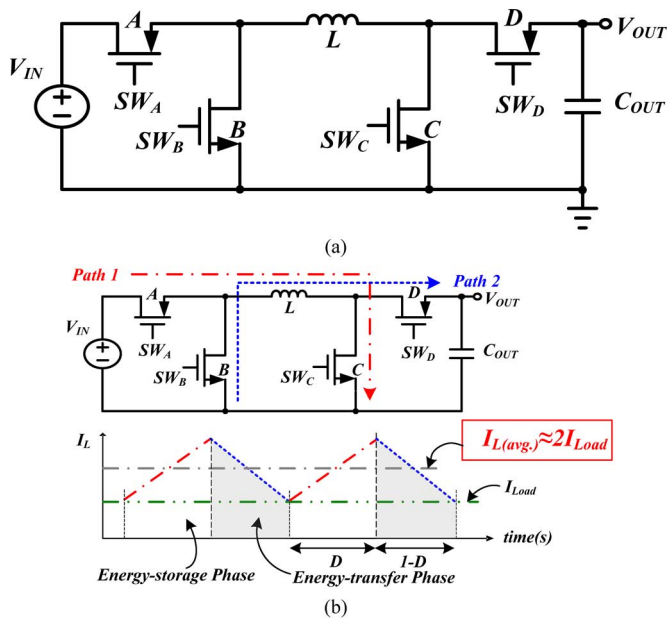


Fig. 3. (a) Topology of H-bridge for the buck–boost converter and (b) energy-delivering path and inductor current waveform of the conventional design.

expressed as (1).

$$I_{L(\mathrm{avg})}(1-D) = I_{\mathrm{Load}} \Rightarrow I_{L(\mathrm{avg})} = \frac{I_{\mathrm{Load}}}{1-D}. \qquad (1)$$

Either a buck or a boost converter, only two switches are turned on and off per cycle. The switching loss [16], [17] of a classic four-switch converter is double compared to the basic buck or boost converter. Especially, it causes an efficiency drop when the battery voltage approaches to the output voltage [18]. The inductor current becomes $2I_{\mathrm{Load}}$ when $V_{\mathrm{IN}} = V_{\mathrm{OUT}}$ and $D = 50\%$. The conduction loss becomes four times that of a buck or a low-duty boost converter. The control topology of the conventional buck–boost converter [19], [20] has the following disadvantages: The major drawback is the four switches are turned on/off during one switching cycle. As a result, much switching loss causes the power conversion efficiency is deteriorated. Furthermore, the efficiency is further reduced when the value of the input voltage is close to that of the output voltage since the average inductor current is twice the load current. That is, the conduction loss is four times that of a pure buck or a low-duty boost converter. The design of buck–boost converter not only needs to simultaneously reduce the conduction and switching losses but also needs to reduce the output ripple during the mode transition. The proposed buck–boost control scheme can effectively reduce the conduction loss through the use of the reduced average inductor current (RAIC) technique for improving efficiency. Besides, it also provides a proximate-linear buffer region with smooth and stable transition between the buck and boost modes in order to achieve low-output voltage ripple.

Furthermore, the feedforward compensation can effectively and rapidly reduce line disturbance on the converter's output to improve line transient response for the design of the voltage-mode switching converters [21]–[24]. The implementation of the feedforward technique simply varies the peak and valley voltages of the sawtooth signal with the input voltage in buck and boost converters, respectively. In other words, one of the peak and valley voltages needs to be changed according to the variation of the input voltage for the basic buck or boost converter. However, the sawtooth signal in the voltage-mode buck–boost converter needs to have the ability to simultaneously vary the peak and valley voltages with the input voltage according to the operation mode, as shown in Fig. 1. It means that line transient response time can be reduced whether the battery voltage is higher than the output supply voltage or not. This paper presents the hybrid buck–boost feedforward (HBBFF) technique integrated in the buck–boost converter to regulate the output voltage with fast line transient response. Good line regulation is guaranteed to get little output voltage variation in case of the input voltage variation. That is, the HBBFF technique can improve the static and dynamic performance of the buck–boost converter without being affected by the large variation of the battery voltage.

The organization of this paper is Section II describes the proposed buck–boost converter with the RAIC technique. Section III describes the circuit implementation composed of the HBBFF technique and the mode detector to demonstrate the performance of the buck–boost converter. The chip was fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 μm process, and the experimental results are shown in Section IV to verify the theory of proposed control scheme. Finally, a conclusion is made in Section V.

II. Topology of the Buck–Boost Converter With the RAIC Technique

The proposed RAIC technique in the buck–boost converter has four operations modes, denoted by mode I–mode IV. When V_{IN} is much higher than V_{OUT}, the converter operates in the basic buck mode, denoted by mode I. Switch *D* and switch *C* always turn on and off, respectively. Similarly, mode IV defines the basic boost mode when V_{IN} is much smaller than V_{OUT}. Switch *A* and switch *B* always turn on and off, respectively. The efficiencies in two modes are approximately equal to the fundamental buck and boost converters, respectively. When V_{IN} approaches to V_{OUT} and the converter needs to switch the buck operation to boost operation, the standard analog PWM control causes the uncontrolled pulse skipping and the increased output voltage ripple. The dash line of the output voltage with large ripple illustrates the limitation of the conventional control, as shown in Fig. 4. It is obvious that the uncontrolled pulse skipping increases the undesired large output voltage ripple. A buffer stage needs to insert between the buck and the boost modes in order to reduce the output ripple. Unfortunately, the new insertion of operation mode reduces the time of the basic buck and boost operations in a battery lifetime [25], [26]. Besides, the buffer stage causes the increasing inductor current level and thus the conduction loss is further increased. As a result, the switching loss is also increased because the four switches need to turn on/off during one switching cycle. That is, the longer buffer

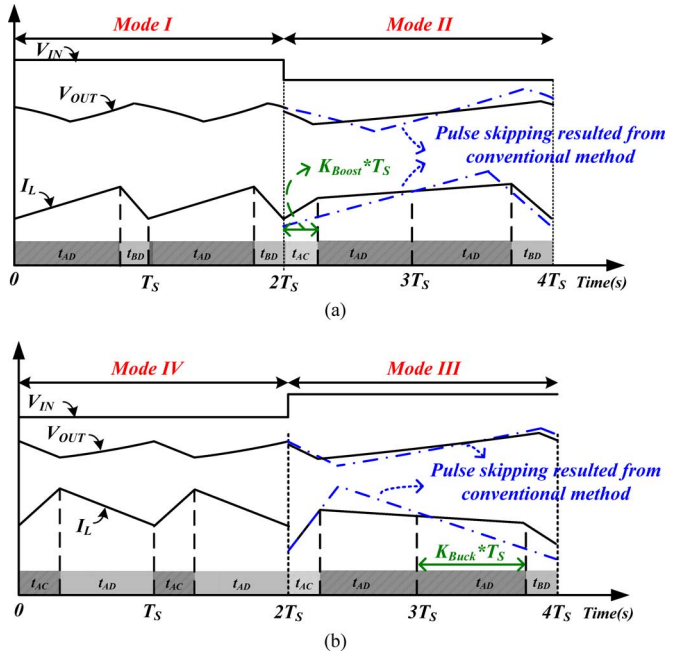


Fig. 4. Output voltage, the inductor current waveform, and the energy-delivering path when the buck–boost converter operates in (a) mode I and mode II and (b) mode III and mode IV.

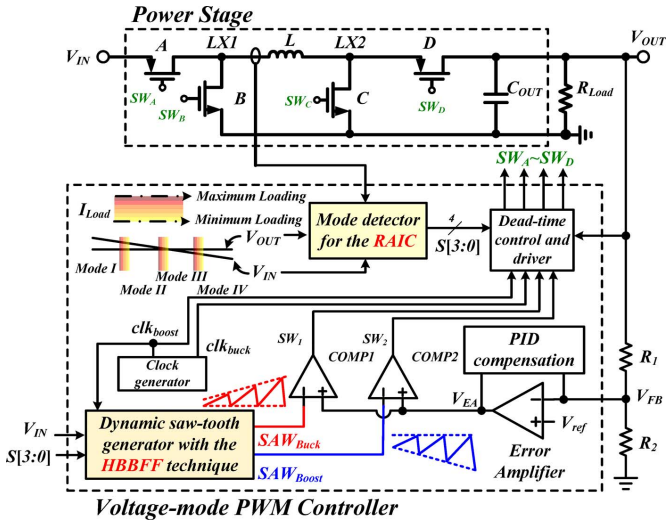


Fig. 5. Proposed buck–boost converter with the RAIC and HBBFF techniques.

stage may cause the power conversion efficiency more deteriorated. Although a regulated and small-ripple output voltage can be achieved by the insertion of the buffer stage. However, the cost is the deteriorated efficiency. The RAIC technique is proposed to reduce the inductor current level and the switching possibility of the four switches for improving the efficiency.

Mode II and mode III constitute a proximate-linear buffer region in order to smoothly transit the operation from buck mode (mode I) to boost mode (mode IV). As conceptually illustrated in Fig. 4, the inductor waveform of the RAIC technique has lower average value without the undesired pulse skipping and large output voltage ripple. Besides, the power conversion efficiency can be improved in the proximate-linear buffer region since the RAIC technique reduces the switching possibility of the four switches during one switching period. The proximate-linear buffer region is described as follows.

When $V_{\rm IN}$ is equal or slightly greater than $V_{\rm OUT}$, the operation needs more buck operation. The mode II uses a fixed boost duty $K_{\rm Boost}$ during the period of T_{S1}. During the period of T_{S2}, the converter is operated in buck mode regulated by the duty cycle of $D_{\rm Buck}$. The value of $K_{\rm Boost}$ should be selected equal to or larger than 10% to avoid the nonlinear operation of the PWM generation. The inductor current waveform and the output voltage are shown in Fig. 4(a) when the buck–boost converter operates in modes I and II. On the other hand, when $V_{\rm IN}$ is slightly smaller than $V_{\rm OUT}$, the buck–boost converter operates in mode III, which needs more boost operation owing to the lower input voltage. During the period of T_{S1}, the buck–boost converter operates in boost mode regulated by the duty cycle of $D_{\rm Boost}$. During the period of T_{S2}, the buck–boost converter operates in buck mode with a fixed duty cycle of $K_{\rm Buck}$. Similarly, the value of $K_{\rm Buck}$ should be selected equal to or smaller than 90% to avoid the nonlinear operation of the PWM generation. Fig. 4(b) shows the inductor current waveform and the output voltage when the buck–boost converter operates in mode III and mode IV. Obviously, the pulse skipping in the conventional method can be eliminated. A regulated and low-ripple output voltage can be guaranteed.

The RAIC technique uses two switching cycles composed of one buck and one boost cycles to constitute one regulation cycle when the supply voltage approaches to the output voltage. The switching loss can be reduced since only two switches are turned on/off in one switching cycle. Furthermore, the period of t_{AC} that only delivers energy to the inductor is minimized and thus the average inductor current level, as shown in (2), can be close to the load current. In other words, the RAIC technique can reduce the conduction loss since the difference between the average inductor current and the output load current is reduced

$$I_{\rm Load} = I_{L,\rm avg}\frac{(t_{AD}+t_{BD})}{(t_{AD}+t_{BD}+t_{AC})} \qquad \because\ t_{AC} \ll t_{AD}+t_{BD}$$
$$\therefore\ I_{L,\rm avg} \cong I_{\rm Load}. \quad (2)$$

III. Implementation of the Proposed Buck–Boost Converter

Fig. 5 illustrates the schematic of the proposed buck–boost converter. The converter is composed of a power stage, a feedback network, and a PWM control stage. A power stage contains an H-Bridge structure with power switches *A*–*D*, an inductor *L*, and a filtering capacitor $C_{\rm OUT}$. $V_{\rm OUT}$ is scaled down to V_{FB} by the voltage divider, composed of resistors R_1 and R_2. A voltage-mode PWM controller is utilized to turn on/off switches *A*–*D*. The mode detector decides the suitable operation mode according to not only the input voltage and output voltage but also load current. Besides, the dynamic sawtooth generator for implementing HBBFF technique improves line response. The comparators COMP1 and COMP2 compare the output signal V_{EA}

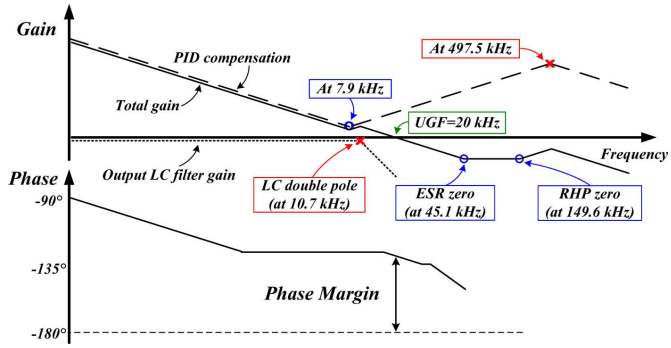


Fig. 6. Frequency response of the buck–boost converter with PID compensation to extend the system bandwidth.

from the error amplifier with the sawtooth signals $\mathrm{SAW_{Buck}}$ and $\mathrm{SAW_{Boost}}$ to decide buck duty D_{Buck} and boost duty D_{Boost}, respectively. The output filter exhibits a double pole response, and a troublesome feature in boost mode (mode IV) is the right-half plane (RHP) zero. The RHP zero limits the unity gain frequency of the closed-loop performance of the buck–boost converter. In order to achieve a higher bandwidth, the PID compensation is used. PID compensation provides two zeros to cancel out the output filter double poles and thus avoid sharply decreasing phase margin. In addition, PID compensation contributes one dominant pole and two high-frequency poles, which are used to suppress high-frequency noise. The converter is compensated for the worst-case where the boost duty cycle is at its peak value. The frequency response of the buck–boost converter with the PID compensation is depicted in Fig. 6.

A. Method and Analysis of the HBBFF Technique

According to the principle of inductor volt-second balance, the relationship between V_{IN} and V_{OUT} in different operation modes is shown in (3)–(6)

$$\text{Mode I: } \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = D_{\mathrm{Buck}} = \frac{V_{EA} - V_{L\_\mathrm{Buck}}}{V_{H\_\mathrm{Buck}} - V_{L\_\mathrm{Buck}}} \tag{3}$$

$$\text{Mode II: } \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{1 + D_{\mathrm{Buck}}}{1 + (1 - K_{\mathrm{Boost}})} = \frac{1 + [(V_{EA} - V_{L\_\mathrm{Buck}})/(V_{H\_\mathrm{Buck}} - V_{L\_\mathrm{Buck}})]}{2 - K_{\mathrm{Boost}}} \tag{4}$$

$$\text{Mode III: } \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{1 + K_{\mathrm{Buck}}}{1 + (1 - D_{\mathrm{Boost}})} = \frac{1 + K_{\mathrm{Buck}}}{1 + [(V_{H\_\mathrm{Boost}} - V_{EA})/(V_{H\_\mathrm{Boost}} - V_{L\_\mathrm{Boost}})]} \tag{5}$$

$$\text{Mode IV: } \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{1}{1 - D_{\mathrm{Boost}}} = \frac{V_{H\_\mathrm{Boost}} - V_{L\_\mathrm{Boost}}}{V_{H\_\mathrm{Boost}} - V_{EA}}. \tag{6}$$

V_{H_Buck} and V_{H_Boost} are the peak voltages of the buck sawtooth $\mathrm{SAW_{Buck}}$ and the boost sawtooth $\mathrm{SAW_{Boost}}$, respectively. Similarly, V_{L_Buck} and V_{L_Boost} are the valley voltages of the buck sawtooth $\mathrm{SAW_{Buck}}$ and the boost sawtooth $\mathrm{SAW_{Boost}}$,

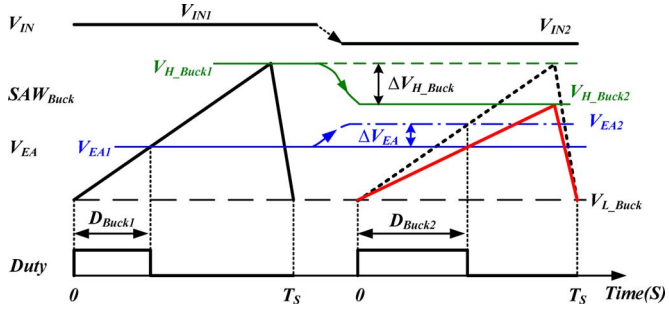


Fig. 7. Conventional PWM waveform and proposed dynamic PWM waveform for buck.

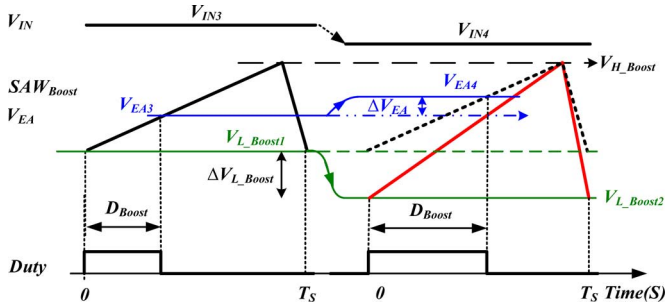


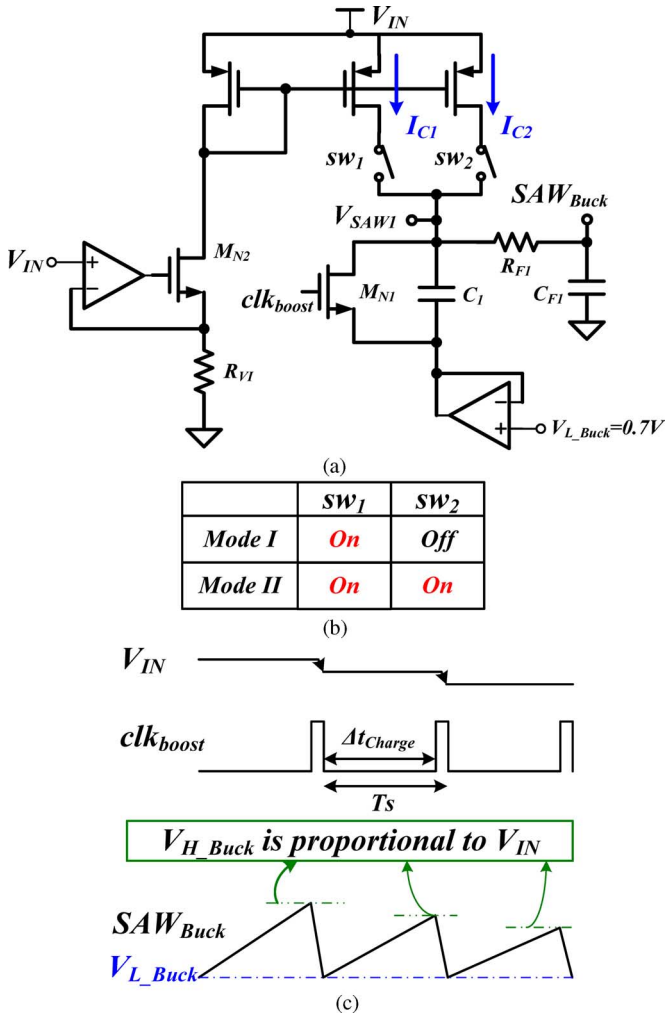
Fig. 8. Conventional PWM waveform and proposed dynamic PWM waveform for boost.

respectively. For the voltage-mode operation, the input voltage change must have an effect on the output voltage to determine the desired duty cycle. As a result, the output voltage needs much time to be regulated to a stable value, which is different to the previous steady-state value. As the dash line shown in Figs. 7 and 8, the transient response is slowed down by the voltage ΔV_{EA} on the large compensation capacitor at the output node of the error amplifier. Thus, a feedforward path is needed to rapidly react to the input voltage change without affecting the regulated output voltage. In (3) and (4), the value of V_{EA} is assumed to be constant. Keeping V_{L_Buck} constant and changing V_{H_Buck} with a value proportional to the input voltage can simplify the implementation of feedforward technique. The solid line in Fig. 7 illustrates the waveform of the sawtooth $\mathrm{SAW_{Buck}}$ in modes I and II. The peak voltage of the buck sawtooth is decreased from V_{H_Buck1} to V_{H_Buck2} and thus the duty cycle, D_{Buck}, is instantly increased to maintain a regulated output voltage.

Similarly, in (5) and (6), the valley voltage V_{L_Boost} needs to be proportional to the input voltage with a constant V_{H_Boost} when the converter operates in modes III and IV. As the solid line depicted in Fig. 8, V_{L_Boost} is decreased from V_{L_Boost1} to V_{L_Boost2} and thus the duty cycle, D_{Boost}, is instantly increased to maintain a regulated output voltage. In conclusion, the feedforward technique can have much small dip voltage and fast response. Therefore, the line transient response is improved substantially.

B. Implementation of Dynamic Buck Sawtooth Generator

The sawtooth generator of the buck mode is shown in Fig. 9(a). The value of V_{L_Buck} is set equal to 0.7 through

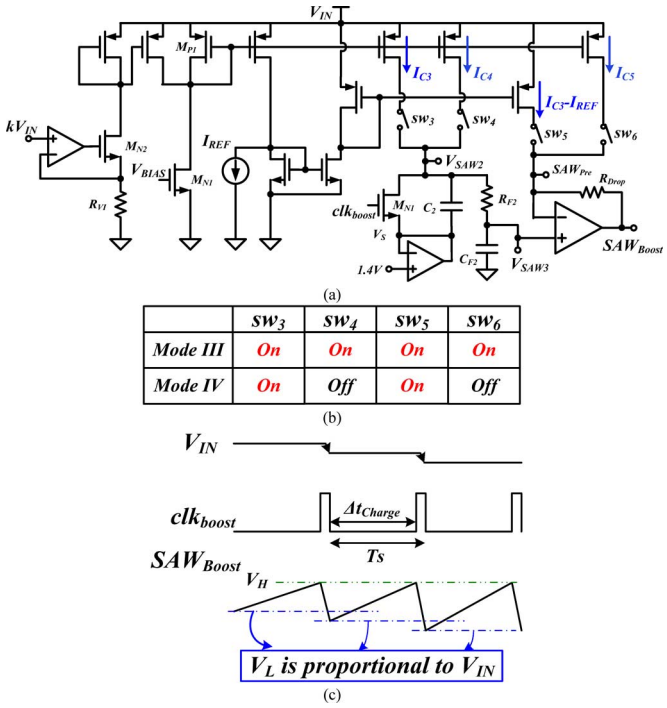


	sw_1	sw_2
Mode I	On	Off
Mode II	On	On

Fig. 9. (a) Proposed dynamic buck sawtooth generator. (b) States of the two switches under different mode. (c) Waveform under different supply voltages.

the use of a unity gain buffer. The charging current I_{C1}, which is from a voltage to current (*V–I*) converter composed of the transistor M_{N2}, a resistor R_{V1}, and an operational amplifier, is proportional to $V_{\rm IN}$. The frequency of pulse signal $clk_{\rm Boost}$ is the same as the converter's switching frequency. The switch $\rm sw_1$ turns on while the switch $\rm sw_2$ turns off in mode I, while $\rm sw_1$ and $\rm sw_2$ are all turned on in mode II. The states of the switches are sorted, as shown in Fig. 9(b), when converter operates in mode I and mode II. The capacitor C_1 is charged by I_{C1} within the period of $\Delta t_{\rm Charge}$ and discharged by the transistor M_{N1} to the low threshold voltage of 0.7 V in mode I. As a result, $V_{L\_\rm Buck}$ is constant and $V_{H\_\rm Buck}$ is proportional to $V_{\rm IN}$. The waveform of the sawtooth $\rm SAW_{Buck}$ and the relationship between the supply voltage $V_{\rm IN}$ and $\rm SAW_{Buck}$ are shown in Fig. 9(c).

A low-pass filer composed of R_{F1} and C_{F1} is used to eliminate the converter's switching noise. The buck duty cycle will be suddenly decreased when the converter transits from mode I to mode II due to the insertion of the boost operation with fixed duty. In order to smooth the output voltage in mode transition, an extra charging current I_{C2}, proportional to $V_{\rm IN}$, is inserted to compensate the mode transition error. The duty cycle would



	sw_3	sw_4	sw_5	sw_6
Mode III	On	On	On	On
Mode IV	On	Off	On	Off

Fig. 10. (a) Proposed dynamic boost sawtooth generator. (b) States of the four switches in different modes. (c) Waveform under different supply voltage.

decrease immediately, because the slope of $\rm SAW_{Buck}$ changes from the value of I_{C1}/C_1 to the value of $(I_{C1}+I_{C2})/C_1$ in the charging period. Therefore, the output voltage is not influenced when the converter transits between modes I and II. The value of $V_{H\_\rm Buck}$ in modes I and II is expressed as (7) and (8), respectively.

$$V_{H\_\rm Buck} = V_{L\_\rm Buck} + \frac{I_{C1}\Delta t_{\rm Charge}}{C_1} \quad \text{where} \quad V_{L\_\rm Buck} = 0.7 \tag{7}$$

$$V_{H\_\rm Buck} = V_{L\_\rm Buck} + \frac{(I_{C1}+I_{C2})\Delta t_{\rm Charge}}{C_1} \quad \text{where} \quad V_{L\_\rm Buck} = 0.7. \tag{8}$$

C. Implementation of Dynamic Boost Sawtooth Generator

The boost sawtooth generator is shown in Fig. 10(a). A unity gain buffer is used to ensure the source voltage V_S is set to 1.4 V. A *V–I* converter is composed of the transistor M_{N2}, a resistor R_{V1}, and an operational amplifier. The current flowing through the transistor M_{N1} is designed larger than that flowing through the transistor M_{N2}. Therefore, the current flowing through the transistor M_{P1} is inversely proportional to the value of $V_{\rm IN}$. By this method, the charging currents I_{C3}–I_{C5} are also inversely proportional to $V_{\rm IN}$. The reference current $I_{\rm REF}$ can charge the voltage on the capacitor C_2 from 1.4 V to $V_{H\_\rm Boost}$ within the period of $\Delta t_{\rm Charge}$. Both switches $\rm sw_3$ and $\rm sw_5$ turn on while $\rm sw_4$ and $\rm sw_6$ turn off in mode IV. In mode III, four switches $\rm sw_3$–$\rm sw_6$ all turn on. The states of switches are sorted, as shown in Fig. 10(b), when converter operates in mode III and mode IV.

In mode IV, the voltage on the capacitor C_2 is charged by I_{C3} within $\Delta t_{\rm Charge}$ and discharged by transistor M_{N2} to 1.4 V. Similar to the buck sawtooth generator, the peak voltage of $V_{\rm SAW2}$ is inversely proportional to $V_{\rm IN}$ and the valley voltage of $V_{\rm SAW2}$ is fixed at 1.4. A low-pass filter composed of R_{F2} and C_{F2} is used to eliminate the glitch of $V_{\rm SAW2}$ and outputs a low noise signal $V_{\rm SAW3}$. Then, an operational amplifier with resistive negative feedback is used to ensure $V_{\rm SAW3} \approx {\rm SAW_{Pre}}$. The voltage across resistor $R_{\rm Drop}$ ($R_{\rm Drop} = \Delta t_{\rm Charge}/C_2$) is equal to the difference voltage between the peak voltage of ${\rm SAW_{Pre}}$ and $V_{H\_{\rm Boost}}$. Therefore, the peak and valley voltages of ${\rm SAW_{Boost}}$ in mode IV are expressed as (9) and (10), respectively.

$$\begin{aligned} V_{H\_{\rm Boost}} &= 1.4 + \frac{I_{C3}\Delta t_{\rm Charge}}{C_2} - (I_{C3} - I_{\rm REF})R_{\rm Drop} \\ &= 1.4 + \frac{I_{\rm REF}t_{\rm Charge}}{C_2} \end{aligned} \tag{9}$$

$$\begin{aligned} V_{H\_{\rm Boost}} &= 1.4 + \frac{I_{C3}\Delta t_{\rm Charge}}{C_2} - (I_{C3} - I_{\rm REF})R_{\rm Drop} \\ &= V_{L\_{\rm Boost}} + \frac{I_{C3}\Delta t_{\rm Charge}}{C_2} \\ &\Rightarrow V_{L\_{\rm Boost}} = 1.4 - (I_{C3} - I_{\rm REF})R_{\rm Drop}. \end{aligned} \tag{10}$$

According to (9) and (10), the value of $V_{H\_{\rm Boost}}$ is constant and the value of $V_{L\_{\rm Boost}}$ is equal to the value of $[1.4 - (I_{C3} - I_{\rm REF})R_{\rm Drop}]$. Therefore, $V_{L\_{\rm Boost}}$ is proportional to $V_{\rm IN}$. The waveform of the sawtooth ${\rm SAW_{Boost}}$ and the relationship between the supply voltage $V_{\rm IN}$ and ${\rm SAW_{Boost}}$ are shown in Fig. 10(c). The boost duty cycle increases when mode IV transits to mode III due to the insertion of the buck operation with fixed duty in mode III. Similarly, in order to have a smooth output voltage during mode transition, the currents I_{C4} and I_{C5} that have the same value are introduced to increase the amplitude of $V_{\rm SAW2}$ and keep the peak voltage of ${\rm SAW_{Boost}}$ invariant. That is $V_{H\_{\rm Boost}}$ and $V_{L\_{\rm Boost}}$ in mode III can be expressed as (11) and (12), respectively.

$$\begin{aligned} V_{H\_{\rm Boost}} &= 1.4 + \frac{(I_{C3} + I_{C4})\Delta t_{\rm Charge}}{C_2} \\ &\quad - (I_{C3} - I_{\rm REF} + I_{C5})R_{\rm Drop} \\ &= V_{L\_{\rm Boost}} + \frac{(I_{C3} + I_{C4})\Delta t_{\rm Charge}}{C_2} \\ &= 1.4 + \frac{I_{\rm REF}\Delta t_{\rm Charge}}{C_2} \end{aligned} \tag{11}$$

where

$$V_{L\_{\rm Boost}} = 1.4 - (I_{C3} - I_{\rm REF} + I_{C5})R_{\rm Drop}. \tag{12}$$

It shows that the peak voltage of the boost sawtooth is kept at $V_{H\_{\rm Boost}}$ even the operating mode transits from mode IV to mode III. According to (11) and (12), the slope of ${\rm SAW_{Boost}}$ adjusts from the value of I_{C3}/C_2 to the value of $(I_{C3} + I_{C4})/C_2$ immediately in the charging period in order to increase the boost duty cycle to smooth the output voltage during mode III–mode IV.

D. Mode Detector for Implementing the RAIC Technique

The design of the proposed buck–boost converter should consider the effect of the power MOSFET's on-resistance. The duty cycle is not only decided by $V_{\rm IN}$ and $V_{\rm OUT}$ but also by load current $I_{\rm Load}$ since $I_{\rm Load}$ flowing through the switches causes large voltage drop $V_{\rm SW}$. Owing to the consideration of the power MOSFET's on-resistance, the output ripples will not be enlarged during mode transition. Correct input/output characteristics of four modes are defined in (13)–(16).

$$\text{Mode I: } V_{\rm IN} - 2\frac{V_{\rm SW}}{D_{\rm Buck}} = \frac{V_{\rm OUT}}{D_{\rm Buck}} \tag{13}$$

$$\text{Mode II: } V_{\rm IN} - \frac{4}{1 + D_{\rm Buck}}V_{\rm SW} = \frac{2 - K_{\rm Boost}}{1 + D_{\rm Buck}}V_{\rm OUT} \tag{14}$$

$$\text{Mode III: } V_{\rm IN} - \frac{4}{1 + K_{\rm Buck}}V_{\rm SW} = \frac{2 - D_{\rm Boost}}{1 + K_{\rm Buck}}V_{\rm OUT} \tag{15}$$

$$\text{Mode IV: } V_{\rm IN} - 2V_{\rm SW} = (1 - D_{\rm Boost})\,V_{\rm OUT}. \tag{16}$$

The proposed mode detector as illustrated in Fig. 11 can provide a smooth and stable transition among the four modes. The mode detector is composed of three parts. The voltage drop sensing circuit is used to detect the value of $V_{\rm SW}$. The current of $V_{\rm SW}/R_1$ flows through the resistor R_2 to generate the decision signal $V_{\rm DEC}$ as expressed in (17).

$$V_{\rm DEC} = V_{\rm IN} - \left(1 + \frac{R_2}{R_1}\right)V_{\rm SW}. \tag{17}$$

In order to derive the boundary condition, assume $D_{\rm Buck} = K_{\rm Buck}$ and $D_{\rm Boost} = K_{\rm Boost}$. When mode I transits to mode II, the difference voltage, which is equal to $V_{\rm DEC} - V_{\rm OUT}$, needs to compare with $K_1 V_{\rm OUT}$, as shown in (18).

$$V_{\rm DEC} = V_{\rm IN} - 2\frac{V_{\rm SW}}{K_{\rm Buck}} = \frac{V_{\rm OUT}}{K_{\rm Buck}} = V_{\rm OUT} + K_1 V_{\rm OUT}$$
$$\text{where } K_1 = \frac{1 - K_{\rm Buck}}{K_{\rm Buck}}. \tag{18}$$

Similarly, the difference voltage needs to compare with $(-K_{\rm Boost}V-)$, as shown in (19), when mode III transits to mode IV.

$$V_{\rm DEC} = V_{\rm IN} - 2V_{\rm SW} = V_{\rm OUT} - K_{\rm Boost}V_{\rm OUT}. \tag{19}$$

Finally, $V_{\rm DEC}$ needs to compare with $V_{\rm OUT}$, as shown in (20), when mode II transits to mode III.

$$V_{\rm DEC} = V_{\rm IN} - \frac{4}{1 + K_{\rm Buck}}V_{\rm SW} = V_{\rm OUT}. \tag{20}$$

Evidently, the value of $V_{\rm DEC}$ in different mode needs to be finely adjusted according to the values of R_1 and R_2.

An absolute voltage $V_{\rm ABS}$ that is equal to $|V_{\rm DEC}–V_{\rm OUT}|$ is used to decide when mode I transits to mode II and mode III transits to IV. The dual modified-cascoded flipped voltage followers (M-CASFVF) *V–I* converter can generate the signal $V_{\rm ABS}$. The negative feedback loop in the input pair causes the output impedance low enough to limit the voltage variations at the drains of the transistors M_{N1} and M_{N2}. As a result, the undesired channel-length modulation can be minimized. The advantage of the M-CASFVF circuit is the gate voltages of the

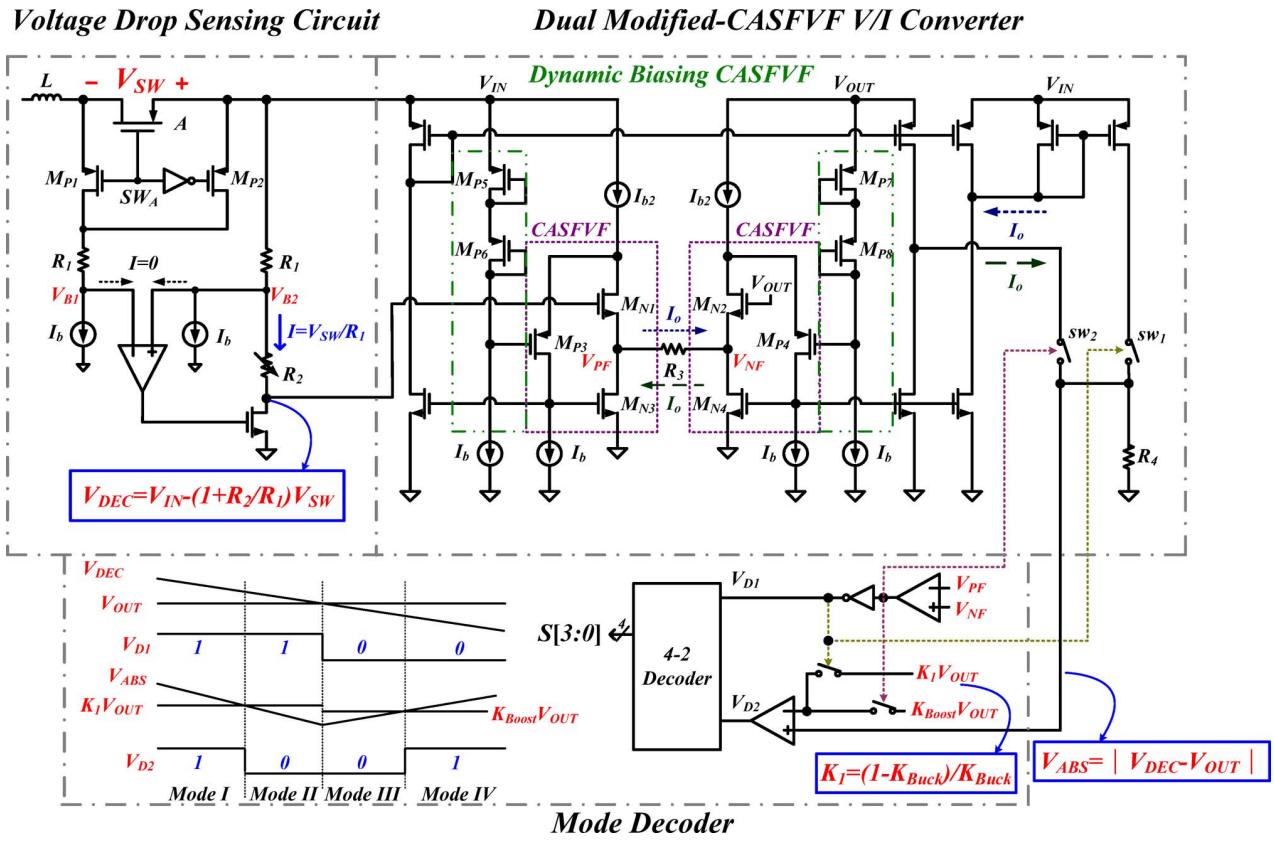


Fig. 11. Proposed mode detector for implementing the RAIC technique.

transistors M_{P3} and M_{P4} are dynamically biased. The input common mode range (ICMR) of the conventional CASFVF circuit with fixed biasing scheme is small and not suitable in the buck–boost converter that needs wide input supply voltage. On the contrary, the transistors M_{P5}, M_{P6}, M_{P7}, and M_{P8} are used to dynamically bias M_{P3} and M_{P4} in the M-CASFVF circuit. Thus, the advantage of the M-CASFVF circuit is the ICMR is much larger than that of the conventional design and is suitable for wide supply voltage range. The difference between $V_{\rm DEC}$ and $V_{\rm OUT}$ is equal to the difference between V_{PF} and V_{NF}. When V_{PF} is greater than V_{NF}, the switch $\rm sw_1$ turns on and the switch $\rm sw_2$ turns off. A current with the value of $(V_{PF}–V_{NF})/R_3$ will flow through the resistor R_4 according to the ratio of current mirror. If $R_3 = R_4$, $V_{\rm ABS} = V_{PF}–V_{NF} = V_{\rm DEC}–V_{\rm OUT}$. Similarly, a programmed current with the value of $(V_{NF}–V_{PF})/R_3$ flows through the resistor R_4 and thus the value of $V_{\rm ABS}$ is equal to the value of $(V_{\rm OUT}–V_{\rm DEC})$ when V_{PF} is smaller than V_{NF}.

The mode decoder can generate the digital signals S[0]–S[3] to indicate mode I to mode IV. It includes two comparators and a 4–2 decoder. The signal V_{D1} is the comparison result between V_{PF} and V_{NF} that are proportional to $V_{\rm DEC}$ and $V_{\rm OUT}$, respectively. Thus, the transient point of V_{D1} represents the boundary between mode II and mode III according to (20). The signal V_{D2} is the comparison result between $V_{\rm ABS}$ and $K_1V_{\rm OUT}$ in mode I and mode II. However, it is the comparison result between $V_{\rm ABS}$ and $K_{\rm Boost}V_{\rm OUT}$ in mode III and mode IV. The signals V_{D1} and V_{D2} pass through the 4–2 decoder and generate S[0], S[1], S[2], and S[3] that are representative of mode I to mode IV, respectively.

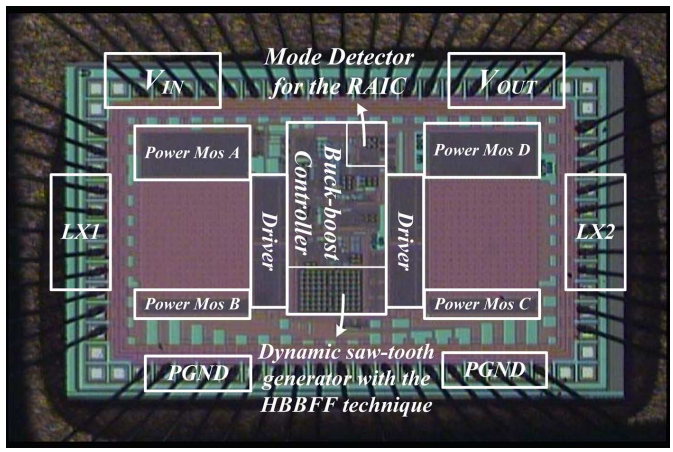


Fig. 12. Chip micrograph.

IV. Experimental Results

The buck–boost converter was fabricated by TSMC 0.25 μm 1P4M process. The filter components contain $L = 4.7$ μH, $C_{\rm OUT} = 47$ μF, and $R_{\rm ESR} = 75$ mΩ. The input voltage ranges from 2.7 to 4.5V, and the nominal output voltage is 3.3 V. The switching frequency is designed as 700 kHz. Fig. 12 shows the chip micrograph with die area of 3.14 mm^2.

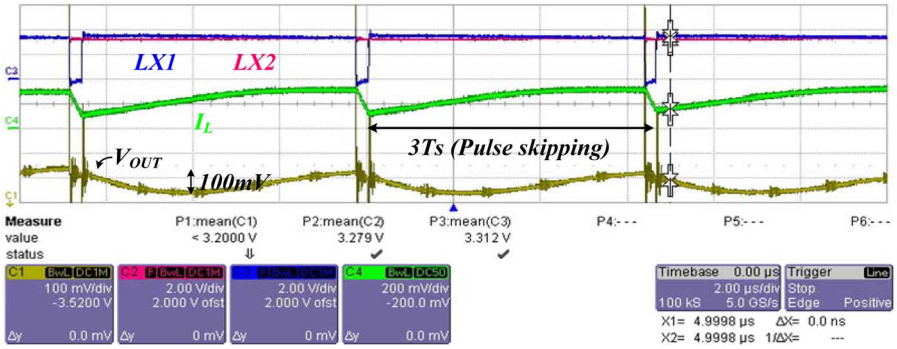


Fig. 13. Uncontrolled pulse skipping increases output ripple around buck–boost mode.

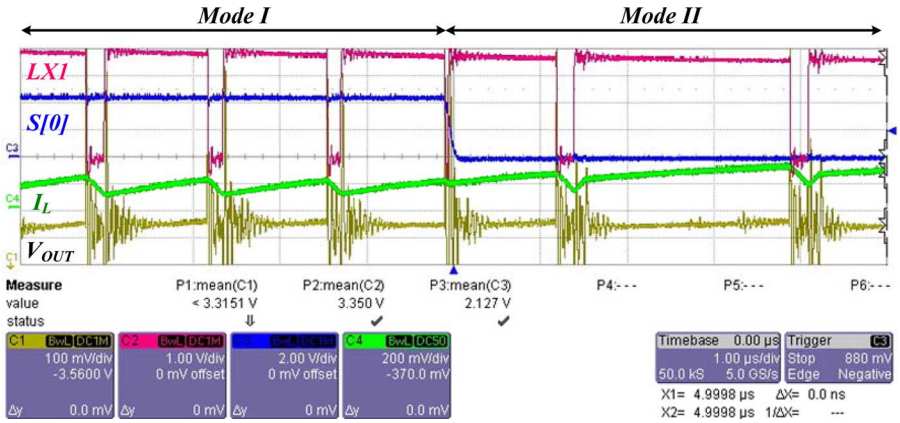


Fig. 14. Mode I transits to mode II when $V_{\rm IN}$ changes from 4.2 to 3.8 V, and $I_{\rm Load}$ is 225 mA.

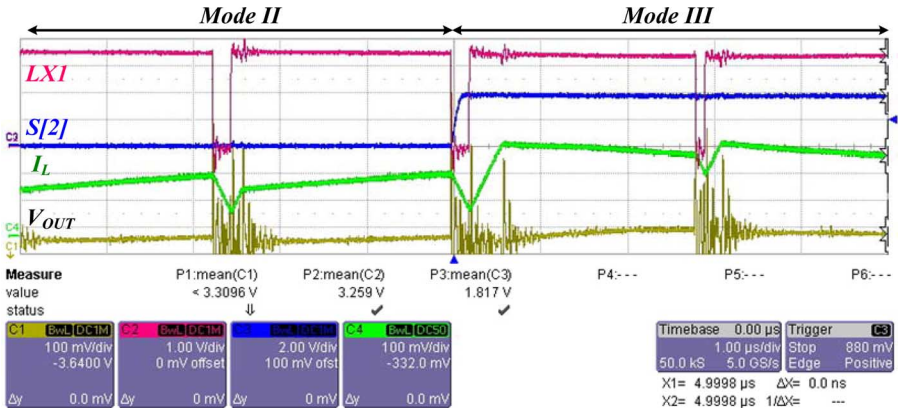


Fig. 15. Mode II transits to mode III when $V_{\rm IN}$ changes from 3.6 to 3.5 V, and $I_{\rm Load}$ is 225 mA.

Fig. 13 shows the increasing output ripple due to the uncontrolled pulse skipping when the operation mode is close to the transition from buck to boost mode without the buck–boost buffer mode. After the implementation of the buck–boost buffer mode, Figs. 14–16 show the stable operation when the input voltage decreases with $I_{\rm Load} = 225$ mA. Figs. 13 and 14 demonstrate that the output voltage ripple is reduced from 100 to within 10 mV in worst-case. The operation mode can smoothly switch from mode I to mode IV, and the inductor current is reduced to close to the value of load current. Thus, the conduction loss can be improved. Besides, the number of switches are used in one switching cycle is also reduced from four to two. As a result, the switching loss can be further reduced. Fig. 17 shows that the output voltage is regulated in steady state when the supply voltage is equal to the output voltage. The proposed control method effectively removes the undesired pulse skipping and thus avoids increasing the output voltage ripple.

Fig. 18 shows the line transient response with and without the HBBFF technique when load current is 225 mA. The input voltage $V_{\rm IN}$ steps from 3.9 to 3.6 V within 50 μs. At this time, the buck–boost converter is operated at the buck–boost mode with more buck operation. The dropout voltage of the

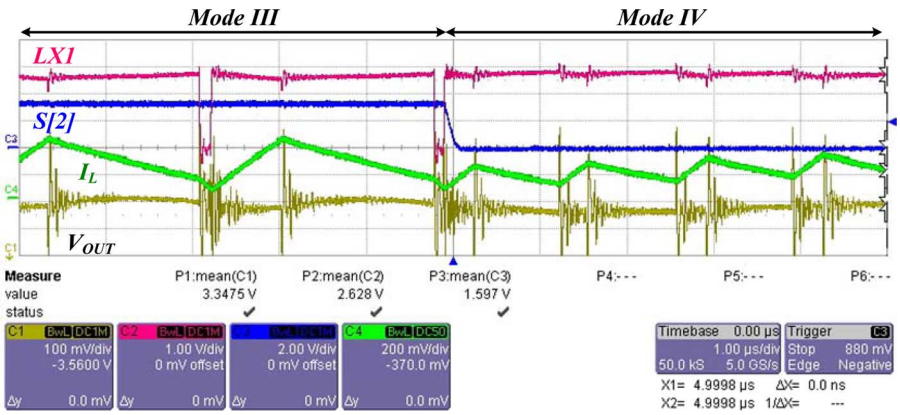


Fig. 16. Mode III transits mode IV when V_{IN} changes from 3.2 to 2.8 V, and I_{Load} is 225 mA.

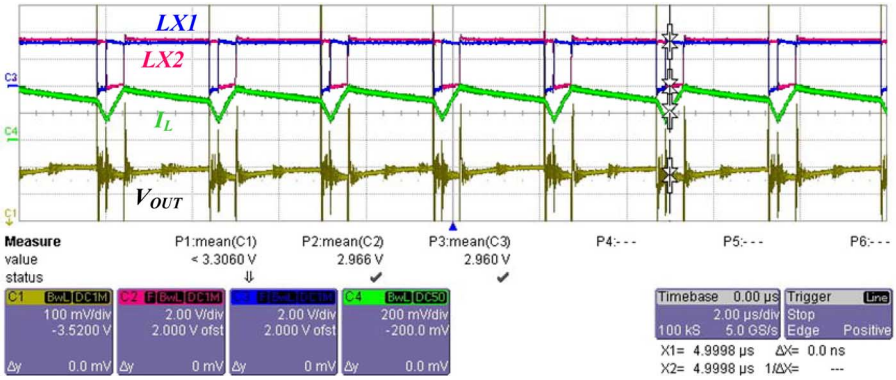
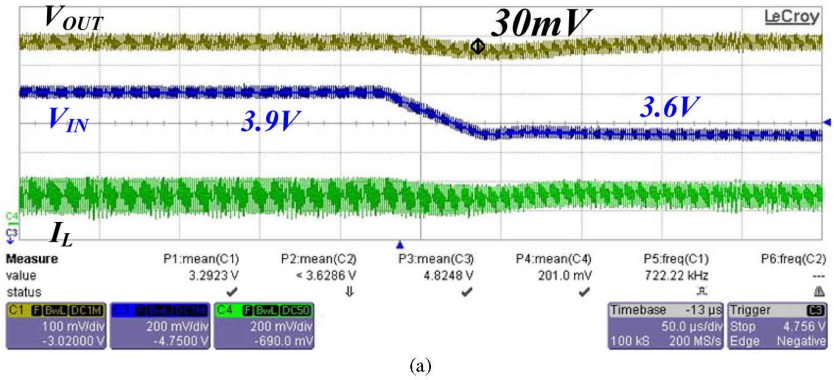
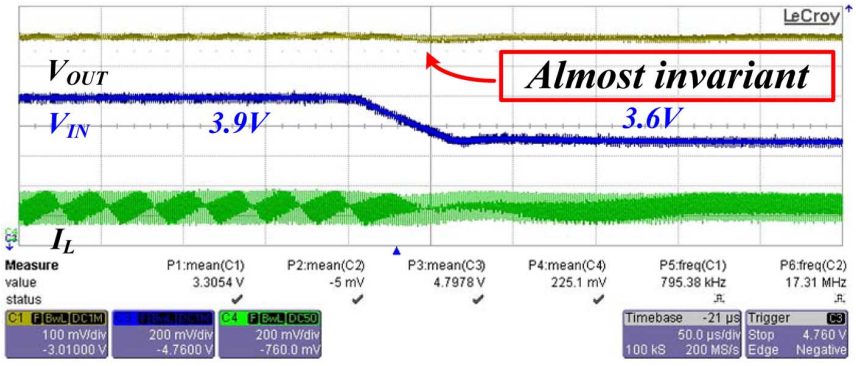


Fig. 17. Waveform under steady state when supply voltage is equal to output voltage with $I_{\mathrm{Load}} = 225$ mA.



(a)



(b)

Fig. 18. Output voltage waveform when the input voltage V_{IN} steps from 3.9 to 3.6 V within 50 μs. (a) Without the HBBFF technique. (b) With the HBBFF technique.

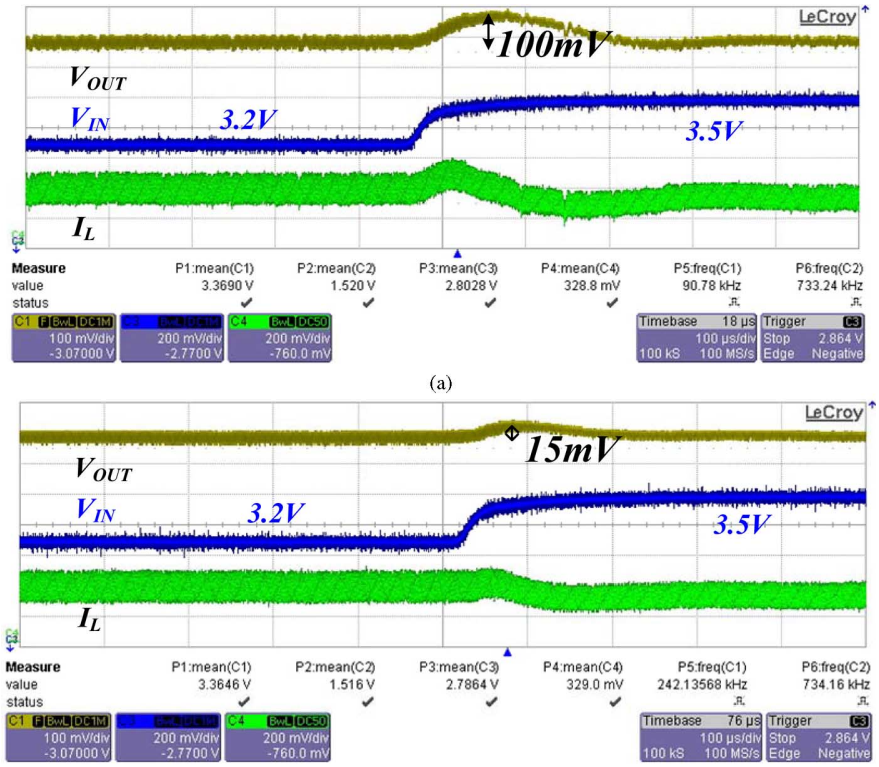


Fig. 19. Output voltage waveform when the input voltage V_{IN} steps from 3.2 to 3.5 V and load current is 225 mA. (a) Without the HBBFF technique. (b) With the HBBFF technique.

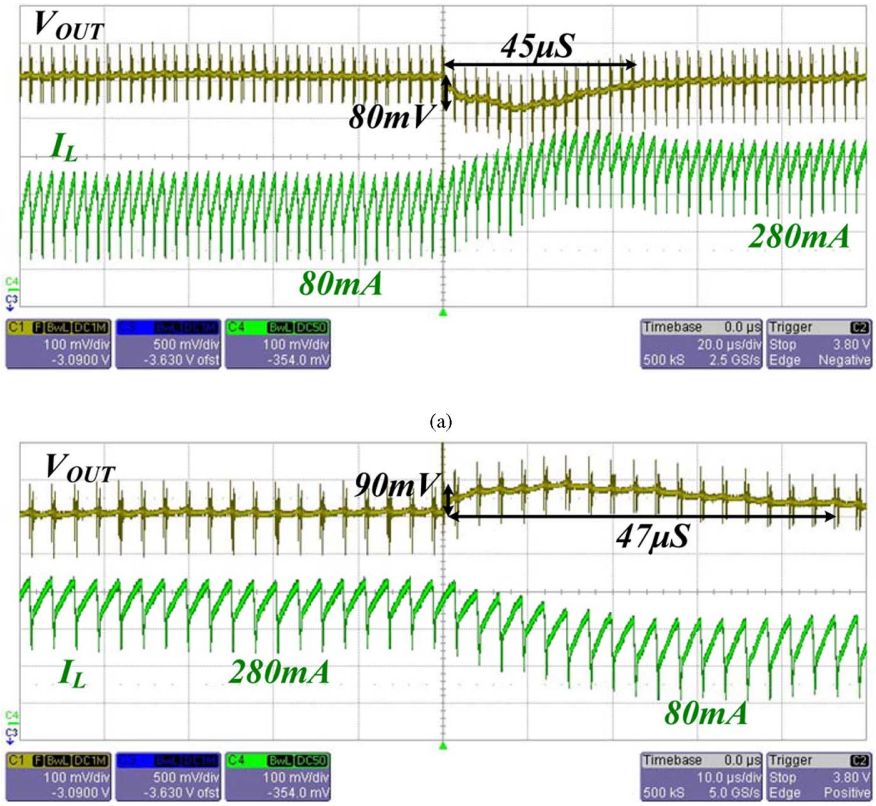


Fig. 20. Load transient response. (a) I_{Load} changes from 80 to 280 mA. (b) I_{Load} changes from 280 to 80 mA.

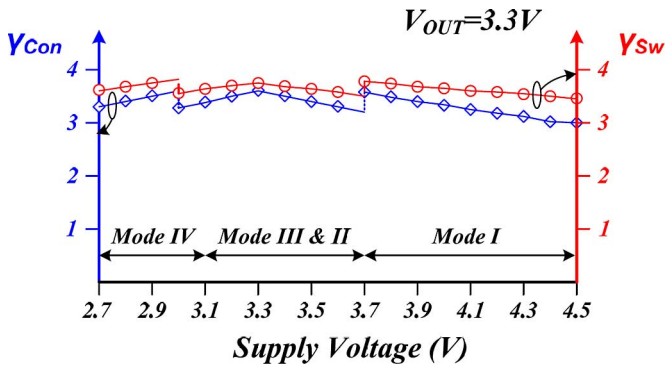


Fig. 21. Improvement of conduction and switching losses.

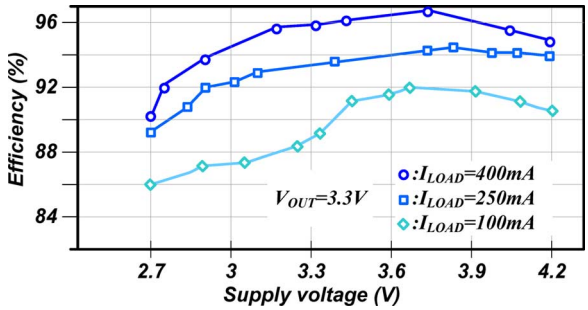


Fig. 22. Measured power efficiency of the proposed converter with different supply voltage and load current.

converter without the proposed control technique is 30 mV. On the contrary, the output voltage $V_{\rm OUT}$ can be maintained at its regulated voltage level owing to the fast response benefited from the HBBFF technique. It is obvious that when the input voltage drops, the converter without the HBBFF technique relies only on the voltage feedback loop. That is the reason that $V_{\rm OUT}$ has large variation during the line transient period.

In Fig. 19, when the input voltage steps from 3.2 to 3.5 V and load current is 225 mA, the buck–boost converter operates at the buck–boost mode with more boost operation. The overshoot voltage is decreased from 100 to 15 mV due to the HBBFF technique.

Fig. 20 shows the measured transient response of the output voltage and the inductor current of the proposed buck–boost converter with 200 mA load step (from 80 to 280 mA) at 3.7 V input. It demonstrates that the proposed converter not only has stable operation over wide input voltage range but also wide load current range. Fig. 21 shows the improvement of power loss. The blue line draws the conduction loss ratio defined as $\gamma_{\rm Con}$, which is equal to conventional buck–boost control to the proposed control. The red line draws the switching loss ratio defined as $\gamma_{\rm Sw}$, which is equal to conventional buck–boost control to the proposed control. Obviously, conduction and switching losses both are improved substantially by the proposed control method. Efficiency of the proposed buck–boost converter is measured and shown in Fig. 22. Maximum efficiency is 97%, operated at input supply voltage of 3.8 V and load current of 400 mA. It also shows that efficiency still maintains at relatively high value when the supply voltage is decreased to close to the output voltage. The summary of specifications is listed in Table I.

TABLE I
SUMMARY OF SPECIFICATIONS AND COMPARISON

Specifications	[25]	This paper
Input voltage	2.5~3.2	2.7~4.5 (Li-Ion battery)
Output voltage accuracy	0.5~3 %	0.1~1 %
Load current	50 mA~800 mA	50 mA~500 mA
Switching frequency	500 kHz	700 kHz
Inductor	2.2 μH	4.7 μH
Output capacitor	47 μF	47 μF
Efficiency	10~62 %	96%@V_{IN}=3.8V and I_{Load}=400mA

V. CONCLUSION

A buck–boost converter with a new control scheme was introduced in this paper. Several advantages include reduced switching losses through the use of only half the number of switches during each cycle and decreased conduction losses of power switches due to the RAIC technique. The efficiency is effectively improved. A new mode detector can select proper operating mode to get a regulated output and thus enhanced control accuracy are guaranteed during mode transition. Besides, the HBBFF technique is integrated in this converter to minimize the voltage variation at the output of error amplifier. As a result, a fast line transient response can be achieved with small dropout voltage at the output. Experimental results show that the output voltage is regulated during the whole battery life, and the output transition is very smooth during the mode transition by the proposed control scheme. The peak efficiency is 97% and the transient dropout voltage can be improved substantially.

ACKNOWLEDGMENT

The authors would like to thank Chunghwa Picture Tubes, Ltd. for their help.

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