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Effective surface treatments for selective epitaxial SiGe growth in locally strained pMOSFETs

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Abstract
Several dry and wet surface treatment methods are explored for a selective SiGe epitaxial film used to fabricate embedded SiGe pMOSFETs. Pre-clean conditions for the device wafers used in this study were limited by a realistic CMOS process window with tight thermal and chemical budgets due to dopant diffusion and hardmask erosion concerns. The effectiveness of these pre-clean methods is evaluated by SiGe epitaxial film quality and SIMS profiles of key residual contaminants such as C and O at the SiGe–Si substrate interface. As an effective low-temperature dry surface treatment, chemical bake in HCl/H_2 at temperature below 800 °C is found to reduce interface C and O peak concentrations by an order of magnitude. Wet clean in multiple cycles of DIW-O_3 (ozonated water), SC1 and diluted HF (DHF) is also presented to prepare epitaxial growth surfaces with accumulated damage and chemical residues from previous process steps. SiGe epitaxial film morphology is also observed to improve by increasing DHF clean time. For further improvement of film quality on the most difficult surfaces, Si seed layer was employed to initiate SiGe film nucleation and yield smooth film growth.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Locally strained Si technology using embedded SiGe has demonstrated an improved pMOSFET device performance through hole mobility enhancement [1–3]. Widely used, embedded SiGe is achieved by selectively growing an epitaxial SiGe film in recessed Si source and drain in the pMOSFET area. Prior to the selective deposition step, device wafers go through the usual gate formation, spacer formation, multiple implants (e.g. LDD, halo and HDD), anneal, etc. Typical process steps and the impact of the process sequence for a recessed source and drain SiGe application are described elsewhere [2]. In this study, wafers were processed through a CMOS flow using an oxide film to protect nFET areas during selective SiGe epitaxial growth. Multiple implants' reactive ion etch used in the recessed source/drain formation, and PR strip prior to selective epi deposition result in physical damage and chemical residues on the film growth surface. Growth surfaces free of damage and chemical contaminants are required to obtain high-quality SiGe epi films. Non-ideal surface conditions lead to film nucleation difficulties and prevent smooth film growth in mild cases and film growth in severe cases. Surface chemical contaminants are typically removed by wet clean and high-temperature bake prior to epi deposition. For example, diluted HF (DHF) is used to remove native oxide and passivate the surface from

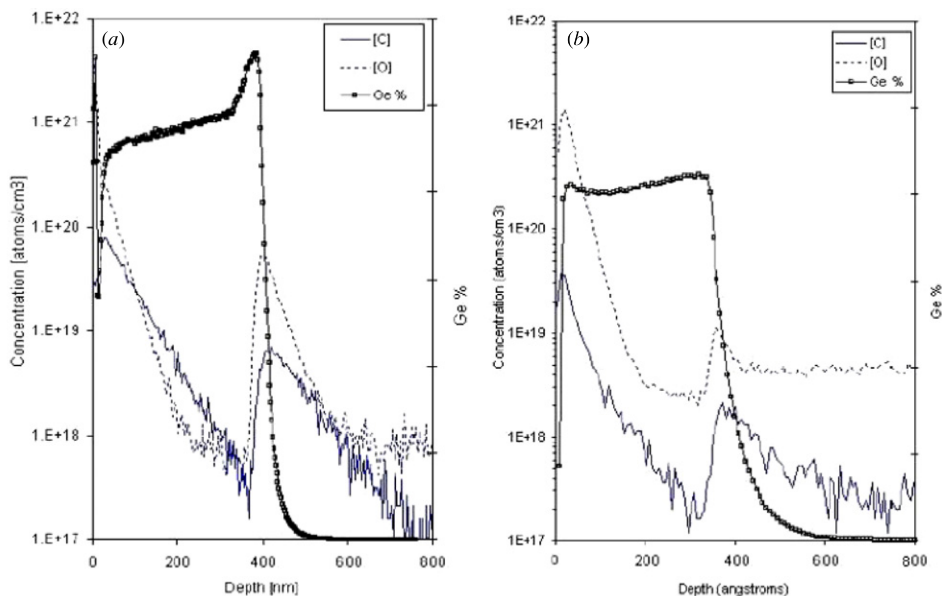


Figure 1. SIMS profiles of C, O and Ge in SiGe epitaxial films grown (*a*) after H_2 bake alone and (*b*) after HCl bake and H_2 bake.

further contamination. However, the DHF clean also removes protective layers (e.g. oxide hardmask) over pFET gates and nFET areas required for selective deposition, and the clean time is limited to the chemical budget of the wafer structure. Pre-epi high-temperature bake (>850 °C) is commonly used [4, 5] to effectively remove interface contaminants (C and O) between epi film layer and Si substrate; however, the bake temperature cannot exceed the thermal budget of the device wafer. Besides, Si migration is a concern for high-temperature bake. Such chemical and thermal budgets impose a small pre-clean window and challenges for both wet and dry cleaning of surfaces with accumulated damage and chemical residues. In this study, we present several cleaning approaches that improve interfacial quality and improve SiGe epi film morphology. One effective method is a cyclical wet clean through ozonated DI water (DIW-O_3), SC1 and DHF, and is discussed. The effect of pre-epi DHF clean time is also explored. A low-temperature chemical bake using HCl (g) in H_2 carrier gas is also presented as an effective method to reduce interfacial contaminants and improve epi film morphology. Use of a Si seed layer was also demonstrated as a way to ease nucleation and achieve smooth void-free films.

2. Experiment and results

2.1. Pre-clean challenges of structured wafers

Pre-epi surface preparation of structured wafers processed through multiple implants and source/drain recess etch is challenging. Complete elimination of residual implant damage and process-related chemical residues is difficult to achieve without an aggressive wet clean or high-temperature bake. As a test, one blanket wafer and one structured wafer were subject to a diluted HF (DHF) clean followed by a low-temperature H_2 bake prior to SiGe epi film deposition. Due to process history and accumulated chemical residues (e.g. in recess etch), the structured wafer was first cleaned in ozonated DI water followed by SC1 before the DHF dip. SIMS measurements indicated that while integrated C and O levels at the Si–SiGe interface were maintained at 7×10^{11} cm^{-2} and 3×10^{12} cm^{-2}, respectively, on the blanket wafer, both C and O doses on the recessed wafer exceeded 10^{13} cm^{-2}.

2.2. Low-temperature chemical bake

Due to additional difficulties with cleaning structured wafers, a new low-temperature bake process besides the commonly used pre-epi H_2 bake was developed. Prior to SiGe deposition, device wafers were dipped in DHF and were introduced to the epi reactor in a flow of HCl, a reactant gas, and H_2 carrier gas. The HCl-based chemical bake step was found to remove the top Si surface containing damage and contaminants. As a result, employment of the HCl-based chemical bake lowered the interfacial C and O on the recessed S/D growth surfaces.

Figure 1 shows SIMS profiles of interface C and O as well as Ge in epitaxially grown SiGe films (*a*) after H_2 bake alone and (*b*) after HCl bake followed by the H_2 bake. The first thing to note is the lowering of C and O peak concentrations by an order of magnitude at the Si–SiGe interface. A uniform Ge profile was observed in the SiGe film grown after the HCl chemical bake while Ge pileup at the interface was observed at the Si–SiGe growth interface without the chemical bake.

To further verify the effect of HCl, two recessed wafers were processed by the same epi condition, but with different HCl treatment time. Figure 2 shows that HCl can recover surface condition once time and flow are optimized. Figure 2(*a*) shows that shorter HCl bake time does not produce good epi near a poly sidewall, but figure 2(*b*) shows that HCl bake can work, once HCl bake time conditions are optimized.

2.3. Effect of pre-epi DHF clean time

Pre-epi clean in DHF prior to epi deposition is commonly performed to remove native oxide and contaminants on the

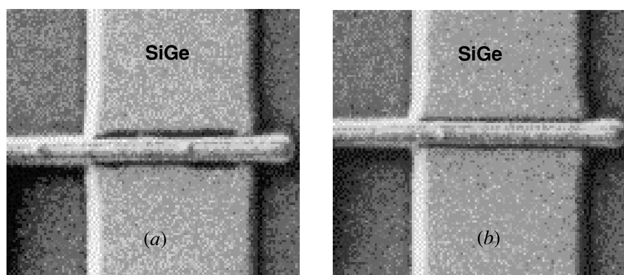


Figure 2. (*a*) Shorter time for HCl bake and (*b*) longer time for HCl bake.

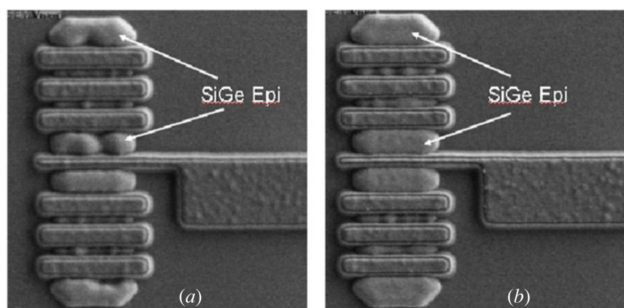


Figure 3. Top view SEM images of selective SiGe epi film after (*a*) shorter and (*b*) longer DHF clean time.

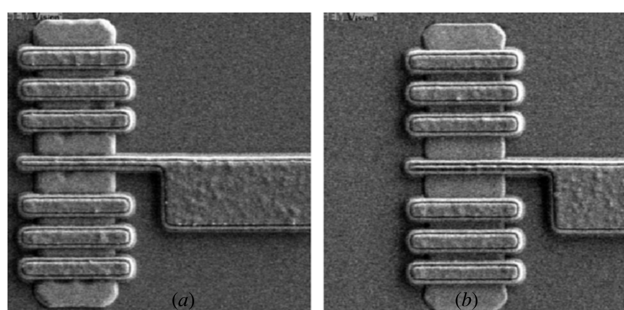


Figure 4. Top view SEM images of selective SiGe epi deposited after (*a*) one cycle of DIW-O_3/SC1 clean and (*b*) multi-cycles of DIW-O_3/SC1. Total HF time was the same.

growth surface. The DHF clean also serves as a surface (H) passivation step to prevent further contamination. Therefore, optimization of pre-epi HF dip time is critical in achieving an interface with minimal contaminants. In addition to residual contaminant reduction, our study reports that longer DHF clean further prepares the growth surface to improve epi film morphology. Two structured wafers were prepared in DHF for different clean times followed by low-temperature HCl-based chemical bake and SiGe epitaxial film deposition. SIMS results indicating residual C and O at the Si–SiGe interface were already reduced to below 10^{18} cm^3 and 10^{19} cm^3, respectively, after DHF clean. Besides, additional DHF clean did improve SiGe epi film quality. Figure 3 compares the top view SEM images of the two samples prepared by different DHF clean time. The SiGe film grown after shorter DHF clean time showed dimpling and uneven morphology while the film grown after double DHF clean time showed much smoother film morphology.

A long pre-epi DHF clean may not be realistic for many device structures due to undesirable etching of protective oxide over nFET areas. Over-etching of oxide film results in undesirable SiGe growth on nFET areas during the selective SiGe growth process. The maximum allowable DHF clean time or chemical budget of a device structure is set by the etch rates and thicknesses of the protective film layers used in the device structure.

2.4. Cyclical wet clean in DIW-O_3/SC1/DHF

An alternative pre-epi surface preparation to a long DHF clean is multiple cyclical cleaning through a DIW-O_3/SC1/DHF sequence. The combination of DIW-O_3 and SC1 removes organic residues and particles while oxidizing the Si surface. By repeating cycles of surface oxidation in DIW-O_3/SC1 and oxide strip in DHF, effective surface preparation was achieved for epitaxial film growth. Figure 4 compares the morphology of selectively deposited SiGe after (*a*) one cycle and (*b*) multi-cycles of O_3-DI/SC1/DHF wet clean with the same total DHF time. Significant improvement in surface morphology is shown in figure 4(*b*) obtained after multi-cycles of cleaning while figure 4(*a*) obtained after one cycle of cleaning showed dimpling along the gate/spacer side.

Multiple cycles of DIW-O_3/SC1/DHF clean also resulted in more consistent film growth rates over different recessed areas of various sizes. Figure 5 shows cross-sectional TEM images of SiGe grown in two opening sizes on the surfaces prepared by (*a*) one cycle and (*b*) multi-cycles of clean. The wafer cleaned with one cycle showed substantially thinner (30% less) SiGe in the smaller opening compared to the larger opening within the imaged area while the

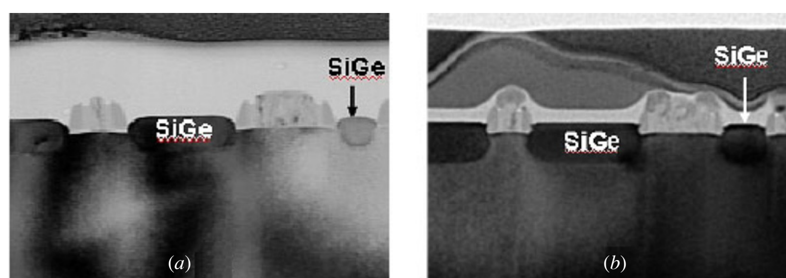


Figure 5. Cross-sectional TEM images of selectively grown SiGe epi in recessed Si after (*a*) one cycle and (*b*) multi-cycles of O_3-DI/SC1/DHF clean.

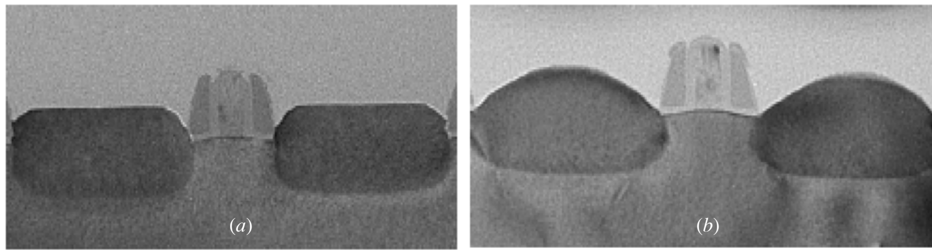
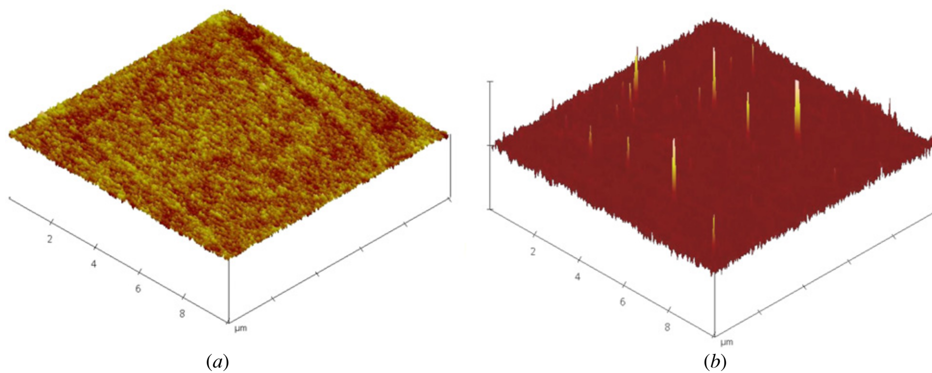


Figure 6. XTEM comparison of selectively grown SiGe film (*a*) with and (*b*) without Si seed.



(*a*) (*b*)

Figure 7. SiGe roughness (*a*) with and (*b*) without Si seed

wafer cleaned with multi-cycles showed no difference in thickness.

2.5. Si seed

For the most difficult surfaces to grow SiGe epitaxial film, a thin Si seed layer was employed to ease the nucleation of epitaxial film growth. Smooth and uniform growth of SiGe was observed on the seeding layer while pitting and voids resulted in SiGe epi grown without a seeding layer. The use of Si seed was also observed to improve growth rate variation in different pattern densities across the wafer.

Wafers with surface damage showed a difference in SiGe film morphology between wafers with and without the Si seed, as shown in figures 6(*a*) and (*b*), respectively. Improved surface morphology is observed in the clear faceting and lack of dislocations around the lateral recessed interface in the case of the Si seed. Also, the surface roughness recovered well in the different density areas of the wafer by Si seed, further improving micro-loading with a similar incubation time to nucleate the uniform SiGe film. Micro-loading between the isolated area and dense area was improved once the Si seed layer was applied. Micro-loading was defined as (maximum thickness − minimum thickness)/minimum thickness in the same die.

For roughness analysis by AFM, we can obtain better roughness in epi film with Si seed. The rms value is 0.188 nm for epi film with Si seed, and 0.481 nm for epi film without Si seed, respectively. The AFM images are shown in figure 7. It also indicates that the Si seed process can recover initial surface roughness and further improve the epi roughness.

A thin layer of Si seed was implemented on selective SiGe epitaxial film growth in recessed source and drain areas. It can improve the epi film morphology to prevent dislocations and improve micro-loading. Moreover, the epi surface roughness was improved.

3. Conclusion

The effects of low-temperature HCl/H_2 chemical bake, DHF clean time and DIW-O_3/SC1/DHF cycle wet cleaning on selective SiGe epi film growth are reported in this paper. The HCl/H_2 chemical bake removed the contaminated top surface and, as a result, effectively reduced C and O at the Si–SiGe growth interface under low-bake temperature. Besides, HCl can be optimized to obtain good epi morphology. Cyclical wet clean through a DIW-O_3/SC1/DHF chemistry sequence improved the growth surface and showed improved SiGe film morphology. Longer pre-epi DHF also showed improved epi film morphology; however, the maximum DHF clean time is set by erosion rates of protective layers and their thickness specification for a given device structure. Depending on thermal and chemical budgets of device structures, combinations of various pre-epi treatments and the Si seeding layer discussed in this paper can be used to improve the pre-epi surface, and consequently, SiGe epi quality.

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