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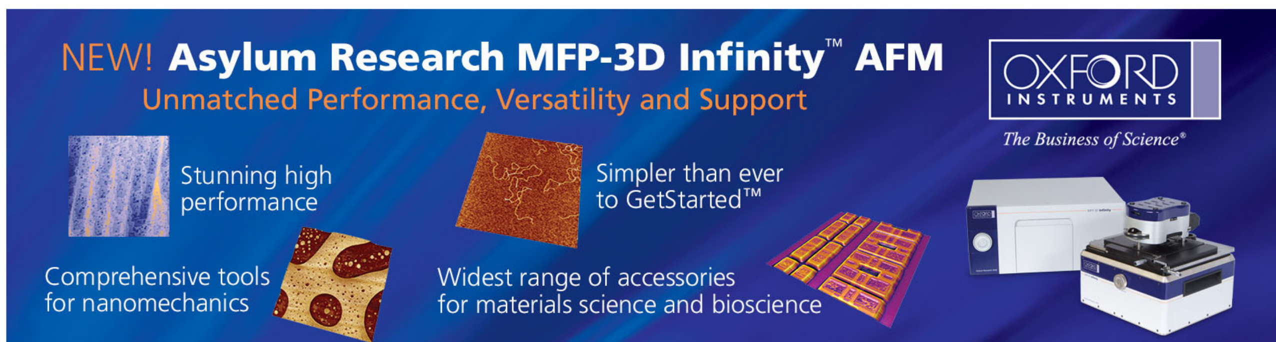

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Insight into the performance enhancement of double-gated polycrystalline silicon thin-film transistors with ultrathin channel

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In this letter, characteristics of independently-controllable double-gated polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with ultrathin channel are characterized and analyzed experimentally and theoretically. As compared with the single-gated mode where only one of the gates is used for driving the device, 1.3–2.1 fold increase in drive current is achieved under double-gated mode as the two gates are biased simultaneously for driving the device. A remarkable lowering of barrier height 7–12 meV in the latter case due to the coupling of the two gate biases is identified as the major origin for such performance enhancement. © *2010 American Institute of Physics*. [doi:10.1063/1.3327336]

Polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) are widely applied in various fields such as active matrix liquid-crystal-displays and three-dimensional electronics[1–3] due to the low temperature and mature fabrication technology. However, as compared with the metal-oxide-semiconductor transistors built on bulk-Si, a large amount of defects contained in the poly-Si channel film would dramatically aggravate the device performance in terms of high subthreshold swing (SS) and OFF-state leakage current.[1] Such concern can be relieved by thinning the channel to reduce the amount of defects[4,5] and/or the adoption of a multiple-gated configuration to enhance the gate controllability.[5–7] The latter approach has also been widely investigated in devices with monocrystalline Si channel.[8,9] By combining the above two approaches, SS smaller than 100 mV/dec can be achieved.[5] On the other hand, there are a lot of theoretical studies devoted to analyzing the properties of traditional planar poly-Si TFTs,[10–12] but few reports were done on the poly-Si-based devices with multiple-gated configuration. Since the carriers transport in the poly-Si channel is mainly affected by the conduction barriers formed at the grain boundaries,[10] the impacts of multiple-gate driving on the transport properties are expected to exhibit some unique features. This motivates us to carry out this study for better understanding of gate coupling on the performance of devices with ultrathin poly-Si channel and independent double-gate configuration.

Figure 1 is the simplified two-dimensional (2D) structure applied in the simulation.[13] The device is configured with two n^+ poly-Si gates having the same gate oxide thickness, and can be biased independently. *X*- and *y* directions are parallel and perpendicular to the channel direction (from source to drain), respectively. The position at depth $y=0$ corresponds to the interface between top gate oxide and channel. Owing to the ultrathin channel studied in this work, the poly-Si channel layer is assumed to have a bamboolike structure with the same grain size. According to previous works, the GB defect traps show Gaussian distribution near the midgap,[14,15]

$$N_d^* e^{-0.5^*(E - E_{\mathrm{midgap}} - 0.08/0.065)^2}, \qquad (1)$$

where E_{mg} is the mid-gap level and $N_d=2\times 10^{13}(\mathrm{eV}^{-1}\,\mathrm{cm}^{-2})$ is assumed in our simulation based on the analysis results with field-effect conductance analysis.[14] In addition to the defects in the grain boundaries, the intragrain states caused by distorted-band defects are assumed to distribute uniformly with fixed density and energy level, similar to the assumption made in Seto's model.[10] The trap density and trap level are employed as parameters to fit the experimental current-voltage characteristics. In this study, trap density of 2.85×10^{19} cm^{-3} with an energy level at 0.05 eV below the conduction band edge were used. Furthermore, the capture and emission processes are handled by the simulator using Shockley–Read–Hall recombination model and a conventional drift-diffusion method is used to model the carrier transport.

Figures 2(a) and 2(b) show the transfer and output current-voltage (*I*-*V*) characteristics, respectively, of a device operated in single-gated (SG) and double-gated (DG) operation. DG operation denotes that both gate electrodes are applied with the sweeping bias. While in SG operation, varying bias is applied to one of the two gate electrodes with the other one grounded. The characterized device is with channel thickness of 20 nm, gate oxide of 16 nm, and gate length of 5 μm. In the figures both simulated and measured results are shown and compared. The fabrication of the test devices can

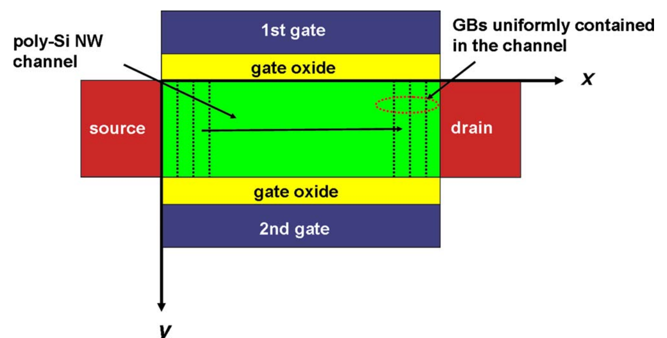

FIG. 1. (Color online) Simplified 2D schematic illustration of the device applied in 2D TCAD simulation.

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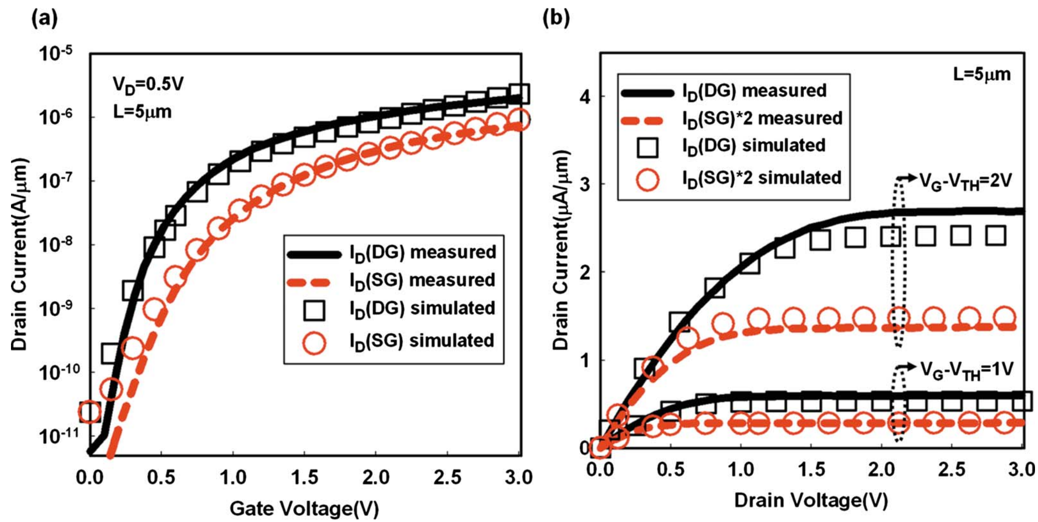

FIG. 2. (Color online) (a) Transfer and (b) output characteristics of the device with poly-Si channel thickness=20 nm, gate oxide=14 nm, and gate length=5 μm under DG and SG modes of operation. Both experimental (solid and dashed lines) and simulated (symbols) data are shown for comparison. In (b), the drain current of SG mode is multiplied by 2 for fair comparison with that of DG mode.

be found in Ref. 16. In the simulation, grain size of the poly-Si film is assumed to be 30 nm, based on the previous transmission electron microscopic (TEM) characterization results performed on the poly-Si films formed with solid-phase crystallization scheme.[16] It is seen that the simulation results well describe the observed behavior of the fabricated devices. It is also interesting to see in Fig. 2(b) that the drain current under DG mode of operation is much larger than twice the drain current under SG mode. It is postulated to be caused by the coupling effect of the two gate biases under DG operation. Note that such phenomenon is absent when the channel thickness becomes thicker than 50 nm.

According to the classic Levinson's model,[11] the drain current and barrier height are related by the following equation:

$$I_D = \frac{W}{L}\mu_0 n e^{-V_B/kT} V_{DS}, \tag{2}$$

where W and L are the width and length of the channel, respectively, n is the concentration of the induced electrons, μ_o is the mobility of the electrons inside the grain, kT is the thermal energy; V_B is the barrier height, and V_{DS} is the drain voltage. From Eq. (1), we can see that more V_B lowering causes more efficient thermionic emission and thus higher drain currents. To clarify this point, we extract the activation energy which represents the effective V_B of the conduction electrons[10,11] from the transfer curves of the fabricated device measured at V_D=0.1 V and temperature ranging from 30 to 90 °C [see the inset shown in Fig. 3(a)]. The results are shown in Fig. 3(a) as a function of gate voltage. As expected, V_B decreases with increasing gate voltage due to the increase in carrier concentration.[10] Moreover, V_B is much lower in the case of DG operation. It should be noted that V_B should be depth-dependent inside the channel of the device and the above results extracted from the experimental *I-V* curves are the effective barrier heights. To gain more insight, the simulated barrier heights at channel depth y=1, 3, and 5 nm are shown in Fig. 3(b). In the figure we can see that V_B becomes lower as y approaches the interface. It is attributed to a larger amount of induced electrons as y approaches the interface.

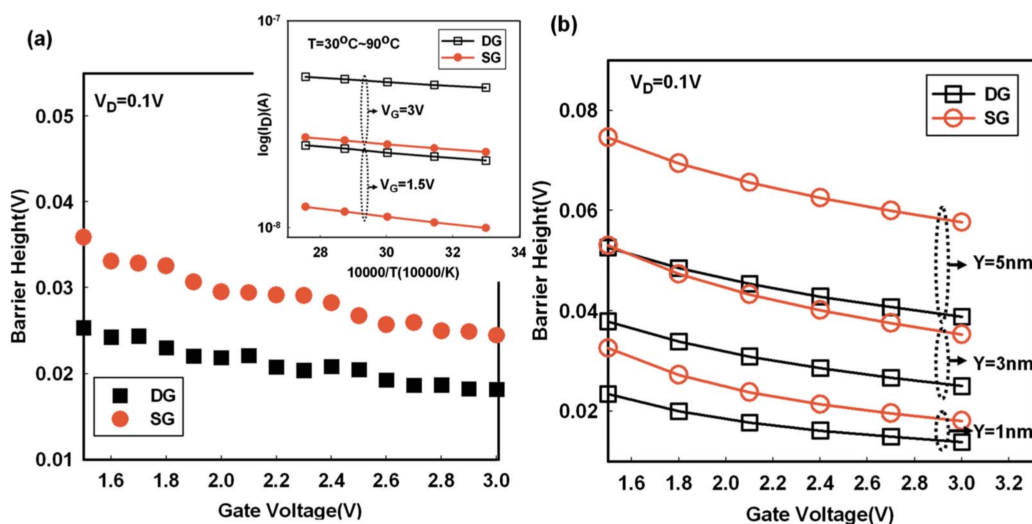

FIG. 3. (Color online) (a) Extracted V_B as a function of gate voltage for the device characterized in Fig. 2. The inset shows some of the log(I_D) vs T curves for extracting V_B. DG mode shows reduced V_B as compared with the SG mode. (b) The simulated V_B values at y=1, 3, and 5 nm.

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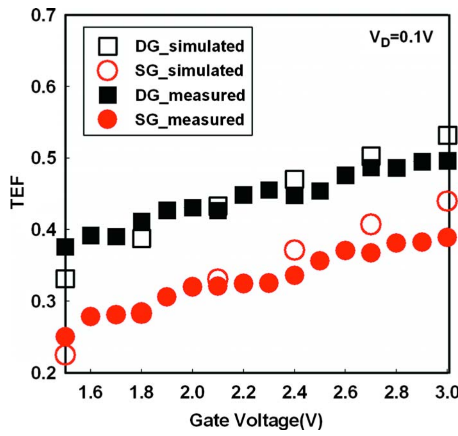

FIG. 4. (Color online) Comparisons of experimental and simulated TEF under DG and SG operations.

Moreover, due to coupling of the two separate gate biases as the channel body is sufficiently thin, larger barrier lowering with DG operation is confirmed in both experimental and simulated results as shown in Fig. 3. Such barrier lowering results in thermionic emission enhancement. In Fig. 4, according to Eq. (2), the thermionic emission factor, (TEF), is defined as,

$$\mathrm{TEF} = \exp\left(\frac{-V_B}{kT}\right). \tag{3}$$

The effective TEF can be obtained by substituting the extracted V_B into Eq. (3). To verify the experimental data with simulation we employ the following relation:

$$\mathrm{TEF} = \frac{\int_0^d n(y)\exp\left[\frac{-qV_B(y)}{kT}\right]dy}{\int_0^d n(y)dy}, \tag{4}$$

where d is the channel thickness, $n(y)$ and $V_B(y)$ are the simulated electron density and barrier height at depth y, respectively. As shown in Fig. 4, the simulated results show excellent agreement with the trend found experimentally. As compared with the SG operation, more efficient thermionic emission is resulted with the DG operation, owing to the enhancement in barrier lowering as the coupling of the two gate biases occurs.

In this work the physical mechanism responsible for the performance enhancement of poly-Si TFTs with ultrathin channel under DG operation is explored. The experimental data indicate that the DG operation results in additional barrier lowering and thus leads to significant improvement in the output drain current as compared with that of the SG operation. Such effect is verified with the simulation results.

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