# Analysis and Design of Two Low-Power Ultra-Wideband CMOS Low-Noise Amplifiers With Out-Band Rejection

Ching-Piao Liang, Pei-Zong Rao, Tian-Jian Huang, and Shyh-Jong Chung, *Senior Member, IEEE*

***Abstract*—Two 3–5-GHz low-power ultra-wideband (UWB) low-noise amplifiers (LNAs) with out-band rejection function using 0.18-$\mu$m CMOS technology are presented. Due to the Federal Communications Commission's stringent power-emission limitation at the transmitter, the received signal power in the UWB system is smaller than those of the close narrowband interferers such as the IEEE 802.11 a/b/g wireless local area network, and the 1.8-GHz digital cellular service/global system for mobile communications. Therefore, we proposed a wideband input network with out-band rejection capability to suppress the out-band properties for our first UWB LNA. Moreover, a feedback structure and dual-band notch filter with low-power active inductors will further attenuate the out-band interferers without deteriorating the input matching bandwidth in the second UWB LNA. The 55/48/45 dB maximum rejections at 1.8/2.4/5.2 GHz, a power gain of 15 dB, and 3.5-dB minimum noise figure can be measured while consuming a dc power of only 5 mW.**

***Index Terms*—Complementary metal–oxide semiconductor (CMOS), low-noise amplifier (LNA), out-band rejection, ultra-wideband (UWB).**

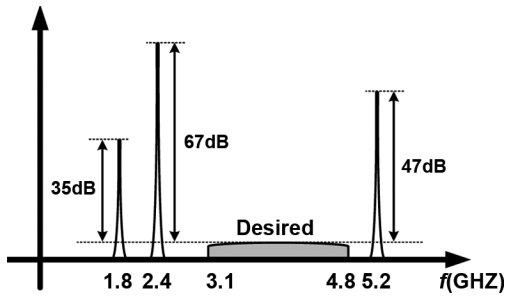



Fig. 1. Spectrum of the UWB system with large interferers.

TABLE I
NOTCH FILTER SPECIFICATIONS

| Standard | Notch center freq. (GHz) | 10 dB attenuation bandwidth (GHz) | Peak attenuation (dB) |
|---|---|---|---|
| GSM-1800/1900 | 1.85 | 1.71~1.99 | > 20 |
| 802.11b/g | 2.44 | 2.4~2.48 | |
| 802.11a | 5.25 | 5.15~5.35 | |

## I. INTRODUCTION

ULTRA-WIDEBAND (UWB) systems realize high data rate in the short-range wireless transmission, which are suitable for integration in various consumer electronics such as PCs, cellular phones, digital cameras, and PDAs. The minimum received power in the UWB channel is 47 and 67 dB, in the worst case, lower than those of the wireless local area network (WLAN) interferer powers at 5.2 and 2.4 GHz, respectively [1]. In addition, a tone is measured at 1.87 GHz in a smart phone currently on the market, and the power level is 35 dB higher than the UWB signal [2]. All of these interferers, as shown in Fig. 1, have a harmful effect on the received UWB signal; they can especially lead to the receiver gain compression and their possible intermodulation products can fall in-band. Although the interferers may further be attenuated by the baseband filter in the receiver, this does not address the problems of the intermodulation distortion and the receiver gain desensitization. In order to achieve reasonable performance for the above considerations, as summarized in Table I, more than 10-dB attenuation over the bandwidth of each interferer with 20-dB peak attenuation is appropriate in the front-end [3]–[7]. On the other hand, a larger attenuation in the front-end can also relax the baseband filter achieving an implementation with the smaller group-delay variations and lower dc power consumption [5].

Recently, a design of multiple-stopband filters is presented for the suppression of interfering signals such as global system for mobile communicatins (GSM), WLAN, and worldwide interoperability for microwave access (WIMAX) in UWB applications [3]. The coupled resonator stopband filter sections with bent resonators were adopted in order to more effectively suppress harmonics and the maximum rejection is about 25 dB at 1.8 GHz. However, this prototype of the filter, which was fabricated on the basis of the standard printed circuit board (PCB) process, will increase the entire UWB system area. Moreover, the multiple receivers with equal-gain combining were employed to eliminate the narrowband interferers received in the two paths and combined out-of-phase to cancel each other by selecting the optimal local oscillator (LO) phase [4]. A maximum 28-dB attenuation of the interferers was measured, but it is unavoidable to increase the system's complexity.

On the other hand, the topologies utilized for wideband amplifiers generally include the distributed configuration [8], [9], resistive shunt-feedback structure [10]–[12], common-gate $1/g_m$ termination [13]–[15], and *LC* input network [16], [17]. The distributed amplifiers are attractive for their ultra-wide bandwidth; however, the major drawbacks are the large area and high dc power consumption, which make them unsuitable for many applications. The resistive shunt-feedback and common-gate $1/g_m$

Manuscript received January 13, 2009; revised August 30, 2009. First published January 15, 2010; current version published February 12, 2010. This work was supported by the National Science Council of Taiwan under Contract NSC96-2752-E009-003-PAE.

The authors are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: sjchung@cm.nctu.edu.tw).

Digital Object Identifier 10.1109/TMTT.2009.2037855

0018-9480/$26.00 © 2010 IEEE

amplifiers can provide good impedance matching and moderate gain while dissipating small amounts of dc power, but without the out-band rejection capability. Recently, a new topology of the broadband amplifier for out-band rejection, which adopted a notch filter circuit with negative-resistance cell embedded, has been reported in [18] and [19]. Inevitably, the extra notch filter circuit made of inductors and cross-coupled transistors will occupy additional chip area and dc power simultaneously.

In this paper, we propose two topologies of the 3–5-GHz UWB low-noise amplifier (LNA) with out-of-band suppression by using the CMOS technology. In the first UWB LNA, a new wideband input impedance-matching network, which is based on the *LC* structure with focus on the improvement of out-of-band rejection capability, is presented. By suitably introducing two additional capacitors in the traditional *LC* input network, two transmission zeros at 1.8 and 8.5 GHz are generated to achieve the out-band rejection property without suffering from deterioration of the in-band performance. As an improvement of the first approach, the second proposed UWB LNA introduces a capacitive feedback path to the input *LC* network for further enhancing the rejection capability at the lower band transmission zero (1.8 GHz). A maximum 32-dB improvement is attained due to the usage of a feedback capacitor. A dual-band notch filter made of active inductors, which occupies only a small chip area, is also employed after the LNA core so as to attenuate the WLAN interferers at 2.4 and 5.2 GHz without influencing the noise figure (NF) of the LNA. The proposed active inductors are designed based on the cascode gain-boosting stage with a feedback resistor, which are with low consumption power while maintaining a sufficient $Q$ value. The introducing of both the feedback capacitor and the dual-band notch filter achieves maximum rejections of about 50 dB on the out-band interferers, which is superior to those presented in the literature [3], [4], [18], [19]. This paper is organized as follows. Sections II and III present the analyses of the first and second UWB LNAs, respectively. The circuit implementation and experimental results are illustrated in Section IV, followed by a conclusion in Section V. In this study, the circuit simulation is performed via Agilent's Advanced Design System (ADS) software with a TSMC design kit.

## II. First UWB LNA

The first 3–5-GHz CMOS UWB LNA proposed here adopts a source-degenerated cascode configuration, as shown in Fig. 2. An *LC* input network for wideband operation is utilized with two new capacitors $C_{RH}$ and $C_{RL}$ for increasing the higher and lower out-band rejections, respectively. The load inductor $L_L$ in series with the resistor $R_L$ helps to enhance the gain flatness. The buffer transistor $M_3$ with a purely resistive load $R_O$ is employed for testing purposes.

### A. Power Gain

The overall gain of the proposed LNA can be easily obtained as follows after a straightforward derivation:

$$S_{21} = \frac{(1+S_{11})\, v_{\text{out}}}{v_{\text{in}}} = (1+S_{11})\, \frac{v'_{\text{out}}}{v_{\text{in}}} \cdot g_{m3}(R_o \| Z_0). \tag{1}$$

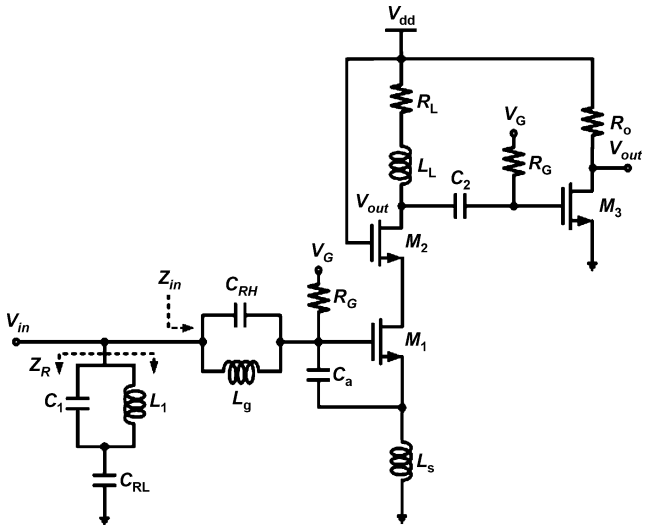



Fig. 2. Complete schematics of the first UWB LNA with out-band rejection.

where

$$\frac{v'_{\text{out}}}{v_{\text{in}}} = \frac{g_{m1}\left(1-\omega^2 L_g C_{RH}\right)}{\chi(\omega)} \cdot \left[(R_L + j\omega L_L) \left\| \frac{1}{j\omega C_L}\right.\right]. \tag{2}$$

with

$$\chi(\omega) = \omega^4 L_g L_s C_t C_{RH} - j\omega^3 L_g L_s g_{m1} C_{RH} - \omega^2 (L_g C_t + L_g C_{RH} + L_s C_t) + j\omega g_{m1} L_s + 1. \tag{3}$$

$Z_0$ is the 50-$\Omega$ source resistance, $C_t = C_{gs1} + C_a$, and $C_L$ is the total capacitance between the drain of the transistor $M_2$ and ground. $S_{11}$ is the reflection coefficient at the input port. From (1), it is seen that extra transmission zeros (i.e., $S_{21} = 0$) can be created when the following conditions are satisfied:

$$S_{11} = -1 \text{ or } \frac{v'_{\text{out}}}{v_{\text{in}}} = 0 \tag{4}$$

in which $S_{11} = -1$ means that the input impedance of the LNA is short circuit, and it occurs as the impedance $Z_R$, i.e., the impedance of the $L_1C_1$ tank in series with the capacitor $C_{RL}$ (see Fig. 2) is equal to zero, where

$$Z_R(\omega) = \frac{\left[1-\omega^2 L_1 (C_{RL}+C_1)\right]}{j\omega C_{RL}\left(1-\omega^2 L_1 C_1\right)}. \tag{5}$$

By using (2), (4), and (5), the locations of transmission zeros can be predicted as

$$\omega_{RH} = \frac{1}{\sqrt{L_g C_{RH}}} \quad \omega_{RL} = \frac{1}{\sqrt{L_1 (C_{RL}+C_1)}}. \tag{6}$$

### B. Optimum Out-Band Rejection

The above ratiocination reveals that the additional capacitors $C_{RH}$ and $C_{RL}$ will bring about two transmission zeros to ameliorate the out-band performance. However, the out-band rejection characteristics are restricted by the series resistance of the on-chip inductor. As seen from(6), the higher and lower out-band transmission zeros are associated with the inductors $L_g$ and $L_1$, respectively. These component values influence not

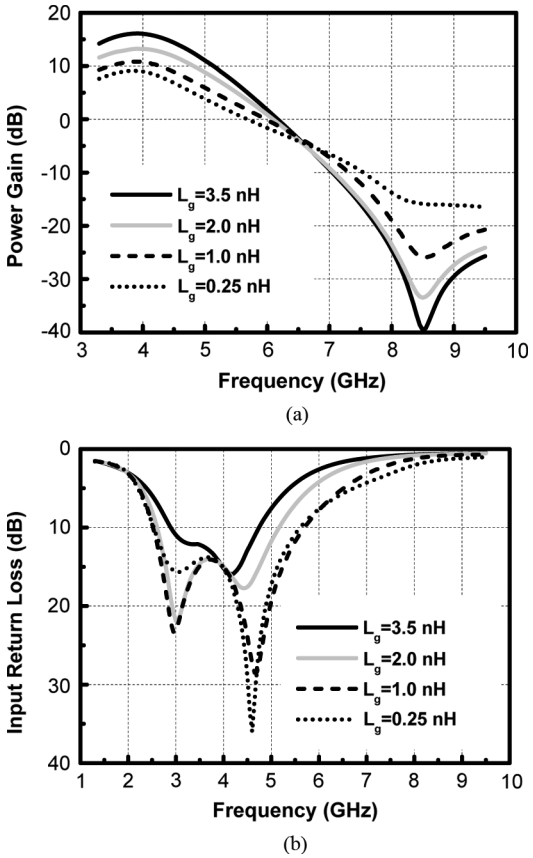



Fig. 3. (a) Simulated power gain $(S_{21})$ and (b) input return loss $(1/S_{11})$ for different values of $L_g$ with $L_1 = 2.0$ nH, $C_1 = 0.82$ pF, and $C_{RL} = 2.95$ pF. The transmission zero $\omega_{RH}$ is kept constant.

only the zeros' frequencies, but also the out-band suppression levels, as shown below.

Fig. 3(a) shows the power gain $(S_{21})$ versus frequency with different values of $L_g$. To begin with, it can be anticipated that the higher frequency out-band elimination efficiency is mainly determined by the impedance of the $L_gC_{RH}$ tank at the resonant frequency (i.e., the larger impedance, the superior out-band suppression). Therefore, the first step is to assign a larger $L_g$ to arrive at larger resonant impedance [20, Ch. 14]. In addition, a preferable power gain in the target frequency range can be procured contemporaneously by using a larger $L_g$, as shown in Fig. 3(a). However, an overlarge $L_g$ will lead to over abounded input impedance, as shown in Fig. 3(b), thus decreasing the input matching bandwidth of the LNA, which is not desirable for this design.

As is clear from (5), the impedance $Z_R$ in Fig. 2 produces one series and one parallel resonance from which the lower transmission zero can be created. It is expectable that a smaller impedance $Z_R$ at the series resonant frequency will accomplish the superior out-band elimination efficiency. Fig. 4 shows the relation between the impedance $Z_R$ and frequency for different $L_1$ values. As is seen, a smaller $L_1$ results in a smaller $Z_R$. This, in turn, does cause a deeper suppression level at $\omega_{RL}$ (1.8 GHz), as can be observed from the power gain versus frequency diagram shown in Fig. 5(a). Nevertheless, a drawback that may make the design unsatisfactory is that a diminishing $L_1$, and thus, a deceasing $Z_R$, may reduce the input impedance, and thus, deteriorate the matching condition, as demonstrated in Fig. 5(b).

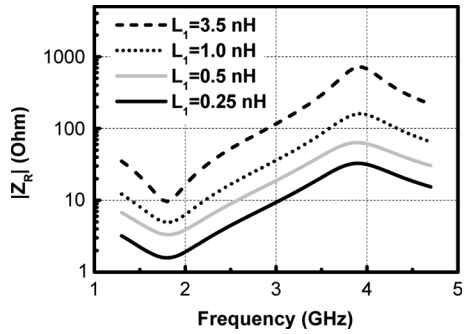



Fig. 4. Impedance $Z_R$ versus frequency with different values of $L_1$. The transmission zero $\omega_{RL}$ is kept constant.

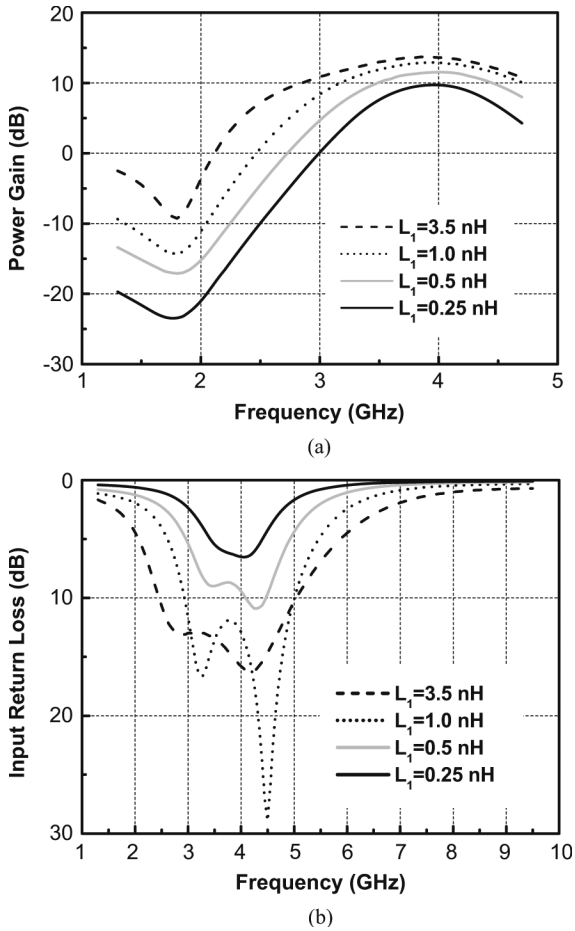



Fig. 5. (a) Simulated power gain $(S_{21})$ and (b) input return loss $(1/S_{11})$ for different values of $L_1$ with $L_g = 2.0$ nH, $L_s = 0.5$ nH, $C_{RH} = 0.17$ pF, and $C_a = 0.23$ pF. The transmission zero $\omega_{RL}$ is kept constant.

From the above discussion, it should be taken into account punctiliously by choosing appropriate values of $L_g$ and $L_1$ to achieve the tradeoff between the input match and out-band rejection performances.

It is interesting to see the influence of the input network on the LNA's NF. After a straightforward derivation following the procedure in [21], the NF of the circuit shown in Fig. 2 can be obtained as

$$\mathrm{NF} \propto \left[1 - \left(\frac{\omega}{\omega_{RH}}\right)^2\right]^{-2} \left[1 - \left(\frac{\omega}{\omega_{RL}}\right)^2\right]^{-2}. \quad (7)$$

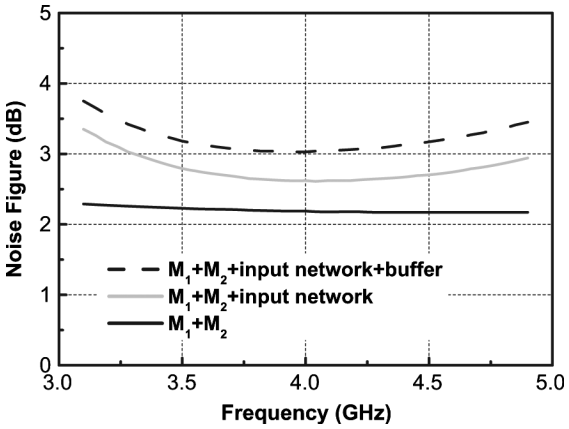



Fig. 6. Simulated NF of the first UWB LNA due to the active gain stages and the losses of the input network.

Obviously, the proposed UWB LNA will produce double-peak maxima in noise factor at the two transmission zeros. Consequently, it must be cautious to prevent from worsening the noise property in the desired frequency range when designing the locations of the zeros. Fig. 6 shows the simulation results of the NFs due to the active gain stage $(M_1 + M_2)$ only, $M_1 + M_2$ with the input network, and the total circuit. It can be observed that the dominant noise contributor is the active gain stage. The out-band rejection input network has a minor influence on the total NF as long as the designed transmission zeros are not too close to the in-band. To reduce the noise contribution from the active gain stage, the width of the transistor $M_1$ will be chosen for optimum noise property [22].

## III. Second UWB LNA

The first UWB LNA improves the higher and lower out-band performances by introducing the capacitors $C_{RH}$ and $C_{RL}$. However, a tradeoff between the input matching and out-band rejection should be carefully considered so as to make an optimum design. In the second approach, we utilize a feedback capacitor $C_{\rm FB}$ and active dual-band notch filter, as shown in Fig. 7, to attenuate the out-band interferers without deteriorating the input matching bandwidth.

### A. Effect of the Feedback Capacitor $C_{\rm FB}$

The capacitor $C_{RL}$ will engender the lower band transmission zero such as 1.8 GHz, but the rejection characteristic is restricted by the series resistance of on-chip inductor. For further suppression of the unwanted signal at 1.8 GHz, we introduce a feedback capacitor to the input *LC* network. As shown in Fig. 7, the voltage gain at node $X$ is equal to $-1$ if appropriate device sizes of $M_1$ and $M_2$ are selected so that the ratio $gm_1/gm_2$ equals unity. This makes the signal at node $X$ 180° out-of-phase with the input signal $V_{\rm in}$. On the other hand, the $L_1C_1$ tank, which provides a parallel resonance at the in-band operation, behaves as an equivalent inductor at 1.8 GHz. Consequently, a suitably designed feedback capacitor $C_{\rm FB}$ in series with the equivalent inductor can produce a series resonance at 1.8 GHz so that the out-of-phase signal at $X$ can be brought back to further cancel the input 1.8-GHz unwanted signal. In short,

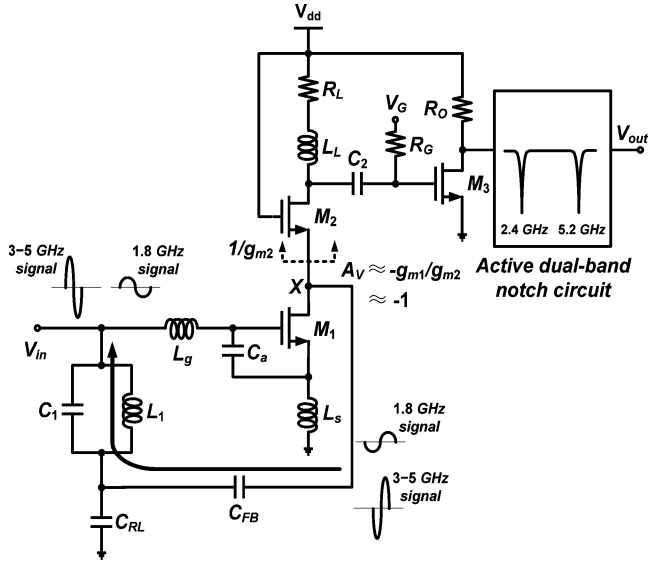



Fig. 7. Principle of the interferer-canceling technique with a feedback capacitor $C_{\rm FB}$ and active dual-band notch filter.

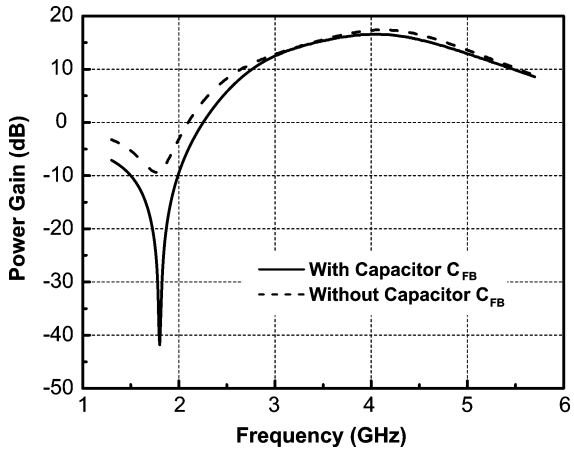



Fig. 8. Simulated power gain $(S_{21})$ of the second UWB LNA with and without the additional capacitor $C_{\rm FB}$.

the $L_1C_1$ tank behaves like an open circuit in the in-band, and thus, has little influence on the input impedance, while it may introduce an out-of-phase feedback signal to eliminate the unwanted 1.8-GHz signal. Fig. 8 shows the simulation results of the power gain with and without the additional capacitor $C_{\rm FB}$. It can be observed and demonstrated that a maximum 32-dB decrease in power gain is attained at 1.8 GHz while maintaining an identical in-band characteristic.

### B. Dual-Band Notch Filter

An on-chip dual-band notch filter is to be placed before the output of the second LNA, as shown in Fig. 7. Here, to avoid the deterioration in NF due to the loss of this notch filter, the filter stage is chosen to place after the gain stage. Fig. 9 illustrates the schematic of the proposed dual-band notch filter. The impedance $Z_A$ shown in the figure can be derived as

$$Z_A = \frac{\omega^4 L_3C_3L_4C_4 - \omega^2(L_3C_3 + L_3C_4 + L_4C_4) + 1}{j\omega C_3[(1 - \omega^2(L_3 + L_4)C_4]}. \quad (8)$$

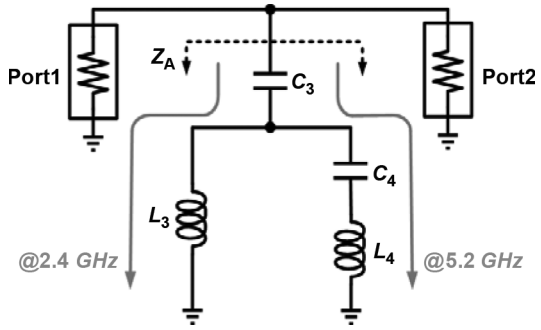



Fig. 9. Dual-band notch filter circuit.

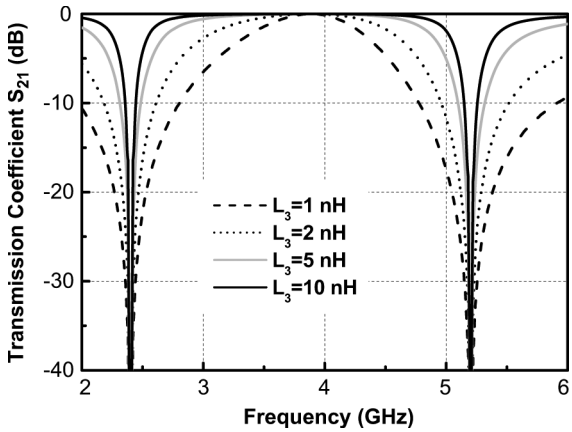



Fig. 10. Simulated transmission coefficient $S_{21}$ of the notch filter for different values of $L_3$.

The notch frequencies of the filter can be obtained by letting the numerator equal null or

$$\omega^4 L_3C_3L_4C_4 - \omega^2(L_3C_3 + L_3C_4 + L_4C_4) + 1 = 0 \quad (9)$$

which results in two transmission zeros $\omega_{z1}$ and $\omega_{z2}$ satisfying

$$\omega_{Z1}^2\omega_{Z2}^2 = \frac{1}{L_3C_3L_4C_4} \quad (10)$$

$$\omega_{Z1}^2 + \omega_{Z2}^2 = \frac{L_3C_3 + L_3C_4 + L_4C_4}{L_3C_3L_4C_4}. \quad (11)$$

Also, from (8), the impedance $Z_A$ contains a pole at

$$\omega_{P1}^2 = \frac{1}{(L_3 + L_4)C_4}. \quad (12)$$

In this study, we contrive that $\omega_{z1}$, $\omega_{z2}$, and $\omega_{p1}$ correspond to 2.4, 5.2, and 3.9 GHz, respectively. We will determine the appropriate values of $L_3$, $L_4$, $C_3$, and $C_4$ for the dual-band notch filter circuit in order to attenuate the WLAN interferers. It is noted that, after the decision of the positions of zeros and pole, we get three equations, i.e., (10)–(12), for the four filter components, which means that there is still one degree of freedom, let us say $L_3$, left for the circuit design. Fig. 10 shows the transmission coefficients $S_{21}$ of the notch filter with different $L_3$ values. As the value of $L_3$ increases, the in-band performance from 3.1 to 4.8 GHz will be improved; this means that we may use a larger inductance to maintain a better property in the target frequency

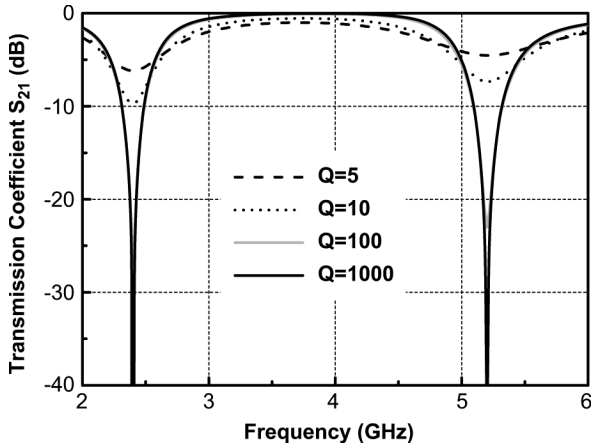



Fig. 11. Simulated transmission coefficient $S_{21}$ of the notch filter for different values of $Q$ with $L_3 = 5$ nH.

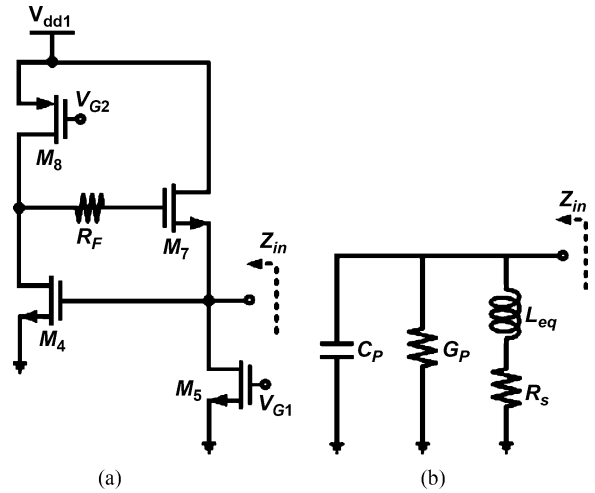



Fig. 12. (a) Schematic and (b) equivalent circuit of the active inductor with a resistor in the feedback path.

range. To achieve a 10-dB attenuation in both 2.4- and 5.2-GHz bands without suffering from deterioration of the in-band performance, the value of $L_3 = 5$ nH in the proposed notch filter will be chosen. On the other hand, the quality factor $Q$ of the inductor also influences the performance of the filter, as can be observed from Fig. 11, where the transmission coefficients of the filter for different inductor $Q$ values are shown. It is seen that a low quality factor will deteriorate the maximum attenuation of the notch filter. To obtain a 20-dB attenuation of the notch filter for the required specifications, the value of the quality factor $Q$ must be higher than 100. In general, the negative-resistance cell by using cross-coupled transistors can be employed to ameliorate the $Q$ value of the on-chip inductor. However, the larger inductors with cross-coupled transistors will concurrently occupy an overlarge chip area and dc power. Therefore, we are inclined to utilize active circuitry to substitute for the integrated passive inductors.

### C. Low-Power Active Inductors

The realization of inductances $L_3$ and $L_4$ is based on the active inductor with a feedback resistor proposed in [23].

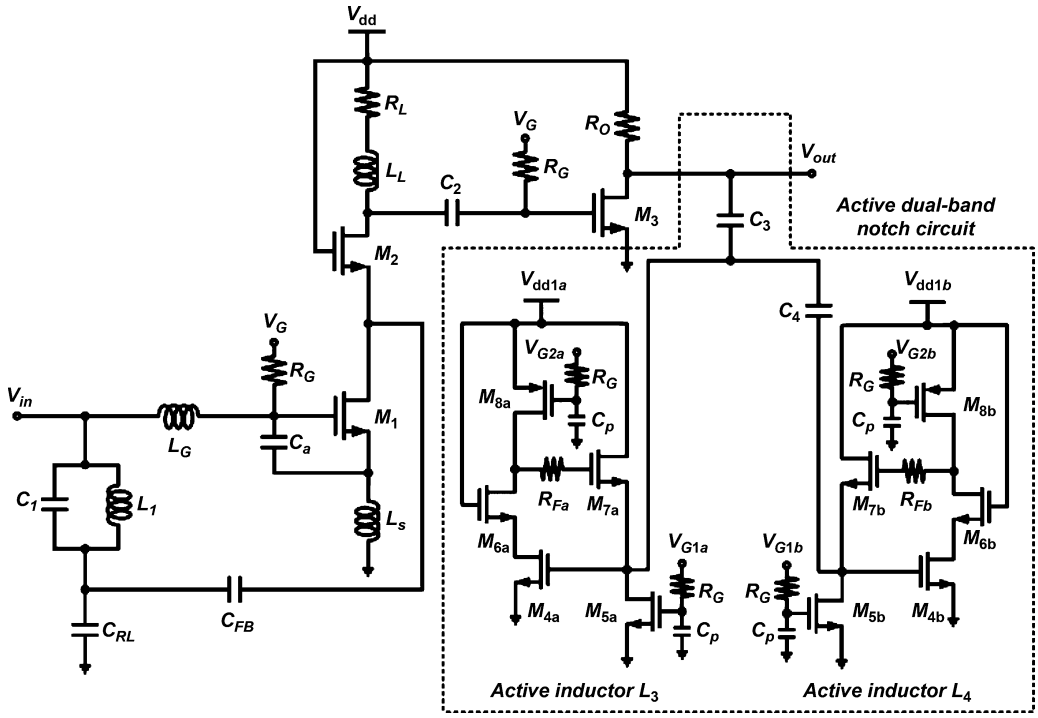



Fig. 13. Complete schematics of the proposed second UWB LNA.

Fig. 12(a) and (b) illustrates the circuit schematic and corresponding equivalent circuit. Through a simple derivation, the components of the equivalent circuit can be obtained as

$$L_{\rm eq} \approx \frac{C_{gs7}\left(1+g_{ds4}R_F\right)}{\left(g_{m4}g_{m7}\right)} \tag{13}$$

$$G_p \approx g_{ds7} + \frac{g_{m4}}{\left(1+g_{ds4}R_F\right)} \tag{14}$$

$$R_s \approx \frac{1}{\left(g_{m7}A_{v4}\right)} = \frac{g_{ds4}}{\left(g_{m7}g_{m4}\right)} \tag{15}$$

$$C_p \approx C_{gs4} \tag{16}$$

with $C_{gsi}$, $g_{dsi}$, and $g_{mi}$ being the gate–source capacitance, output conductance, and transconductance of the corresponding transistors, respectively. In general, the quality factor of the active inductor can be promoted by decreasing the values of $G_p$ and $R_s$. From (14), the use of the feedback resistor $R_F$ does reduce the value of the parallel conductance $G_p$ by introducing the factor $(1 + g_{ds4}R_F)$. In addition, a larger $g_{m7}g_{m4}$ is required, as shown in (15), to get lower value of $R_s$. However, this will increase the whole dc power consumption in the active inductor since $g_{mi}$ is proportional to the current of transistors. To overcome this drawback, here we modify the active inductor circuit by using the gain-boosting technique [24] to achieve a small amount of dc current while maintaining a sufficient $Q$ value. This is accomplished by using a cascode stage $M_4$ and $M_6$ to replace the only common-source transistor $M_4$, resulting in a new active inductor configuration, as shown in the complete schematic of the second UWB LNA in Fig. 13. The voltage gain in (15) can thus be substantially augmented and the value of $R_s$ will be obtained as

$$R_s \approx \frac{1}{\left(g_{m7}A_{v4}A_{v6}\right)} = \frac{g_{ds4}g_{ds6}}{\left(g_{m7}g_{m4}g_{m6}\right)}. \tag{17}$$

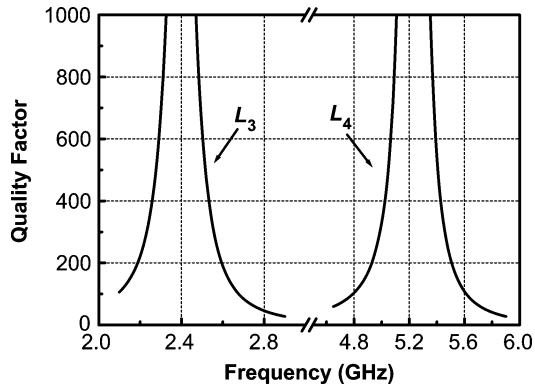
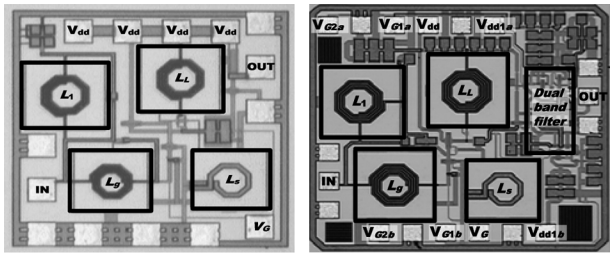



Fig. 14. Simulated quality factor of the proposed active inductors $L_3$ and $L_4$.

Therefore, a low-power active inductor is easily accomplished due to the use of the cascode gain-boosting stage with a feedback resistor. Fig. 14 illustrates the simulated $Q$ factor of the proposed active inductor, which shows that the active inductor exhibits a $Q$ factor larger than 1000 at both 2.4- and 5-GHz bands. These high-$Q$ inductors undoubtedly provide a larger attenuation at the interferer frequencies, as can be observed from Fig. 11. Only 0.55-mA (for $L_4$) and 0.8-mA (for $L_3$) dc currents are required in the second UWB LNA circuit shown in Fig. 13, which are smaller than those in the previous literature [23]–[25].

Moreover, it is obvious in (13) that the inductance of an active inductor is related to the transconductances, and thus, the bias currents, of the transistors. Consequently, the notch frequencies will be effectively tuned by adjusting the bias currents of the active inductor. The externally controlled bias voltages $V_{G1}$ and $V_{G2}$ in Fig. 13 are designed here for adjusting the bias currents to compensate the frequency shift due to the process variation.




(a) (b)

Fig. 15. Microphotograph of: (a) the first UWB LNA with $0.78 \times 0.8$ mm$^2$ die area and (b) the second UWB LNA with $0.9 \times 0.85$ mm$^2$ die area.

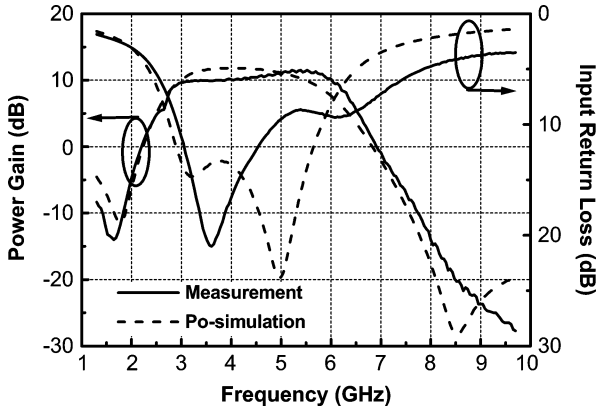



Fig. 16. Measured and simulated power gain $(S_{21})$ and input return loss $(1/S_{11})$ of the first UWB LNA.

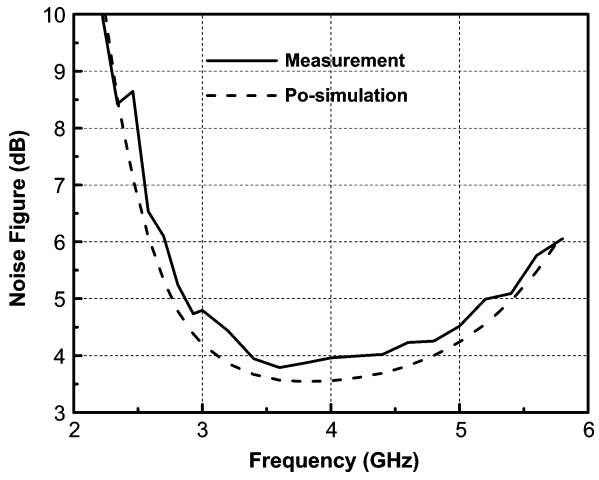



Fig. 17. Measured and simulated NF of the first UWB LNA.

For further design, these control voltages $V_{G1}$ and $V_{G2}$ can be utilized together with a feedback mechanism demonstrated in [6] and [7] and [26] and [27] for automatically calibrating the frequency drift of the notch filters.

## IV. Implementation and Measurements

The proposed out-band rejection UWB LNAs are designed and fabricated using the TSMC 0.18-$\mu$m CMOS process. Moreover, on-wafer probing is performed to measure the characteristics of the LNA circuits.

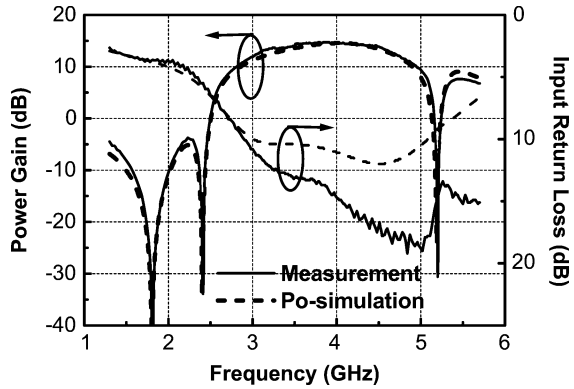



Fig. 18. Measured and simulated power gain $(S_{21})$ and input return loss $(1/S_{11})$ of the second UWB LNA.

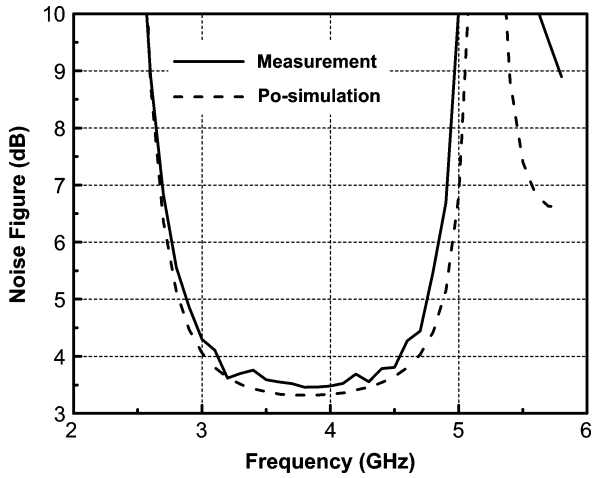



Fig. 19. Measured and simulated NF of the second UWB LNA.

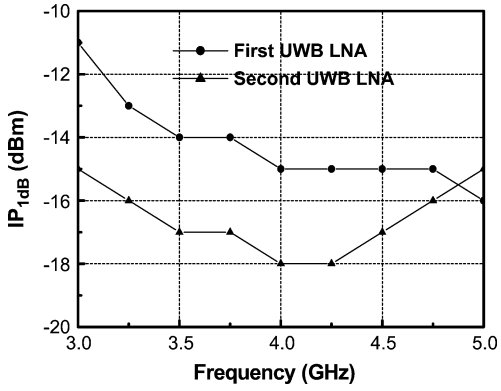



Fig. 20. Measured $\mathrm{IP_{1dB}}$ of the proposed UWB LNAs.

### A. First UWB LNA With Capacitors $C_{RH}$ and $C_{RL}$

For the first UWB LNA shown in Fig. 2, the width of the transistor $M_1$ $(225\ \mu\mathrm{m})$ is optimized with 2.5-mW power dissipation to achieve good noise property. The size of the cascode transistor $M_2$ $(320\ \mu\mathrm{m})$ is selected to be as large as possible to reduce its voltage headroom requirement, which is conducive to low-voltage operations. In addition, the design of the input network will engender the tradeoff between the input match and out-band rejection characteristics, which can be observed

TABLE II
UWB LNA PERFORMANCE SUMMARY

| Reference | Technology | $V_{DD}$ [V] | $BW$ [GHz] | $S_{11}$ [dB] | $G_{max}$ [dB] | $NF_{min}$ [dB] | $P_{diss}$ [mW] | Area [mm$^2$] | Out-band rejection |
|---|---|---|---|---|---|---|---|---|---|
| [28] | 0.18 μm CMOS | 1.8 | 3 ~ 6 | < -12 | 15.9 | 4.7 | 59.4 | 1.1 | - |
| [29] | 0.25 μm CMOS | 2.5 | 3.2 ~ 4.8 | < -10 | 7.5 | 2.7** | 20* | - | - |
| [30] | 0.13 μm CMOS | 2 | 2 ~ 5.2ζ | < -9 | 16 | 4.7 | 38 | 0.24 | - |
| [31] | 0.35 μm BiCMOS | 3 | 2.5 ~ 5.5 | < -9 | 11.8 | 2.1** | 9* | 1.13 | - |
| [32] | 0.13 μm CMOS | 1.5 | 2 ~ 4.6 | < -10 | 9.5 | 3.5 | 16.5* | 1.08 | - |
| [33] | 0.18 μm CMOS | 1.3 | 0.04 ~ 7 | < -16 | 8.6 | 4.2 | 9 | 1.16 | - |
| [34] | 0.18 μm CMOS | 1.8 | 2.8 ~ 7.2 | < -4 | 19.1 | 3 | 32 | 1.63 | - |
| [35] | 0.18 μm CMOS | 1.8 | 3 ~ 4.8 | < -10 | 13.9 | 4.7 | 14.6 | 0.95 | - |
| [36] | 0.18 μm CMOS | 1.5 | 3 ~ 4.8 | < -7 | 16 | 2.7 | 11.9* | 1.8 | 15 dB @2.4 GHz<br>19 dB @5.3 GHz |
| [18] | 0.13 μm CMOS | 1.5 | 3 ~ 5 | < -10 | 19.4Ψ | 3.5 | 31.5 | 1.6 | 6 dB @2.4 GHz<br>44 dB @5.2 GHz |
| [19] | 0.18 μm CMOS | 1.8 | 3 ~ 4.8 | < -10 | 19.7 | 4.0 | 24 | 1.43 | 13 dB @2.4 GHz<br>20 dB @5.8 GHz |
| This work LNA1 | 0.18 μm CMOS | 0.9 | 2.8 ~ 6.2 | < -9 | 11.5 | 3.8 | 2.5* | 0.62 | 25 dB @1.8 GHz<br>32 dB @8.5 GHz |
| This work LNA2 | 0.18 μm CMOS | 1.8 | 3 ~ 4.8 | < -10 | 15 | 3.5 | 5* | 0.76 | 55 dB @1.8 GHz<br>48 dB @2.4 GHz<br>45 dB @5.2 GHz |

Ψ voltage gain ζ 1dB bandwidth * only core LNA ** external inductors for the input matching network

in Figs. 3 and 5. Hence, it should be chosen cautiously to obtain a reasonably out-band rejection performances in the target input matching bandwidth. In this study, the components values of the input network are $L_1 = 1.8$ nH, $L_g = 2.0$ nH, $L_s = 0.5$ nH, $C_1 = 0.91$ pF, $C_{RL} = 3.3$ pF, $C_{RH} = 0.17$ pF, and $C_a = 0.23$ pF . The load consists of the on-chip inductor $L_L$ in series with the resistor $R_L$ to achieve flat gain over the whole bandwidth. The components values of the load are $L_L = 2.4$ nH and $R_L = 15\,\Omega$. Moreover, the value of $R_o$ in this and the following LNAs is set as 50 Ω to achieve output match for testing purposes. A die microphotograph of the first UWB LNA is shown in Fig. 15(a) and the die area including pads is $0.78 \times 0.8$ mm$^2$.

The first UWB LNA drew a 2.8-mA dc core current from the 0.9-V supply voltage. The $S$-parameters of the designed LNAs were measured using the Agilent 8510C vector network analyzer. The simulated and measured results of power gain and input return loss are depicted in Fig. 16. The measured peak gain is 11.5 dB with a 3-dB bandwidth of 3.4 GHz from 2.8 to 6.2 GHz and the input return loss is better than 8.7 dB in the operation bandwidth. Moreover, due to the addition of the capacitors $C_{RH}$ and $C_{RL}$, extra transmission zeros are created and measured at 1.7 and 10 GHz. The NF was measured using the Agilent N8975A NF analyzer with Agilent 346C noise source. The simulated and measured NFs at the same bias condition are depicted in Fig. 17. It is seen that the minimum value of the measured NF is equal to 3.8 dB at 3.6 GHz.

### *B. Second UWB LNA With a Feedback Capacitor $C_{\rm FB}$ and Active Dual-Band Notch Network*

For the second UWB LNA shown in Fig. 13, the components values of the active inductors are as follows: $M_{4a} = 60$ μm , $M_{5a} = 4.5$ μm, $M_{6a} = M_{7a} = 37.5$ μm, $M_{8a} = 1.5$ μm, $M_{4b} = 16.5$ μm, $M_{5b} = 2.1$ μm, $M_{6b} = 31.5$ μm, $M_{7b} = 35$ μm, $M_{8b} = 2.7$ μm, $R_{Fa} = 125\,\Omega$, and $R_{Fb} = 1.1$ kΩ. A die microphotograph of the second LNA is shown in Fig. 15(b) and the die area including pads is $0.9 \times 0.85$ mm$^2$.

The total dc power of the second UWB LNA without an output buffer is 5 mW, drawn from 0.9- and 1.8-V power supply. The simulated and measured results of power gain and input return loss are depicted in Fig. 18. The measured peak gain is 15 dB from 3 to 4.8 GHz and the input return loss is better than 10 dB in the operation frequencies while the maximum rejections at 1.8, 2.4, and 5.2 GHz are 55, 48, and 45 dB, respectively. The simulated and measured NFs are depicted in Fig. 19 and the measured minimum NF is 3.5 dB at 3.9 GHz. The input-referred 1-dB compression point ($\rm IP_{1dB}$) of the proposed LNAs performed with an Agilent 83640B signal generator and 8564EC spectrum analyzer are depicted in Fig. 20. Minimum values of the measured $\rm IP_{1dB}$ in the first and second UWB LNAs are −16 and −18 dBm, respectively. The presented LNAs are compared with a recently published CMOS LNA and summarized in Table II.

## V. CONCLUSION

In this paper, we proposed two UWB LNA configurations with out-band rejection ability and demonstrated them by using the TSMC 0.18-$\mu$m CMOS process. Extra transmission zeros are created in the first UWB LNA due to the use of an *LC* input network with additional capacitors $C_{RH}$ and $C_{RL}$ for improving the higher and lower out-band performances, respectively. Furthermore, using a feedback capacitor and dual-band notch filter made of the low-power active inductors can achieve the maximum rejections of about 50 dB at the out-band interferers, which was demonstrated in the proposed second UWB LNA. The measured results, including the power gain, return loss, and NF, agree quite well with the simulated results.

## ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center (CIC), Taiwan, for the help of chip fabrication.

## REFERENCES

[1] S. Lo, I. Sever, S.-P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, V. T. Phan, and T. Nguyen, "A dual-antenna phased-array UWB transceiver in 0.18-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2776–2786, Dec. 2006.

[2] T. W. Fischer, B. Kelleci, K. Shi, A. I. Karsilayan, and E. Serpedin, "An analog approach to suppressing in-band narrow-band interference in UWB receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 5, pp. 941–950, May 2007.

[3] K. Rambabu, M. Y.-W. Chia, K. M. Chan, and J. Bornemann, "Design of multiple-stopband filters for interference suppression in UWB applications," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3333–3338, Aug. 2006.

[4] I. Sever, S. Lo, S.-P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, and T. Nguyen, "A dual-antenna phase-array ultra-wideband CMOS transceiver," *IEEE Commun. Mag.*, vol. 44, no. 8, pp. 102–110, Aug. 2006.

[5] A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez, and E. Sánchez-Sinencio, "An 11-band 3–10 GHz receiver in SiGe BiCMOS for multiband OFDM UWB communication," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 935–948, Apr. 2007.

[6] A. Bevilacqua, A. Maniero, A. Gerosa, and A. Neviani, "An integrated solution for suppressing WLAN signals in UWB receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 8, pp. 1617–1625, Aug. 2007.

[7] A. Vallese, A. Bevilacqua, C. Sandner, M. Tiebout, A. Gerosa, and A. Neviani, "Analysis and design of an integrated notch filter for the rejection of interference in UWB systems," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 331–343, Feb. 2009.

[8] X. Guan and C. Nguyen, "Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3278–3283, Aug. 2006.

[9] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1892–1905, Sep. 2007.

[10] Y. Park, C.-H. Lee, J. D. Cressler, and J. Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pp. 1687–1697, Apr. 2006.

[11] P. Z. Rao, Y. C. Cheng, C. P. Liang, and S. J. Chung, "Cascode feedback amplifier combined with resonant matching for UWB system," in *Proc. Progr. Electromagn. Res. Symp.*, Mar. 2007, pp. 1040–1043.

[12] J. Lee and J. D. Cressler, "Analysis and design of an ultra-wideband low-noise amplifier using resistive feedback in SiGe HBT technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 3, pp. 1262–1268, Mar. 2006.

[13] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18-$\mu$m CMOS selective receiver front-end for UWB applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1764–1771, Aug. 2006.

[14] Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, and Z. Lu, "A novel CMOS low-noise amplifier design for 3.1- to 10.6-GHz ultra-wideband wireless receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1683–1692, Aug. 2006.

[15] X. Li, S. Shekhar, and D. J. Allstot, "$Gm$-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-$\mu$m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[16] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[17] A. Ismail and A. A. Abidi, "A 3–10-GHz low-noise amplifier with wideband *LC*-ladder matching network," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.

[18] A. Bevilacqua, A. Vallese, C. Sandner, M. Tiebout, A. Gerosa, and A. Neviani, "A 0.13-$\mu$m CMOS LNA with integrated balun and notch filter for 3 to 5 GHz UWB receivers," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2007, pp. 420–421.

[19] Y. Gao, Y. J. Zheng, and B. L. Ooi, "0.18-$\mu$m CMOS dual-band UWB LNA with interference rejection," *Electron. Lett.*, vol. 43, no. 20, pp. 1096–1098, Sep. 2007.

[20] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2000.

[21] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[22] K.-J. Sun, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "A noise optimization formulation for CMOS low-noise amplifiers with on-chip low-$Q$ inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pp. 1554–1560, Apr. 2006.

[23] M.-J. Wu, J.-N. Yang, and C.-Y. Lee, "A constant power consumption CMOS *LC* oscillator using improved high-$Q$ active inductor with wide tuning-range," in *Proc. IEEE 47th Midwest Circuits Syst. Symp.*, Jul. 2004, vol. 3, pp. 347–350.

[24] U. Yodprasit and J. Ngarmnil, "$Q$-enhancing technique for RF CMOS active inductor," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2000, pp. 589–592.

[25] H.-H. Hsieh, Y.-T. Liao, and L.-H. Lu, "A compact quadrature hybrid MMIC using CMOS active inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 6, pp. 1098–1104, Jun. 2007.

[26] T. Das, A. G. C. Washburn, and P. R. Mukund, "Self-calibration of input-match in R.F. front-end circuitry," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 12, pp. 821–825, Dec. 2005.

[27] A. Vallese, A. Bevilacqua, C. Sandner, M. Tiebout, A. Gerosa, and A. Neviani, "An analog front-end with integrated notch filter for 3–5 GHz UWB receivers in 0.13 $\mu$m CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Munich, Germany, Sep. 2007, pp. 139–142.

[28] C.-P. Chang and H.-R. Chuang, "0.18-$\mu$m 3–6 GHz CMOS broad-band LNA for UWB radio," *Electron. Lett.*, vol. 41, no. 12, pp. 696–698, Jun. 2005.

[29] J. Lerdworatawee and W. Namgoong, "Wide-band CMOS cascode low noise amplifier design based on source degeneration topology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2327–2334, Nov. 2005.

[30] R. Gharpurey, "A broad-band low noise front-end amplifier for ultra-wideband in 0.13 $\mu$m," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1983–1986, Sep. 2005.

[31] M. Liu, J. Craninckx, N. M. Iyer, M. Kuijk, and A. R. F. Barel, "A 6.5 kV ESD-protected 3–5-GHz ultra-wideband BiCMOS low noise amplifier using interstage gain roll-off compensation," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pp. 1698–1706, Apr. 2006.

[32] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3–5 GHz ultra-wideband wireless receivers," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 3, pp. 134–136, Mar. 2006.

[33] F. Zhang and P. R. Kinget, "Low-power programmable gain CMOS distributed LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.

[34] Y.-J. E. Chen and Y.-I. Huan, "Development of integrated broad-band CMOS low noise amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2120–2127, Oct. 2007.

[35] M. l. Jeong, J. N. Lee, and C. S. Lee, "Design of UWB switched gain controlled LNA using 0.18-$\mu$m CMOS," *Electron. Lett.*, vol. 44, no. 7, pp. 477–478, Mar. 2008.

[36] S.-K. Tang, K.-P. Pun, C.-S. Choy, C.-F. Chan, and K. N. Leung, "A fully differential band-selective low-noise amplifier for MB-OFDM UWB receivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 7, pp. 653–657, Jul. 2008.

**Ching-Piao Liang** was born in Changhwa, Taiwan, in 1980. He received the B.S. and M.S. degrees in communication engineering from Yuan Ze University, Taoyuan, Taiwan, in 2003 and 2005, respectively, and is currently working toward the Ph.D. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan.

His primary research interests include RF integrated circuits and monolithic microwave integrated circuits.

**Pei-Zong Rao** was born in Kaohsiung, Taiwan, in 1980. He received the B.S. degree in physics from National Kaohsiung Normal University, Kaohsiung, Taiwan, in 2002, and is currently working toward the Ph.D. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan.

His research interests include RF integrated circuits, multiband wireless systems, and frequency synthesizer designs.

**Tian-Jian Huang** was born in Taichung, Taiwan, in 1983. He received the B.S. and M.S. degrees in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2006 and 2008, respectively.

His research focuses on RF integrated circuit design.

**Shyh-Jong Chung** (M'92–SM'06) was born in Taipei, Taiwan. He received the B.S.E.E. and Ph.D. degrees from National Taiwan University, Taipei, Taiwan, in 1984 and 1988, respectively.

Since 1988, he has been with the Department of Communication Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he is currently a Professor and serves as the Director of the Institute of Communication Engineering. From September 1995 to August 1996, he was a Visiting Scholar with the Department of Electrical Engineering, Texas, A&M University, College Station. His areas of interest include the design and applications of active and passive planar antennas, low-temperature co-fired ceramic (LTCC)-based RF components and modules, packaging effects of microwave circuits, vehicle collision warning radars, and communications in intelligent transportation systems (ITSs).

Dr. Chung was the treasurer of the IEEE Taipei Section (2001–2003) and the chairman of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Taipei Chapter (2005–2007). He was the recipient of the 2005 Outstanding Electrical Engineering Professor Award of the Chinese Institute of Electrical Engineering and the 2005 Teaching Excellence Award of National Chiao Tung University.