A 250 MHz 14 dB-NF 73 dB-Gain 82 dB-DR Analog Baseband Chain With Digital-Assisted DC-Offset Calibration for Ultra-Wideband

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***Abstract*—A 250 MHz analog baseband chain for Ultra-Wideband was implemented in a 1.2 V 0.13 μm CMOS process. The chip has an active area of 0.8 mm^2. In the analog baseband, PGAs and filters are carried out by current-mode amplifiers to achieve wide bandwidth and wide dynamic range of gain, as well as low noise and high linearity. Besides, a current-mode Sallen–Key low-pass filter is adopted for effective rejection of out-of-band interferers. A 6th-order Chebyshev low-pass filter realized in G_m-C topology is designed in the baseband chain for channel selection. Digitally-assisted DC-offset calibration improves second-order distortion of the entire chain. The design achieves a maximum gain of 73 dB and a dynamic range of 82 dB. Measured noise figure is 14 dB, an IIP3 of −6 dBV, and IIP2 of −5 dBV at the maximum gain mode. The analog baseband chain consumes 56.4 mA under supply of 1.2 V.**

***Index Terms*—Analog filter, current-mode filter, current-mode VGA, DC offset calibration, analog baseband, ultra wideband.**

I. Introduction

ENLARGING signal bandwidth is the most direct way to increase the data rate in wireless transmission. For the purpose, the spectrum from 3.1 GHz to 10.6 GHz was approved by FCC for commercial applications of Ultra-Wideband (UWB) systems in 2002. Proposed by the WiMedia alliance as Multi-Band (MB) OFDM UWB, the system realizes a high date rate of 480 Mbits/s in short-range communication as a wireless technique to replace cables. The spectrum is partitioned into five band groups. Each band group consists of three bands with a bandwidth of 500 MHz, which leads to a large baseband bandwidth of 250 MHz in direct-conversion receivers [1], [2]. Large signal bandwidth, however, leads to an interference problem. It occurs that signals of other narrowband communication systems, such as WiMax and WLAN, appear as interferers to an UWB RF receiver, causing strict linearity requirement [3].

An UWB RF receiver is composed of a broadband RF front-end and a wideband analog baseband. While the RF front-end boosts up the signal level, interferers will also be amplified. Typically the RF front-end carries out a low gain level, as compared to that in a narrowband receiver, such that the analog baseband can sustain those interferers. Consequently the analog baseband shall provide sufficient gain with very low input-referred noise to meet noise and gain requirements of the entire receiver. It therefore includes programmable gain amplifiers (PGAs) and filters. PGAs provide sufficient dynamic range, while filters give channel selection. In general, it is preferred to arrange in the order of PGAs, filters and PGAs for the optimal performance regarding to noise and linearity consideration of the overall analog baseband.

PGAs and filters are typically designed in voltage-mode operational amplifier (op amp)-based circuits in narrowband communication systems [4]. Those voltage amplifiers have advantages of good gain accuracy, low process-voltage-temperature (PVT) variation, and low power consumption. But they have a very limited bandwidth at high closed-loop gains, typically up to several tens of megahertz. Furthermore, in advanced deep sub-micron processes, linearity performance is greatly affected by rapid decrease of the maximum voltage rating as devices are scaled down. Therefore, it is getting harder to design high performance voltage-mode circuits. On the other hand, current-mode amplifiers turn out more suitable for realizing the UWB analog baseband. Low impedance at current-mode circuit nodes easily leads to a wider operating bandwidth [5], [6]. In addition, current-mode circuits feature high linearity owing to small voltage swings and lower supply voltage sensitivity than voltage-mode circuits. In 1968, a current conveyer was proposed as the first building block intended for current signal processing [7], then several proposals for a CMOS current-mode OP-Amp have been published [8], [9]. In 1997, BJT-based current-mode variable gain amplifiers (VGAs) are successfully realized by a trans-linear loop with at least 250 MHz bandwidth, good blocking and inter-modulation (IM) performance [10]. Later a 240 MHz low-pass-filter for an UWB receiver has been successfully realized in the G_m-C topology [11].

Another critical issue to baseband circuit design is DC-offset, which might lead to second-order distortions arising from the third-order nonlinearity in a balanced baseband circuit [12]. The third-order inter-modulation between the input signal and the DC-offset generates the second-order distortions. The propagation of the amplified second-order distortion from stage to stage in the baseband chain not only degrades signal-to-noise ratio

Manuscript received April 02, 2009; revised October 06, 2009. Current version published February 05, 2010. This paper was approved by Associate Editor Andreas Kaiser.

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Digital Object Identifier 10.1109/JSSC.2009.2036320

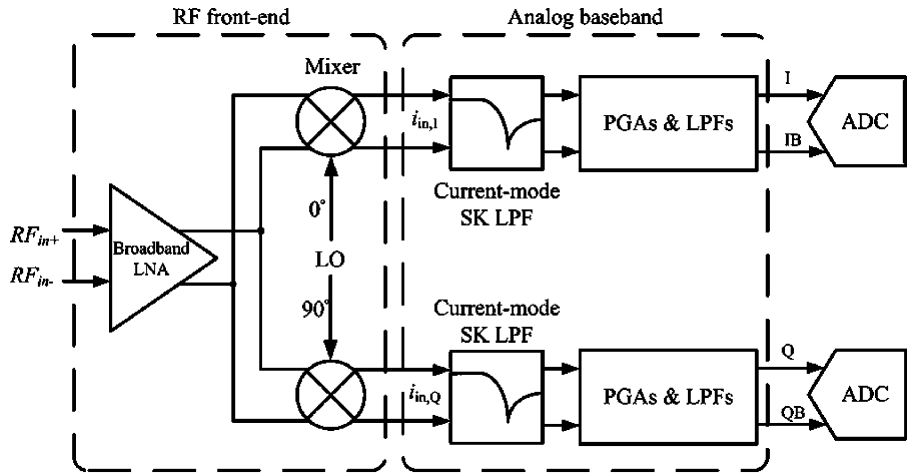

Fig. 1. Architecture of a direct-conversion RF receiver for UWB.

(SNR) but also saturates circuits. Calibration is required to improve this DC-offset related second-order nonlinearity.

In this paper, the analog baseband circuit is implemented by balanced current-mode amplifiers. Current-mode PGAs are combined with a 6th-order G_m-C low-pass filter to obtain a high gain, a high dynamic range and low noise. A current-mode Sallen-Key low-pass filter (SK LPF) is placed at the first stage to attenuate out-of-band interferers and relax linearity requirement of the following PGAs. Calibration circuits are also implemented to calibrate the corner-frequency of the G_m -C low-pass filter. DC-offset in the balanced circuits is resolved by a proposed digitally-assisted calibration loop. Compared to our previous publication [13], this paper focuses on the design concept of the UWB analog baseband. It is described in details why we process signals in the current domain, why we need a SK LPF instead of a single-pole filter and how we perform DC-offset calibration by digital assistance, as well as how to implement those functions in circuits. This paper is organized as follows. The baseband chain architecture and specifications are presented in Section II. Then, Section III describes in detail about the circuits of the UWB analog baseband chain. Finally, Section IV is dedicated to the measurement results of the baseband chain, in terms of frequency response, input-referred noise, linearity performance (IIP2, IIP3) and dynamic range of gain.

II. Baseband Chain Architecture and Specifications

Fig. 1 shows a direct-conversion RF receiver (DCR) for UWB. The receiver includes an RF front-end (a low noise amplifier and a down-conversion mixer) and an analog baseband (PGAs and LPFs). The MB-OFDM UWB signal is amplified and down-converted to the baseband with a bandwidth of 250 MHz. The strong out-of-band interferer is down-converted as well. To avoid saturating the analog-to-digital converter (ADC) due to the interferer, the baseband is required to pass signals and suppress interferers. As compared to narrowband systems, design challenge of the UWB analog baseband lies in high linearity and wide bandwidth to handle both signals and interferers.

Linearity restriction of the UWB RF receiver is at the output of the down-conversion mixer (input of the analog baseband). Large signal swing at the mixer output generates harmonics due to non-linearity of MOS transistors in the switching cells of the mixer and the input stage of the analog baseband. One way to reduce the signal swing without degrading SNR is to translate signals from the voltage domain to the current domain. To do so, a voltage-mode op amp can be configured as resistance feedback, forming low input impedance at the input of analog baseband. In addition, a capacitor can be parallel-connected with the feedback resistor to form a first-order low-pass filter to suppress out-of-band interferers. This method has already adopted in narrowband receiver design to achieve high linearity under a low supply voltage [14]. In this work, we further extend the method to a wideband RF receiver, such as a UWB RF receiver. First of all, it requires realizing low input impedance over the entire wide bandwidth. Second, we need current-mode filters. Wideband current-mode circuits have been developed for applications of optical wireline communications. Some design techniques can be borrowed here. For example, the active feedback technique helps to reduce input impedance of the amplifiers. Also filters constructed by current-domain circuits have been developed. Owing to WLAN 802.11a strong interferers are only 700 MHz away from MB-OFDM UWB 4.5 GHz channel, single-pole filter provides insufficient roll-off at 700 MHz away. The Sallen-Key filter has been applied to deeply filter specific harmonics in some applications [15]. In this work, we realize a Sallen–Key filter constructed by current-domain circuits to filter the strong interferers in current domain efficiently.

Here, the reference specifications of the analog baseband are addressed following to the receiver conformance requirement. The entire receiver must meet the required sensitivity and signal-to-noise radio (SNR) of -80.8 dBm and 9.3 dB, respectively, under the data rate of 53.3 Mb/s with the longest transmission distance of 10 m which leads to the most strict sensitivity requirement to the receiver [2]. The maximum received signal strength is -10 dBm. Hence, the dynamic range of the RF receiver is 70.8 dB. 10 dB of the required dynamic range is contributed by RF front-end, the remainder is taken into account in the analog baseband. Owing to the full-scale of

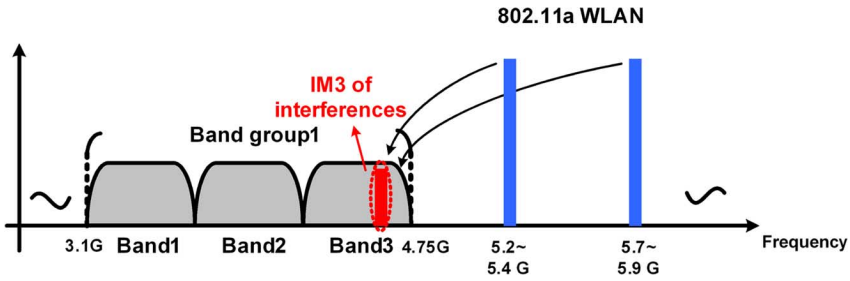

Fig. 2. Strong nearby interferers at 5 GHz (WLAN 802.11a) cause serious SNR degradation at 4.5 GHz channel.

TABLE I
SPECIFICATIONS OF ANALOG BASEBAND

Bandwidth	250 MHz
Gain Range	61 dB
Maximum gain	53 dB
Gain control resolution	1 dB
Noise Figure	14 dB
Out-of-band IIP3	-8 dBV
Out-of-band IIP2	-5 dBV

a UWB ADC is -14 dBV (200 $\mathrm{mV_p}$), the required maximum voltage gain of the RF receiver is 67.8 dB to amplify signals from the sensitivity level to the ADC full-scale with a back-off of the MB-OFDM UWB signal peak-average radio (PAR) as 9 dB. Given that the RF front-end voltage gain is fixed at 15 dB, the analog baseband shall provide the maximum voltage gain of 52.8 dB. The required sensitivity translates to the required receiver noise figure (NF) as 6.6 dB. Assume the RF front-end NF is a nominal value of 3 dB. Consequently the required noise figure of the analog baseband is less than 14 dB.

Linearity requirement for the RF receiver is constrained by the worst case that strong out-of-band interferers at the 5 GHz band (WLAN 802.11a) cause serious SNR degradation to the 4.5 GHz-channel as shown in Fig. 2 [16]. The test case defines two interferers allocated at 5.2 GHz and 5.85 GHz with the power level of -4 dBm. The required sensitivity is -75 dBm and the required SNR remains 9.3 dB [17]. Assume the pre-filter in front of the RF receiver provides 30 dB attenuation for out-of-band interferers. The required input-referred third-order intercept point (IIP3) of the RF receiver is -9 dBm. Therefore, the required out-of-band IIP3 of the analog baseband shall be over -8 dBV at the maximum gain setting. The interferers at 5.2 GHz and 5.85 GHz also could cause second-order inter-modulation distortion. To avoid degradation of SNR, the required IIP2 of the analog baseband should be better than -5 dBV as 10 dB attenuation of interferers is provided by the first stage of the analog baseband. According to the calculated specifications, Table I summarizes the baseband chain requirements to comply MB-OFDM UWB performance.

III. CIRCUIT DESIGN OF ANALOG BASEBAND CHAIN

As shown in Fig. 3, a proposed wideband, wide dynamic range baseband chain is composed in the order of three-stage current-mode PGAs, a $\mathrm{G_m}$-C filter, three-stage current-mode PGAs, an I-to-V converter and a voltage buffer. Besides, a digital-assisted DC-offset calibration loop is adopted to eliminate DC-offset of the baseband chain. The current-mode PGA is realized by balanced current-mode amplifiers to provide gain and gain tuning range. The first current-mode PGA also includes a current-mode SK LPF. Placed in the middle of the baseband chain, the $\mathrm{G_m}$-C filter filters out-of-band unwanted signals. The I-to-V converter is used to covert output current-domain signals of the current-mode PGAs to voltage-domain signals. Finally, a voltage buffer is designed for driving analog-to-digital converter (ADC).

In [11], the gain tuning function of the UWB low-pass filter is attained by controlling trans-conductance $(\mathrm{g_m})$ in the filter circuits, resulting in less gain, less gain tuning range and poor noise figure performance. In this design, the gain tuning function of the analog baseband is accomplished by the current-mode PGAs. The three-stage current-mode PGAs in front of the $\mathrm{G_m}$-C filter are designed with the gain of 47 dB to suppress $\mathrm{G_m}$-C filter noise. So the analog baseband exhibits much better noise figure performance than that reported in [11]. The three-stage current-mode PGAs follow the $\mathrm{G_m}$ -C filter to achieve the required overall gain and dynamic range. The analog baseband has gain tuning range from -9 dB to 73 dB, which leads to maximum gain of 73 dB and the dynamic range of 82 dB with gain resolution of 0.5 dB. The corner frequency of the baseband chain, determined by the $\mathrm{G_m}$-C filter and adjusted by the capacitors arrays, ranges from 250 MHz to 300 MHz. A $\mathrm{G_m}$-C calibration circuit is also integrated to tune the capacitors arrays against PVT variation.

A. Programmable Gain Amplifiers (PGAs)

Ideally the current amplifier should have infinite output impedance and zero input impedance for optimal current signal transfer. But in the advance CMOS process, drain-source

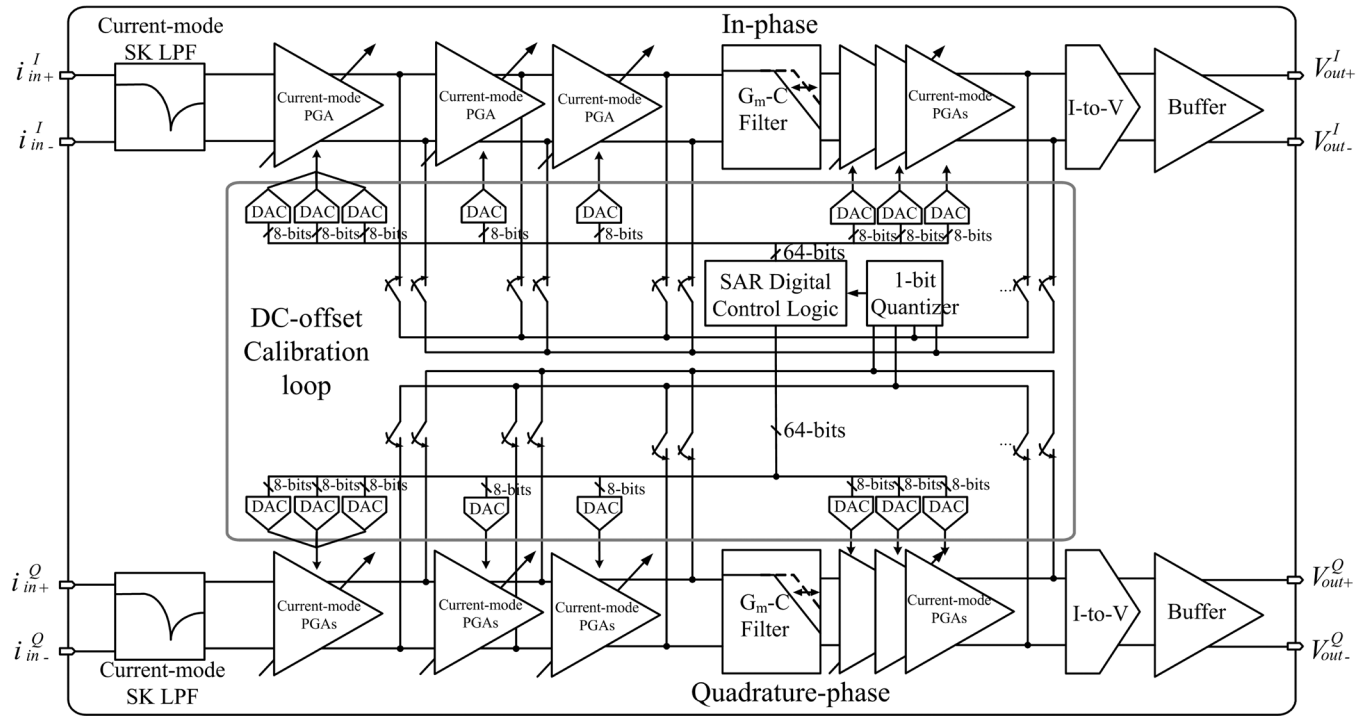

Fig. 3. Block diagram of the wideband, wide dynamic range baseband chain.

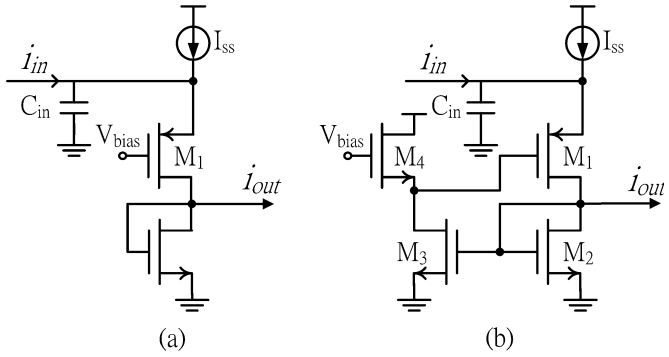

Fig. 4. (a) Conventional CG current amplifier. (b) Proposed current amplifier with series-series feedback.

$(\mathrm{R_{ds}})$ resistance is greatly decreased. Cascode topology for increasing output impedance cannot be easily realized due to the headroom limitation under a low supply voltage. Circuit design effort is therefore on very low input impedance.

PGAs are constructed by the current amplifier in the simple common-gate (CG) configuration, as shown in Fig. 4(a), exhibiting an input resistance of $1/\mathrm{g_{m1}}$. Low input impedance indicates a large-size transistor and high bias current, and in turn, leads to large input capacitance and high input-referred noise from the tail current source [18]. As shown in Fig. 4(b), a series-series feedback loop through M3 and M4 is added to decrease the input resistance without degrading bandwidth and noise performance. The input impedance of the current amplifier with the feedback is derived as (1), where $C_1 = C_{gs4} + C_{ds4} + C_{ds3}, C_2 = C_{gs2} + C_{ds2} + C_{gs3}$. At low frequencies, the input resistance can be reduced to

$$Z_{\mathrm{in,DC}} = \frac{1}{g_{m1}} \cdot \left(1 - \frac{g_{m1}}{g_{m4}} \cdot \frac{g_{m3}}{g_{m2}}\right) \tag{2}$$

The input-impedance is reduced by a factor of $1 - g_{m1} \cdot g_{m3}/(g_{m4} \cdot g_{m2})$ due to the series-series feedback.

The complete schematic of the differential PGA is shown in Fig. 5. The input stage is accomplished by the series-series feedback for low input impedance. The bandwidth of the feedback must be large enough across the entire channel band (250 MHz in this case since direct conversion is used). As shown in Fig. 6, the simulated input impedance exhibits a low value of 15 ohm up to 1 GHz. The PGA load is composed of current mirrors in the cascode configuration for high output impedance. Current gain is programmable by changing the size ratio of the current mirror load using switches to turn on or off the cascode stage. Therefore, current consumption of the PGA is proportional to its gain. For linearity concern, DC bias current is designed in class-A operation. As to the output DC voltage, it is defined by

$$Z_{\mathrm{in}} = \frac{1}{g_{m1}} \cdot \frac{s^2 C_1 C_2 + s(C_1 g_{m2} + C_2 g_{m4}) + (g_{m4} \cdot g_{m2} - g_{m1} \cdot g_{m3})}{s^3 \frac{C_1 \cdot C_2 \cdot C_{\mathrm{in}}}{g_{m1}} + s^2 \left[C_1 C_2 + \frac{C_{\mathrm{in}}}{g_{m1}}(C_1 g_{m2} + C_2 g_{m4})\right] + s\left[C_1 g_{m2} + C_2 g_{m4} + \frac{C_{\mathrm{in}}}{g_{m1}}(g_{m4} g_{m2} - g_{m1} g_{m3})\right] + g_{m4} \cdot g_{m2}} \tag{1}$$

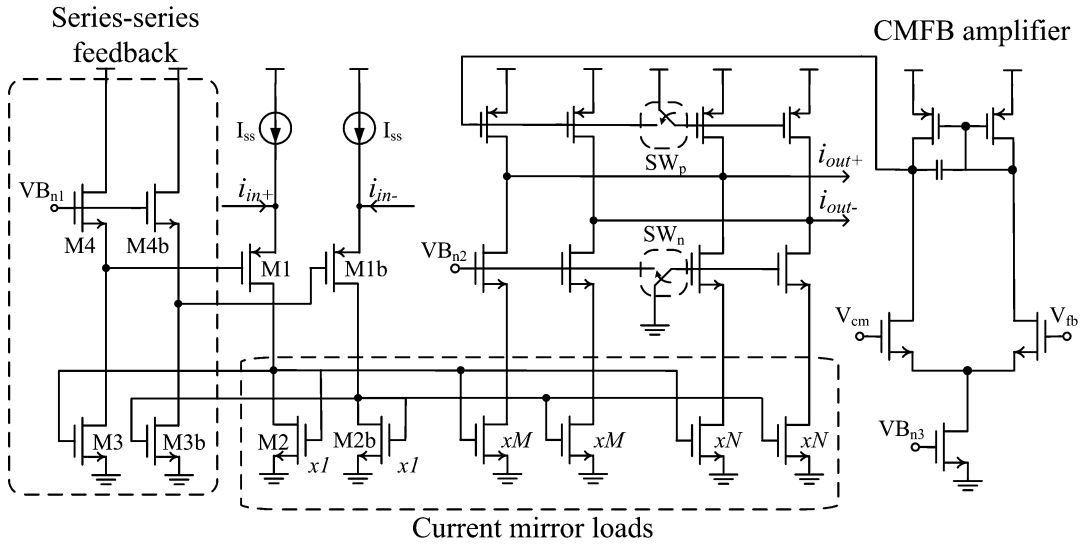

Fig. 5. The schematic of PGA based on current amplifier.

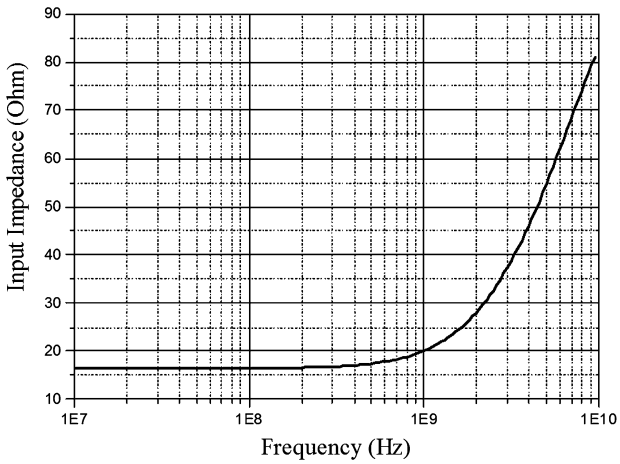

Fig. 6. Simulated input impedance of PGA.

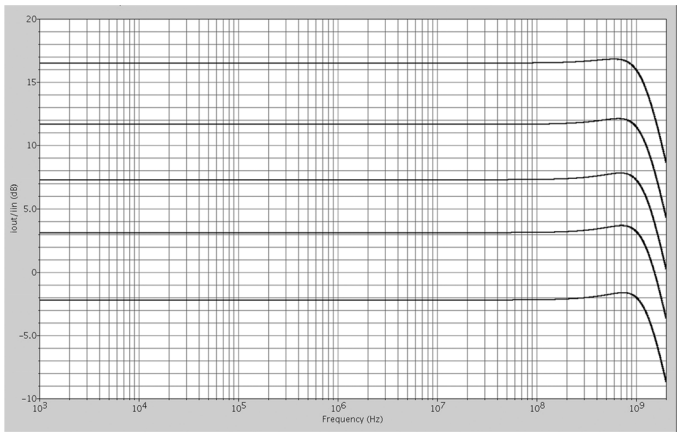

Fig. 7. The frequency response of the PGA over different gain settings.

a common-mode feedback (CMFB) amplifier and matched to the input DC voltage of the next PGA stage. Fig. 7 shows the frequency response of the PGA over different gain settings.

As shown in Fig. 5, owing to high source impedance, noise contributed by M1 and the series-series feedback circuit (M3-M4) of the PGA can be neglected. The input-referred noise current of the PGA depends critically on the trans-conductance of M2 and current source $(\mathrm{I_{ss}})$, as indicated in the following equation:

$$\overline{i}^2_{n,\mathrm{in}} = 4kT \cdot \gamma \cdot (g_{m2} + g_{\mathrm{mss}}). \tag{3}$$

As $\mathrm{g_{m2}} = 12$ mS and $\mathrm{g_{mss}} = 5.77$ mS, the PGA exhibits a low input-referred noise current of 42.5 pA/$\sqrt{\ }$Hz. Simulated by SpectreRF, noise analysis shows that the input-referred noise of the analog baseband is dominated by the current noise of the first two PGAs and governed by (3). Circuit noise after the first two PGAs is greatly suppressed by the high gain of the first two PGAs.

In the first stage of the PGAs, the current-mode SK LPF is implemented for filtering the interferers from WLAN 802.11a signals [19], [20]. The schematic is similar to the current amplifier except the resistor-capacitor feedback at the output as shown in Fig. 8. Therefore, the inter-modulation term due to the interferers is greatly reduced, which leads to relaxed linearity requirement to the following PGAs. The equivalent circuit model of the current-mode SK LPF is shown in Fig. 9. The transfer function of the current gain can be derived as (4), where F is the current gain of the current amplifier and r_i is the non-zero input resistance of the current amplifier. Composed by a complex-conjugate pair, the zeros in (4) form a transmission zero

$$H(s) = \frac{i_{\mathrm{out}}(s)}{i_{\mathrm{in}}(s)} = \frac{s^2 C_1 C_2 R_1 r_i + s C_2 r_i - F}{s^2[C_1 C_2 (R_1 R_2 + r_i(R_1 + R_2))] + s\{C_1(R_1 + R_2) + C_2[R_i + R_2(1 + F)]\} + 1} \tag{4}$$

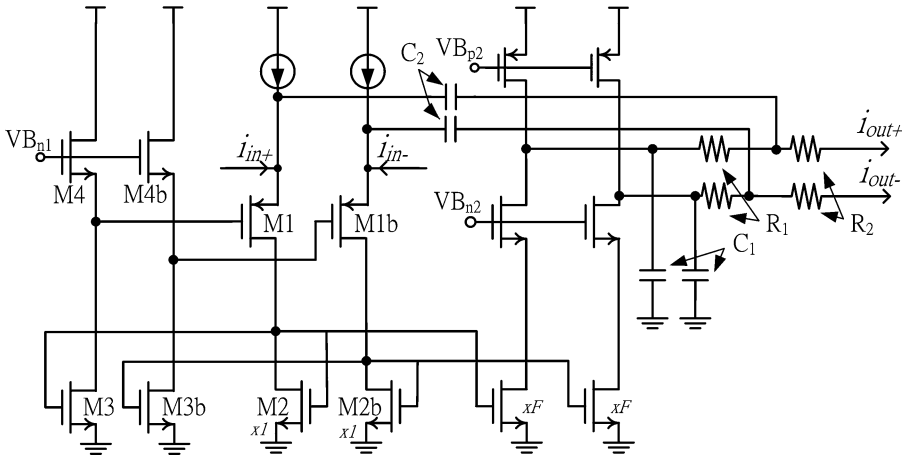

Fig. 8. The schematic of current-mode SK LPF.

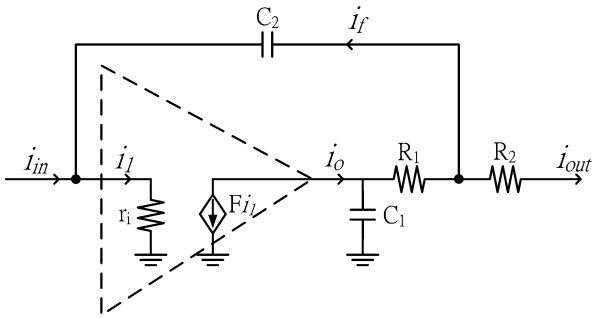

Fig. 9. Equivalent circuit model of the current-mode SK LPF.

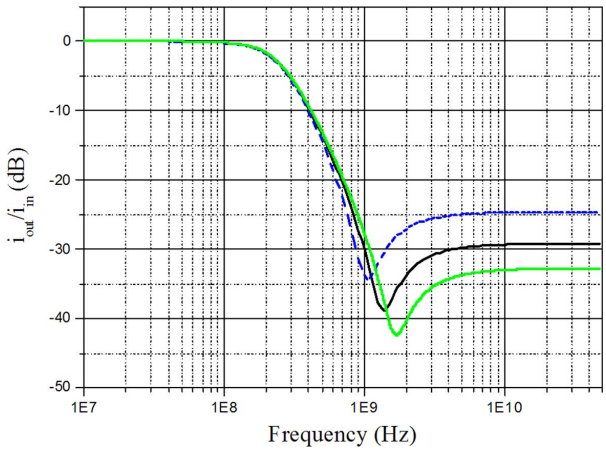

Fig. 10. Frequency response of the current-mode SK LPF.

and make a notch in the frequency response. By assuming that the zeros are located at $s = -a \pm jb$, we can write the numerator of (4) in the form of

$$H_{\mathrm{num}}(s) = s^2 + 2as + (a^2 + b^2). \tag{5}$$

The notch frequency $(\mathrm{w_t})$ satisfies the following equation:

$$\frac{d(|H_{\mathrm{num}}(s)|)}{ds}\Big|_{s=w_t} = 0\ . \tag{6}$$

Substituting (5) into (6), we obtain the notch frequency as:

$$w_t = \sqrt{b^2 - a^2}. \tag{7}$$

Assume $C_1 = C, C_2 = \alpha C, R_1 = R, R_2 = \lambda R, r_i = \beta R$ and $\mathrm{F} = -1$. Equation (4) can be rewritten as (8). Solving a and b by using (5) and numerator of (8), notch frequency $(\mathrm{w_t})$ and quality factor $(\mathrm{Q_z})$ can be expressed by the filter parameters $(\mathrm{RC}, \alpha, \beta$ and $\lambda)$ as follows:

$$w_t = \frac{1}{\mathrm{RC}}\sqrt{\frac{1}{\alpha\beta} - \frac{1}{2}} \tag{9}$$

$$Q_z = \sqrt{\frac{1}{\alpha\beta}}. \tag{10}$$

Besides, pole frequency $(\mathrm{w_p})$ and quality factor $(\mathrm{Q_p})$ of the denominator of (8) can be derived as follows:

$$w_p = \frac{1}{\mathrm{RC}}\sqrt{\frac{1}{\alpha(\lambda + \beta + \beta\lambda)}} \tag{11}$$

$$Q_p = \frac{\sqrt{\alpha(\lambda + \beta + \beta\lambda)}}{1 + \lambda + \alpha\beta}. \tag{12}$$

Finally, we can obtain the filter parameters (RC, α, β and λ) by solving (9), (10), (11) and (12).

Consider the worst case that the UWB channel of band 3 (frequency centered at 4.5 GHz) is used. The WLAN 802.11a interferer in the RF band of 5.7 GHz–5.9 GHz will be down-converted to the baseband frequency of 1.2 GHz–1.4 GHz by the receiver. The notch of the SK LPF can be designed in the frequency of 1.2 GHz–1.4 GHz to filter the interference signals.

$$H(s) = \frac{i_{\mathrm{out}}(s)}{i_{\mathrm{in}}(s)} = \frac{\alpha\beta}{\alpha(\lambda + \beta + \beta\lambda)} \times \frac{\mathrm{s}^2 + \frac{1}{\mathrm{RC}}s + \frac{1}{\alpha\beta(\mathrm{RC})^2}}{\mathrm{s}^2 + \frac{1+\lambda+\alpha\beta}{\alpha(\lambda+\beta+\beta\lambda)}s + \frac{1}{\alpha(\lambda+\beta+\beta\lambda)(\mathrm{RC})^2}} \tag{8}$$

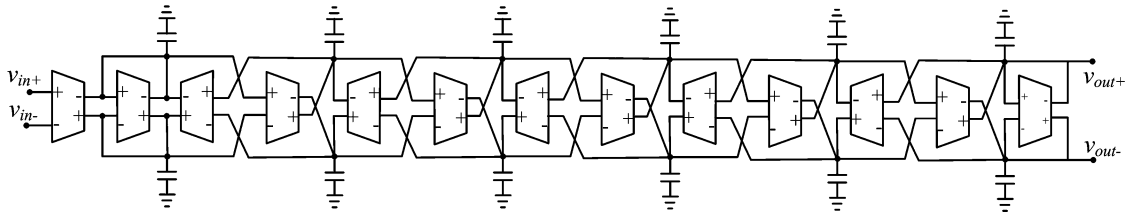

Fig. 11. The 6th-order G_m-C filter.

Actually another WLAN 802.11a interfere in the RF band of 5.2 GHz–5.4 GHz is down-converted to the baseband frequency of 0.7–0.9 GHz, closer to the signal band. Yet choosing the notch in 1.2–1.4 GHz causes less in-band signal degradation while reducing the same amount of baseband inter-modulation distortion due to these two interferers. Therefore, the inter-modulation term falls into band 3 caused by WLAN 802.11a signals in 5.2 GHz–5.4 GHz and in 5.7 GHz–5.9 GHz can be greatly reduced. Thus, we design the notch frequency (W_t) of the current-mode SK LPF at 1.3 GHz (middle frequency of 1.2 GHz–1.4 GHz) and the pole frequency (W_p) at 250 MHz (bandwidth of the channel). Furthermore, let Q_z and Q_p to be 3 and 0.707, respectively. Assume C_1 is 1 pF, we can have the following filter parameters from (9)–(12):

$$\alpha = 2.0637$$
$$\beta = 0.0538$$
$$\lambda = 1.4116$$
$$RC = 3.5693 \times 10^{-10}$$

The simulated frequency response of the current-mode SK LPF is shown in Fig. 10. In the circuit design, the capacitors (C_1 and C_2) and resistors (R_1 and R_2) in the SK LPF are designed in a binary-weighted array and can be tuned by a 3-wire control interface to cover PVT variations. As shown in Fig. 10, by tuning the passive components (C_1, C_2, R_1 and R_2), the notch frequency of the current-mode SK LPF can be designed at 1.2 GHz, 1.3 GHz and 1.4 GHz, respectively.

B. G_m-C Filter

The G_m-C filter utilizes the *LC* ladder structure to accomplish the 6th-order Chebyshev low-pass filter as shown in Fig. 11. The schematic of the G_m cell is as shown in Fig. 12. The super source follower structure as in [21] is applied to improve the linearity of the G_m cells. Regulated by the gain-bandwidth product limit, the G_m-C filter is therefore designed with no gain to extend its bandwidth to 250 MHz. However, the PVT process variation might cause bandwidth change significantly. G_m-C calibration circuit is necessary to reduce impact on the cutoff frequency of the channel selection filter.

Calibration circuits are integrated to tune the capacitors arrays against the variation. The main issue is accurate implementation of the time constant (G_m/C). In [22], the time constant is tuned automatically by varying G_m. The analog-type tuning method is sensitive to noise and consumes much power. Instead, digital-type control of passive component C is chosen.

Fig. 13 shows the architecture of the G_m-C calibration loop adopted in this design. The G_m -C calibration loop consists of a

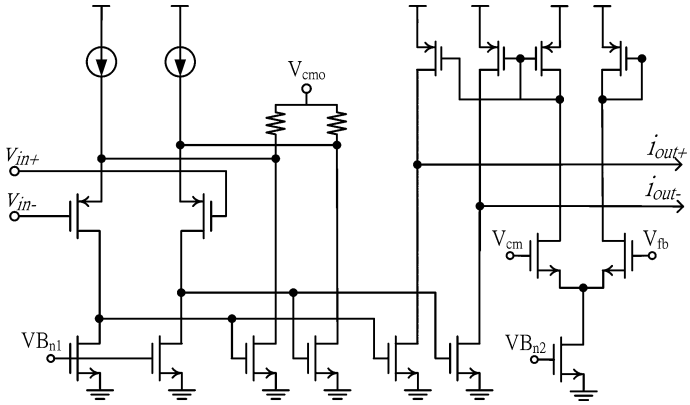

Fig. 12. The schematic of G_m cell in G_m -C filter.

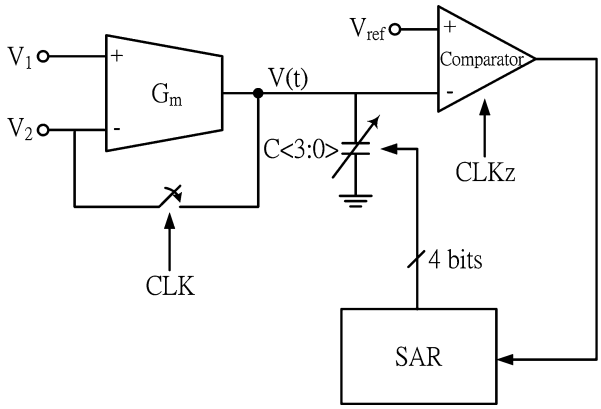

Fig. 13. The architecture of G_m-C calibration loop.

G_m cell, a capacitor array, a comparator and a digital controller. The G_m cell and the capacitor array are identically matched to those used in the filter chain. An accurate reference clock signal is used to control a MOS switch between DC voltage source (V_2) and the G_m cell output to decide the charging time of the capacitor array. The G_m cell output voltage (V(t)) is compared to a reference voltage (V_{ref}) corresponding to the desired G_m/C time constant. By the algorithm of successive approximation (SAR) search, the digital controller controls the capacitor array to an appropriate setting according to the comparator output result. In this control loop, the output voltage of the G_m cell in the time domain is governed by

$$V(t) = \int_0^t e^{-\frac{1}{\frac{g_m}{C}(V_1 - V_2)}t} dt + V_2. \tag{13}$$

Fig. 14 shows an example of the timing diagram of CLK, CLKz and V(t) during the calibration. Initially, the capacitor

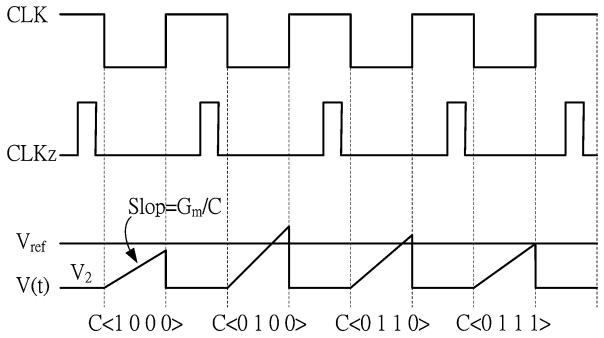

Fig. 14. Timing diagram of G_m-C calibration.

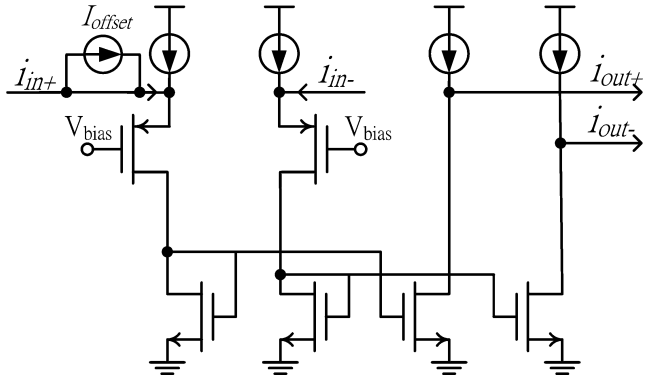

Fig. 15. A typical balanced current amplifier with an input referred DC-offset current.

array is set as $\langle 1\,0\,0\,0\rangle$, CLK is high, and V(t) is charged to V_2. When CLK becomes low, V(t) is further charged with the time constant of G_m/C as indicated in (13). If C is too small, V(t) is eventually higher than V_{ref} as CLK turns from low to high, or vice versa. It takes four clock cycles for the digital controller to process SAR search to set the capacitor array to the appropriate result. Consequently, the capacitor array is calibrated to achieve the desired G_m/C time constant.

C. DC-Offset Calibration

The issues of balanced current amplifiers are poor IP2 performance owing to DC-offset in the circuits. As shown in Fig. 15, a typical balanced current amplifier is with an input-referred DC-offset current, I_{offset}. Therefore, the received input currents $i_{\text{in}+}$ and $i_{\text{in}-}$ to the amplifier can be described as

$$i_{\text{in}+} = I_{\text{offset}} + A\cdot\cos(wt), i_{\text{in}-} = A\cdot\cos(wt+180^\circ) \quad (14)$$

Circuit non-linearity will lead to output current, i_{out} as

$$i_{\text{out}} = a + b\cdot i_{\text{in}} + c\cdot i_{\text{in}}^2 + d\cdot i_{\text{in}}^3 + \cdots \quad (15)$$

The balanced output of the current amplifier can be derived as

$$i_{\text{out}+} - i_{\text{out}-} = \cdots d\cdot 3\cdot I_{\text{offset}}\cdot A^2\cdot(1+\cos(2wt))+\cdots \quad (16)$$

It indicates that DC-offset current results in the second-order distortion at the output of the balanced current amplifier. Consequently it is uncommon in literature that cascading current amplifiers for high-gain and wide dynamic range applications. Another second-order linearity issue is poor IP2 performance due to absence of common current biasing for the balanced branches in typical circuit implementation. In [23], a digital calibration scheme had been proposed for calibrating IIP2 of a down-conversion mixer. Here, the critical second-order distortion issue in the analog baseband is tackled by using a digitally-assisted DC-offset calibration. The digital technique benefits in circuits and substrate noise immunity, low power consumption and fast settling time.

As shown in Fig. 3, the digitally-assisted DC-offset calibration consists of a 1-bit quantizer, one digital control logic unit and digital-to-analog converters (DACs). DC-offset current in the current-mode PGA is converted to DC-offset voltage at the PGA output by the equivalent output resistance. Therefore, DC-offset of balanced branches in the PGA can be sensed by a voltage-mode 1-bit quantizer as shown in Fig. 16. The 1-bit quantizer is composed of an auto-zeroing amplifier and a latch. The auto-zeroing amplifier eliminates its own DC-offset in half of a clock period and then amplifies the DC-offset of balanced branches in another half of a clock period. The latch converts the output of the auto-zeroing amplifier into a 1-bit digital code. To save the time consumed by the DC-offset calibration, the auto-zeroing amplifier and the latch work as a pipeline in time domain. That is, as the latch works, the auto-zeroing amplifier performs self DC-offset elimination to prepare for sampling next incoming DC-offset.

The DC-offset calibration range and resolution are dependent on number of bits and LSB current of DAC, respectively. An 8-bit balanced DAC based on a current-steering structure is connected to the balanced branches of the PGA. The schematic of the DAC is shown in Fig. 17. The DAC steals current from PGA to eliminate DC-offset of its balanced branches. Initially, the DAC is set in the middle code as $\langle 1,0,0,0,0,0,0,0\rangle$, which leads to steal one more LSB current from one of balanced branches of PGA. The digital control logic performs successive approximation (SAR) search to set the DAC according to the output of the 1-bit quantizer.

Fig. 18 shows an example of the DC-offset calibration procedure. Initially, the DAC is set as $\langle 1,0,0,0,0,0,0,0\rangle$. Then, the output of the 1-bit quantizer is '0', which means output DC at the '$-$' branch of PGA is higher than that of the '$+$' branch. For eliminating the DC-offset, by SAR method, the DAC is re-set as $\langle 0,1,0,0,0,0,0,0\rangle$ by the digital control logic unit. This means that the DAC steals more current from the '$-$' branch of PGA (less current from the '$+$' branch of PGA). After that, the output of the 1-bit quantizer becomes '1', which means output DC at the '$-$' branch of PGA is lower than that of the '$+$' branch. Then, the DAC is re-set as $\langle 0,1,1,0,0,0,0,0\rangle$ by the digital control logic unit to steal more current from the '+' branch of PGA, and so on. After the eight bits of DAC are set, the DC-offset of the PGA is calibrated to the minimum DC-offset limited by the LSB current of DAC, which consumes time of eight clock cycles. As the reference clock of 33 MHz is used, the time consumed by calibrating DC-offset of one stage of PGAs only needs 0.25 μs.

In the analog baseband, the DC-offset calibration is performed in PGAs which amplify DC-offset and second-order nonlinearity. However, the 6th-order Chebyshev low-pass filter designed with no gain does not need to calibrate its DC-offset.

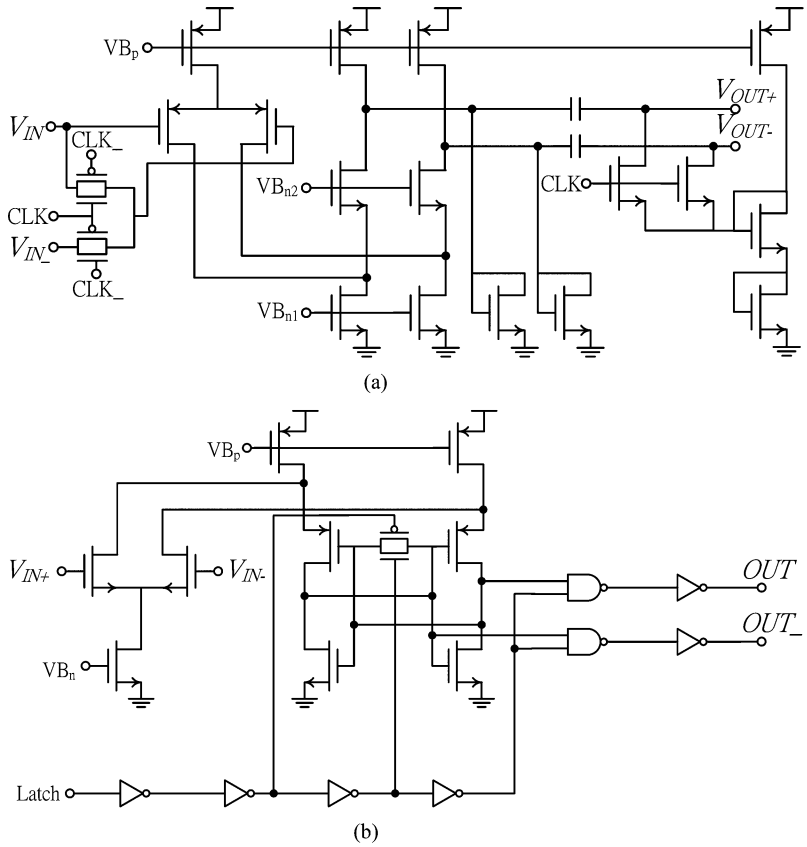

Fig. 16. The schematic of 1-bit quantizer. (a) Auto-zeroing amplifier. (b) Latch.

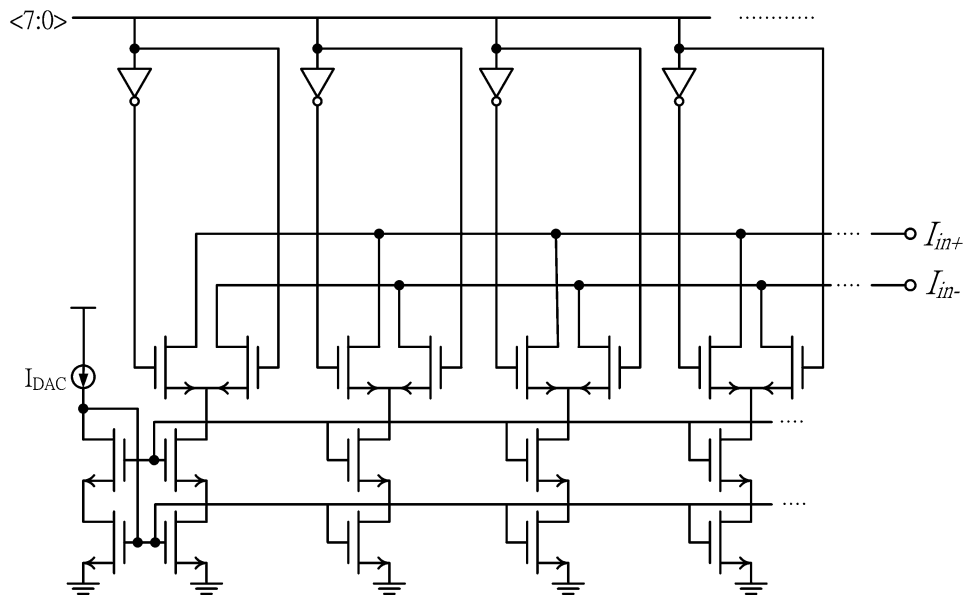

Fig. 17. The schematic of 8-bits differential DAC.

The DC-offset calibration carries out by starting from the first PGA stage of the analog baseband and ending at the last PGA stage. Initially, the DC-offset calibration is performed as the receiver is power-on and before receiving the first symbol of data. Due to DC-offset varies with temperature, DC-offset calibration needs to be re-executed in the time slot of transmission (transmitter is working and receiver is idle) as obvious temperature variation is detected.

In MB-OFDM UWB, fast frequency hopping is adopted within three bands in a band group to interleave interference in time domain. Changing LO frequency will lead to DC-offset variation in the input of analog baseband, which needs individual DAC to recode DC-offset corresponding to different LO frequency. Therefore, as shown in Fig. 3, there are three DACs used in the first stage of the analog baseband. As frequency hopping, the DAC corresponded to the frequency channel is

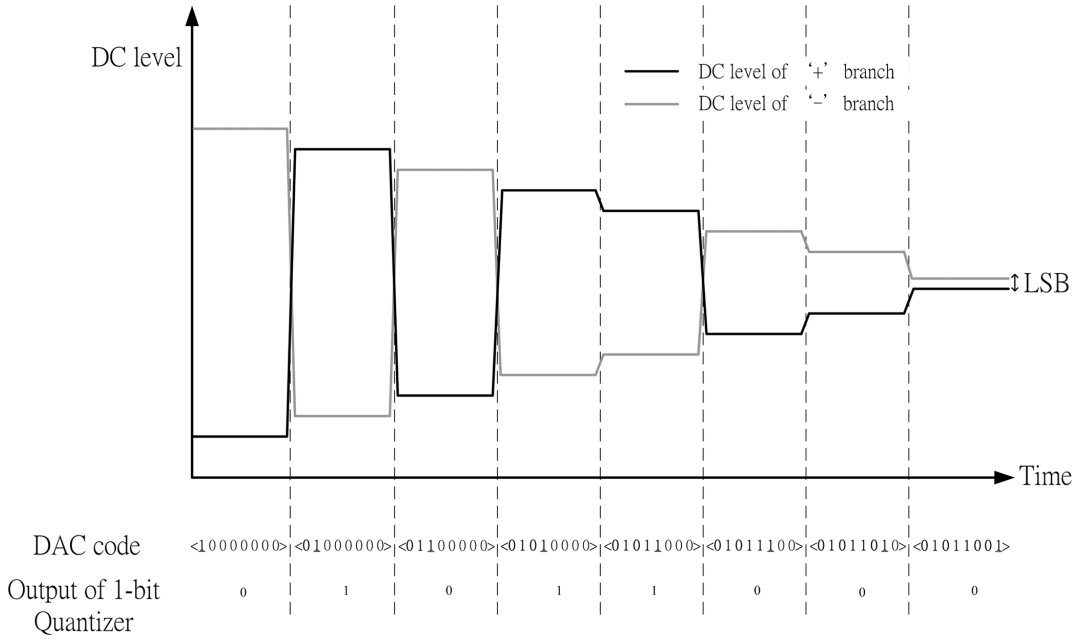

Fig. 18. An example of the successive approximation (SAR) DC-offset calibration.

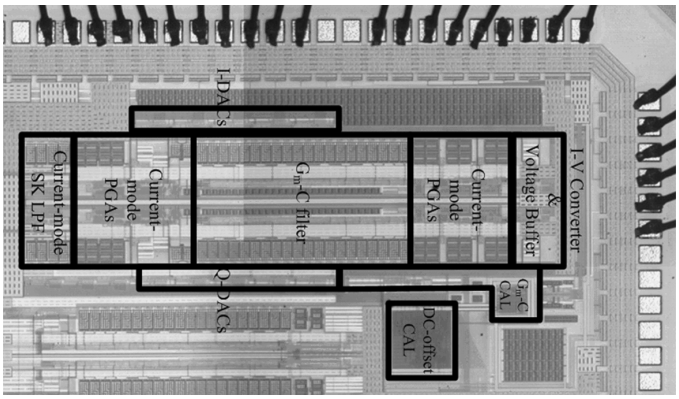

Fig. 19. Die photo of the baseband chain in 0.13 μm CMOS technology. The baseband chain comprises SK LPF, current-mode PGAs, 6th-order Chebyshev G_m-C filter and circuitry for G_m-C and DC-offset calibration.

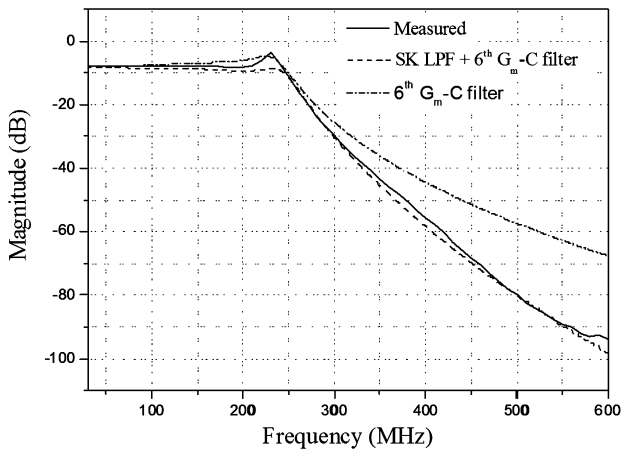

Fig. 20. Measured and simulated frequency response of the baseband chain.

switched for compensating the DC-offset. Frequency hopping is required to be performed within 9.5 ns in MB-OFDM UWB. The switching time between DACs can fulfill the strict requirement. Every PGA stage unless the first PGA uses one DAC for recoding results of DC-offset calibration. Totally, 16 DACs are used for calibrating two-phase (I-phase and Q-phase) of the analog baseband. Therefore, the calibration procedure can be completed within 4 μs.

IV. Measurement Result

The baseband chain has been implemented in a 1.2 V 0.13 μm CMOS technology. The chip micrograph is shown in Fig. 19. It is embedded in a RF transceiver and occupies 0.8 mm^2. Fig. 20 shows the measured frequency response of the analog baseband with comparing to the simulated frequency response of the 6th G_m-C filter and the analog baseband (SK LPF+6 th G_m-C filter). The measured pass-band edge frequency is 250 MHz with 1 pF of probe capacitance. As shown in Fig. 21, measured out-band IIP3 (f1 $=$ 400 MHz, f2 $=$ 790 MHz) of the filter is

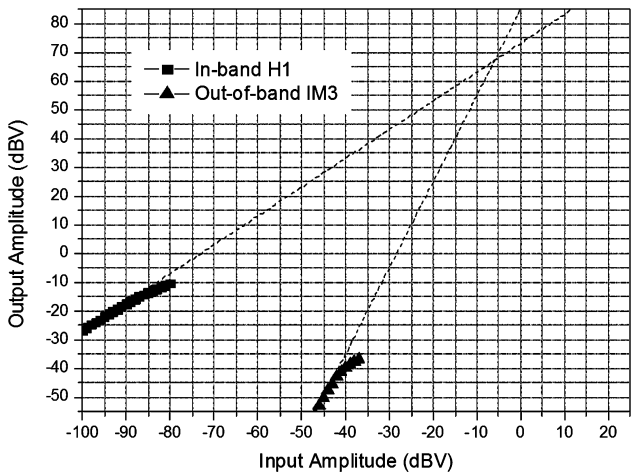

Fig. 21. Measured out-band IIP3 (f1 $=$ 400 MHz, f2 $=$ 790 MHz) of the baseband chain under voltage gain of 73 dB and pass-band edge frequency of 250 MHz.

TABLE II
PERFORMANCE SUMMARY OF THE BASEBAND CHAIN AND COMPARISON TO [11]

	[11]	This work	
Technology	0.13μm CMOS	0.13μm CMOS	
Supply Voltage	1.2V	1.2V	
Filter order	5	6	
Passband edge frequency	240MHz	250~300MHz	
Voltage Gain at 10MHz	12.9~47.6dB	-9~73dB	
Gain Resolution (dB)	N.A.	0.5	
Input-referred noise figure	7.7nV/√Hz (43.4dB)	1.42 nV/√Hz (14dB)	
In-band IIP3 (f1=30MHz, f2=50MHz)	-48.2dBV (under gain of 47.6dB)	-71dBV (under gain of 73dB)	
Out-band IIP3 (f1=400MHz, f2=790MHz)	-8.2dBV (under gain of 47.6dB)	-6dBV (under gain of 73dB)	
In-band IIP2 (f1=40MHz, f2=50MHz)	N.A.	-59dBV (under gain of 68dB)	
Out-band IIP2 (f1=400MHz, f2=410MHz)	+18.2dBV (under gain of 47.6dB)	-5dBV (under gain of 68dB)	
Power consumption	24mW	Core	56.4mW
		DACs for DC-offset calibration	3.6mW
FOM (maximum gain/power consumption)	10 /mW	79.2 /mW	

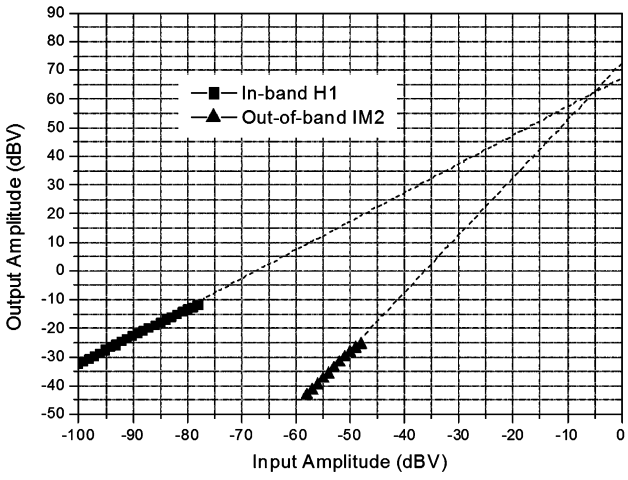

Fig. 22. Measured out-band IIP2 (f1 = 400 MHz, f2 = 410 MHz) of the baseband chain under voltage gain of 68 dB and pass-band edge frequency of 250 MHz.

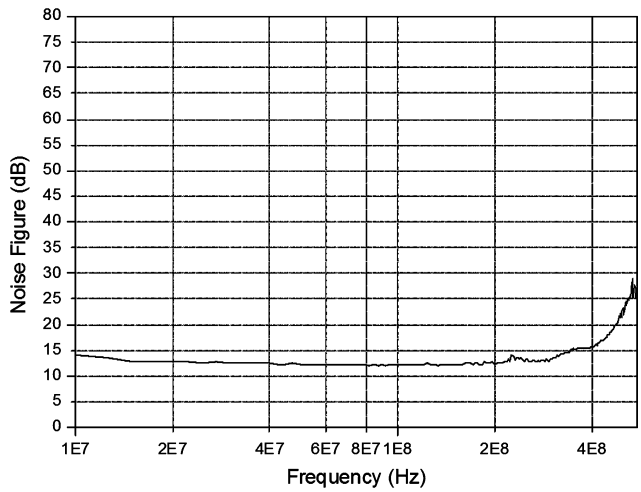

Fig. 23. Measurement noise figure of the baseband chain under voltage gain of 73 dB and pass-band edge frequency of 300 MHz.

−6 dBV under voltage gain of 73 dB and pass-band edge frequency of 250 MHz. The high linearity performance is achieved under 1.2 V supply by the current-mode PGAs and the proposed current-mode SK LPF. Measured in-band IIP2 (f1 = 40 MHz, f2 = 50 MHz) of the filter is −59 dBV under voltage gain of 68 dB and pass-band edge frequency of 250 MHz. The measured out-of-band IIP2 (f1 = 400 MHz, f2 = 410 MHz) is −5 dBV under the voltage gain of 68 dB and the pass-band edge frequency of 250 MHz (Fig. 22). Therefore, the issue of current amplifiers indicated by poor HD2 performance is improved by the proposed architecture and the DC-offset calibration. The measured Noise Figure (Fig. 23) is 12–14 dB within the BW at the maximum gain setting of 73 dB. Performance summary and comparison to [11] are listed in Table II.

V. Conclusion

An analog baseband chain with features of wide-bandwidth and wide dynamic range of gain, as well as low noise and high linearity for UWB has been presented. Current-mode PGA gives excellent noise figure and IIP3 performance. Digital-assisted DC offset calibration solves the problem of poor IP2 performance associated with DC offset of the current-mode PGA. A current-mode SK LPF is used to suppress out-of-band interferers efficiently. The chip occupies 0.8 mm^2 and consumes 56.4 mA in a 1.2 V 0.13 μm CMOS process. The bandwidth of the current-mode PGA and G_m-C filter can be further extended by using nanometer CMOS process. This work demonstrates a realization of a baseband chain applied for wideband communication systems.

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