The Role of Resist for Ultrathin Gate Oxide Degradation During O_2 Plasma Ashing

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Abstract— **During ashing process, resist has been intuitively regarded as a protection layer and deliberately removed in previous studies by wet process prior to plasma exposure in an effort to amplify the damage effect. Recently, we found instead that resist does not simply act as a protection layer. This newly observed phenomenon cannot be explained by the well-known electron shading effect which should not affect the area-intensive antenna structure used in our study. In this letter, we hypothesize that this resist-related charging damage is determined by the plasma potential adjustment difference between those devices with and without resist overlayer. The experimental results show a good correlation with our explanation. To be specific, severe antenna area ratio (ARR) dependent degradation of thin gate oxide is induced during the initial ashing stage while the resist is still on the electrodes, not during the overashing period.**

I. Introduction

The role of resist has seldom been noticed during plasma ashing damage on thin oxides [1]–[4]. Previously resist was regarded only as a protection layer, and fully exposed thin oxides during overetching period were expected to suffer more severe charging degradation from plasma. Recently we showed that, contrary to previous belief, the presence of resist instead causes even more severe damage during plasma charging [5]. In this letter, we show that the resist indeed participates in plasma charging and plays an important role on plasma ashing damage of ultrathin oxides. Severe damage occurs during the stage while the resist still exists on the antenna electrodes. It is qualitatively explained by the well-known self-surface-potential adjustment behavior [6] and a simple equivalent capacitor circuit model [7]. Good agreement is obtained between the observed results and the proposed model.

II. Experiments

MOS capacitors were fabricated on 6-in p-type (100) 15–25 Ω-cm silicon wafers. Active regions with area of $20 \times 20\ \mu m^2$ were defined by LOCOS isolation with field oxide thickness of 500 nm. Ultrathin gate oxides were grown in dry oxygen ambient at 900 °C, followed by polysilicon deposition at 620 °C and $POCl_3$-doping at 950 °C. After polygate definition, a 0.5-μm TEOS oxide was deposited for dielectric passivation. Finally, antenna structures were defined by wet etching after 1-μm thick aluminum film deposition. The area-intensive antenna test structures were used and antenna area ratios (ARR $= A_f/A_g$) were varied from 16 to 10^4. A commercial O_2/CH_3OH down-stream plasma resist asher was used to evaluate the damage on the thin oxides. The ashing process was operated at 13.56 MHz, 1.5 torr, and 800 W. The total processing time was 160 s, while the substrate was maintained at 200 °C. Devices received a 400 °C post-metal-anneal (PMA) for 30 min before constant current stress testing.

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III. Results and Discussion

The configuration of our down-stream asher is similar to that reported in [3]. Since the gas is injected from the radial center at the top portion of the chamber, the generated plasma is more intense at the central region and spatial plasma potential distribution will curve upward [3]. The authors predicted that nonuniform plasma would dictate a nonuniform floating potential on the wafer surface and lead to a net electron current flowing through thin oxides at the wafer central region, which will tunnel out from the wafer edge back to the plasma [3], [4].

Fig. 1 shows the distribution of charge-to-breakdown across the wafer for devices with or without resist overlayer on the antenna electrodes. Thin gate oxide with 4.2 nm in thickness and antenna area ratios (ARR) varying from 16 to 10^4 are employed to clarify charging damage. It is intuitively expected that devices with resist protection will suffer less degradation from plasma [1]–[3]. This prediction, however, contradicts with the experimental observation, which become more observable for ultrathin oxides [5]. Devices with resist covering suffer severe antenna degradation at the wafer center while those without resist overlayer do not. Our results indicate that only minor degradation (i.e., 1 C/cm^2 at 25 °C and 0.02 C/cm^2 at 200 °C) is observed for the nonresist-covered devices even with a 10^4 ARR and 4.2-nm oxide. These imply that uniform plasma in our machine can be expected from the charging model in [3]. However, resist is known as an insulator [7]. Even if charging current will tunnel through thin resist toward the endpoint, devices with resist overlayer should not suffer more damage than those without resist covering.

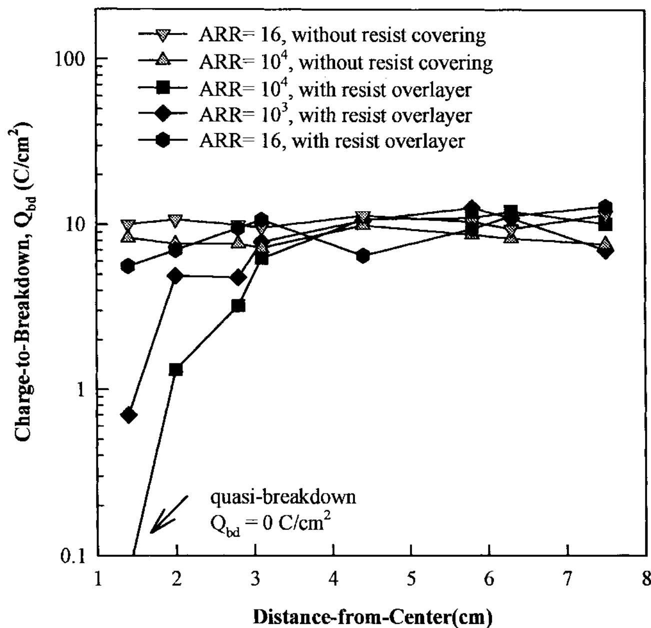

Fig. 1. The radial distribution of charge-to-breakdown across the wafer for devices with and without resist covering. Ultrathin oxide thickness is 4.2 nm and the stress current is -200 mA/cm^2, i.e., gate injection at 25 °C. Quasi-breakdown is defined as a failure due to high leakage current level at low voltage [8].

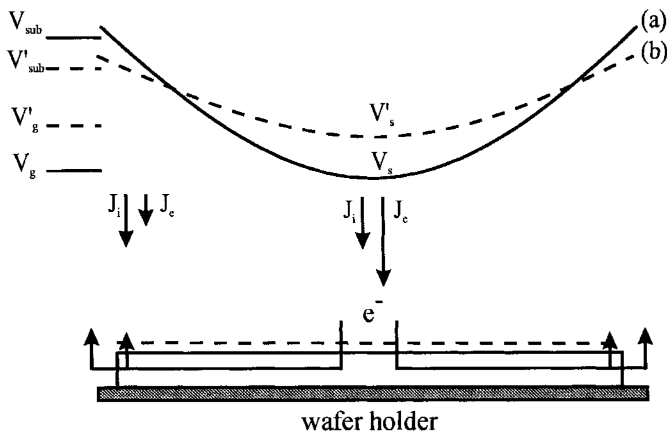

Fig. 2. Diagrams of surface potential dictated by the plasma. (a) Resist surface floating potential which tracks the plasma potential for the wafer with resist overlayer [6]. (b) Gate potential distribution after plasma self-adjustment for the sample without resist overlayer.

Thus, if charge imbalance is solely determined by plasma nonuniformity, this phenomenon should not occur. Finally, it should be noted that electron shading effect should not cause damage on thin oxide with area-intensive antenna structure [9]. To explain our experimental results, we have but to reconsider the role of photoresist on the wafer surface in the charging mechanism [2], [3].

Previously, Cheung has pointed out that the electric-field across gate oxide resulted from plasma nonuniformity cannot

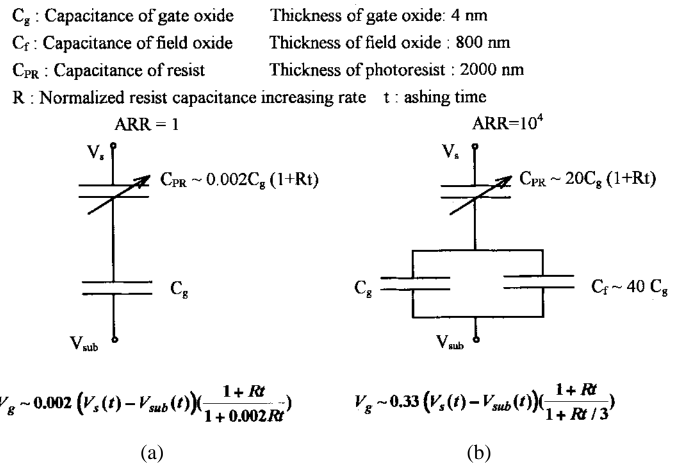

Fig. 3. A simple equivalent capacitor circuit for the devices with resist overlayer: (a) control sample and (b) sample with large antenna (ARR $= 10^4$) electrodes.

cause oxide breakdown due to the limited supply of current [6]. The oxide field induced by plasma cannot develop to the full extent since the substrate and gate potential will both respond in order to reach charge balance on the wafer surface, i.e., self-adjustment. Fig. 2 shows the illustrative diagrams of potential adjustment of the samples with and without resist overlayer. The self adjustment behavior will enhance gate potential at the wafer center by losing electron from wafer surface to the substrate, and the substrate potential is lowered. When the wafer is exposed to the plasma without resist blocking, most of the electron current can easily flow through substrate contact, and the adjustment behavior will be so effective if the exposed substrate area is large enough [6]. Potential distribution will rapidly change as shown in (b) of Fig. 2. Therefore only very little current resulting from charge imbalance will pass through thin gate oxide. In fact, only minor damage is observed even in the largest ARR case without resist covering. With resist being an insulator as an overlayer, however, the potential adjustment is severely retarded. There will be a large voltage difference between the wafer substrate and the gate at the wafer center as a result of plasma nonuniformity. A simple equivalent circuit, as shown in Fig. 3, can be used to illustrate what happens to thin gate oxides with the presence of resist on the gate electrodes [7]. As shown in Fig. 3(a), for the case when the gate electrode area is comparable to the active region (i.e., small ARR ratio), the voltage difference between the wafer surface and the substrate will mostly drop across the resist and no severe damage on thin oxides is expected. But, when the gate electrode is attached with large ARR metal pad, voltage built up on thin oxide could become 100× larger as shown in Fig. 3(b). Although the voltage starts to drop after the tunneling current begins to flow, high field still could sustain for a period of time, because the resist capacitance increases while the resist is being gradually removed. As a consequence, the total charge fluence collected by the large antenna pad edge causes damaging effects on the underneath thin oxide (i.e., either broken or quasi-broken). It should be emphasized that the dynamic behavior is much more complex beyond our description in Fig. 2, and more endeavor should

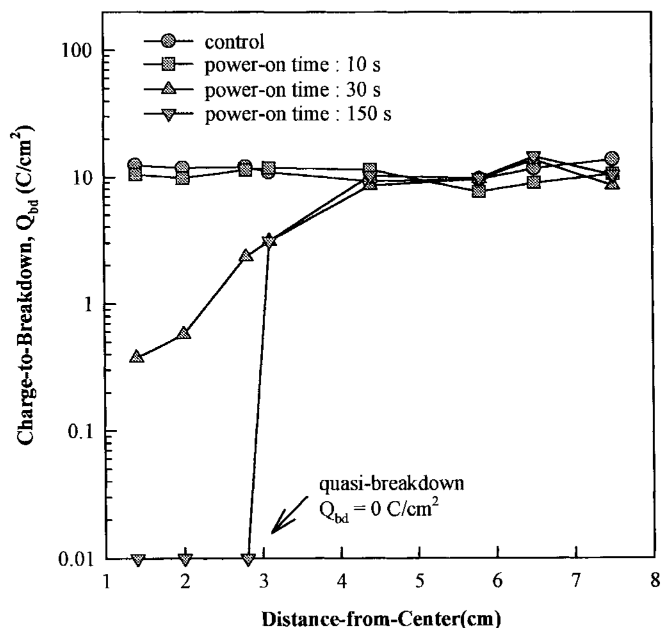

Fig. 4. The evolution of spatial charge-to-breakdown distribution with different RF power-on times. Ultrathin oxide thickness is 4.2 nm and the stress current is -100 mA/cm^2, i.e., gate injection at 25 °C. ARR = 10^4. Control samples are from the wafer without plasma ashing.

be taken to investigate the exact mechanism. Nonetheless, this model can be roughly illustrated by the evolution of spatial charge-to-breakdown distribution with different RF power-on times in Fig. 4. Essentially, the degree of damage increases with process time. No obvious degradation of the devices is observed for a short 10-s RF power-on time, while severe oxide damage appears at the wafer center for 30-s power-on time. Actually resist is still on the metal pads at this processing stage. This resist-related charging damage is found to strongly depend on oxide thickness [5]. As the oxide thickness becomes thicker, this phenomenon is hardly observed. The critical oxide thickness depends on the plasma potential condition.

IV. Summary

It has been generally recognized that photoresist acts as a protection layer during plasma etching and ashing [1]–[4]. In this work, however, photoresist is clearly demonstrated to be a source of damage rather than a protection layer. Our results indicate that the occurrence of antenna effect induced on ultrathin oxides (<6 nm) correlates with the presence of resist overlayer [5]. This is ascribed to the retarded capability of adjusting the potential difference between wafer surface and substrate. A model is proposed to explain this resist-related antenna effect. Unlike the electron shading effect [9], the damage is not resulted from the dense line patterns which are not used in our study. Therefore, the role played by the resist during plasma processing should be carefully examined, especially for future technologies where ultrathin oxides are used.

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