Design and Fabrication of 0/1-Level RF-Via Interconnect for RF-MEMS Packaging Applications

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***Abstract*—This paper presents the parametric study of RF-via (0-level) and flip-chip bump (1-level) transitions for applications of packaging coplanar RF-MEMS devices. The key parameters were found to be the bumps' and vias' positions and the overlap of the metal pads, which should be carefully considered in the entire two levels of packages. The length of the backside transmission line, determining the MEMS substrate area, showed minor influence on the interconnect performance. With the experimental results, the design rules have been developed and established. The optimized interconnect structure for the two levels of packages demonstrates the return loss beyond 15 dB and the insertion loss within 0.6 dB from dc to 60 GHz.**

***Index Terms*—Fabrication, interconnections, microelectromechanical devices, microwave technology, packaging.**

I. Introduction

RADIO-FREQUENCY micro-electro-mechanical system (RF-MEMS) devices have demonstrated great potential for applications at millimeter-wave frequencies because of several advantages such as high signal linearity, low insertion loss, and power saving [1]. For RF-MEMS devices to be reliably used, the devices have to be packaged in a stable and hermetic environment [2]. However, the key requirement for packaging is that it should not lead to any performance degradation of RF-MEMS devices, especially the RF characteristics.

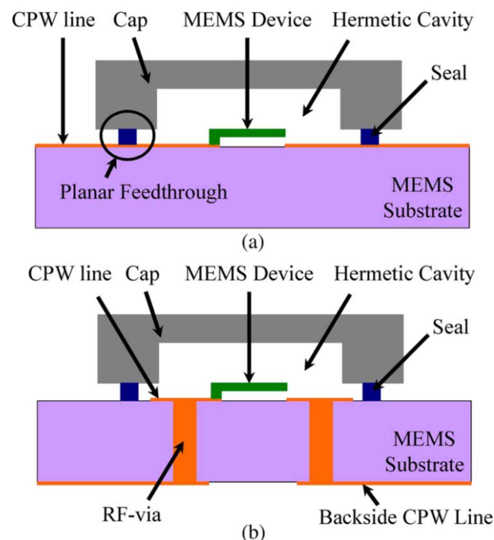

Fig. 1. Two main 0-level interconnect schemes for RF-MEMS devices. (a) RF planar feed-through. (b) RF-Via transition.

At 0-level packaging, a ceramic cap or metal can is usually employed to form a hermetic cavity for sealing the RF-MEMS devices. Fig. 1 shows two main 0-level interconnect schemes for RF-MEMS devices, RF direct feed-through and RF-via transition [1], [2]. RF feed-through scheme requires a thin dielectric layer on the transmission line to pass RF signals through the sealed cap, which causes additional return loss and insertion loss due to the impedance mismatching [3], [4]. Furthermore, the hermeticity of the cavity is not so good since the seals have to cross over the planar transmission line, resulting in degradation of device reliability. The second scheme of the 0-level package is the RF transition by vertical RF-via transitions. A silicon micromachined on-wafer package scheme for RF-MEMS switch was reported using dc and RF vertical via transitions through the wafer [5], [6], which can easily form a real hermetic package for MEMS devices because the hermeticity of the sealing can be achieved by using soldering or gold–gold thermocompression at the seals. However, RF vertical via transitions can have strong impacts on the performances of the packaged RF-MEMS devices because of the involved via parasitics. When operating frequency increases, a poor consideration in packaging can result in serious reflection and impedance mismatch, causing signal

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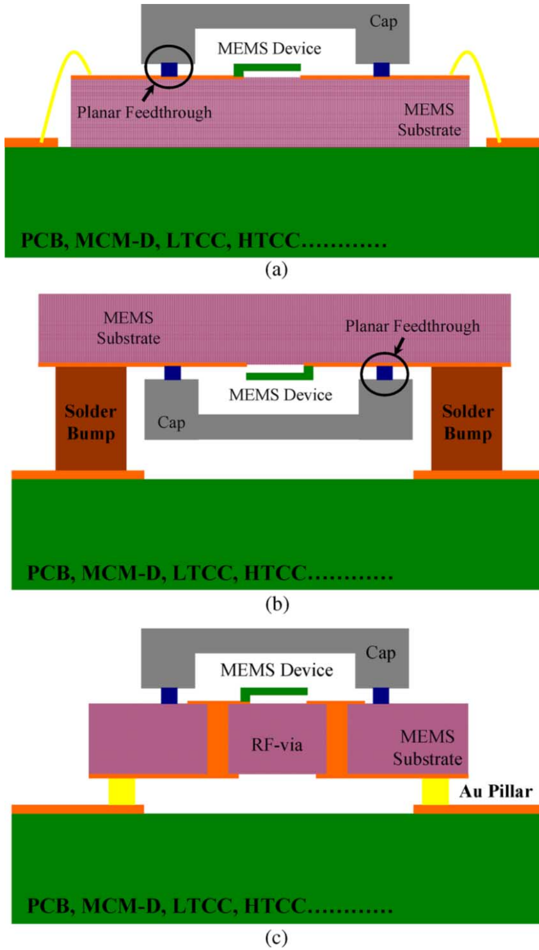


Fig. 2. Three main possible 0/1-level packaging structures (a) planar RF feedthrough with wire-bonding (b) planar RF feedthrough with flip-chip (c) RF-via transition with bump interconnect (similar to "hot-via").

loss. The situation becomes worse if the packaging level increases further.

At 1-level packaging, there are several possible packaging architectures depending on which 0-level package used. Fig. 2 illustrates three main possible 0/1-level packaging structures. For planar RF feed-through, both wire-bonding and flip-chip can be used as the 1-level interconnect. Wire-bonding [Fig. 2(a)] uses attenuated wires to connect 0- and 1-level packages, which generates serious parasitic effects at higher frequency due to its long interconnect length. Flip-chip, on the other hand, is a more promising high frequency interconnect technology because of excellent RF performance [7], high input/output (I/O) density, fast assembly speed and higher production yield. From Fig. 2(b), however, when using planar feed-through, higher flip-chip bump height and additional chip area for pads are needed. It increases the package cost and the size is not compact enough. For RF-via interconnect as shown in Fig. 2(c), a face-up bump transition architecture similar to "hot-via" [8]–[10] can be used to realize a compact and high performance package. Since it is a face-up mounting technology, the chip can be optically inspected after bonding and the detuning effect can also be effectively reduced [8]–[10].

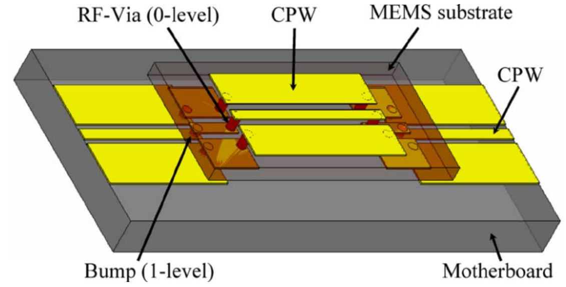


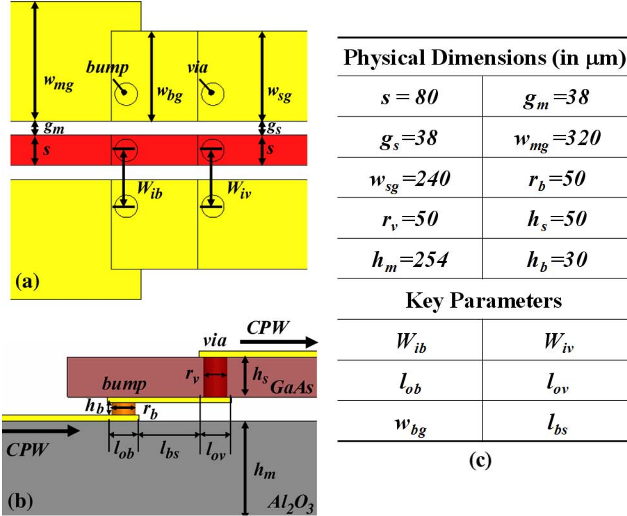
Fig. 3. Schematic of the 0/1-level RF-via interconnect studied in this paper.

From literature, most researches related to RF-MEMS device packaging are mainly focused on 0-level package. Very few studies pay attention on 1-level package. In our previous report, we have presented an optimized 0/1-level RF-via interconnect structure with good performance up to 60 GHz [11]. To further establish the design concepts for coplanar RF-MEMS devices packaging, the 0/1-level interconnect structures using RF-via and bump transitions are experimentally investigated. The interconnect structures with various designed key parameters have been fabricated and characterized from dc to 67 GHz. Based on the experimental results, the optimized interconnect structure including two levels of packages demonstrates the return loss less than 15 dB and the insertion loss within 0.6 dB from dc to 60 GHz, showing the feasibility for application of such technology for the coplanar RF-MEMS device packaging.

II. Design Parameters

Fig. 3 illustrates the schematic of the 0/1-level interconnect structure studied in this paper where the RF-via interconnect is used in 0-level and the vertical bump transition is used in 1-level. The sealing cap is not realized in this study. For the demonstrated interconnect structures, the material of the MEMS substrate and motherboard were GaAs and $\mathrm{Al_2O_3}$; the thickness of the MEMS substrate and motherboard were 50 $\mu\mathrm{m}$ and 254 $\mu\mathrm{m}$, respectively. The conductor metal was 3 $\mu\mathrm{m}$ Au. The characteristic impedances (Z_0) of the coplanar waveguide (CPW) transmission lines on the MEMS substrate and motherboard were both equal to 50 Ω. The total length of the back-to-back 0/1-level RF-via interconnect structure was 3000 $\mu\mathrm{m}$, including 1500 $\mu\mathrm{m}$ on the MEMS substrate and 1500 $\mu\mathrm{m}$ on the motherboard.

In the design, a finite-ground coplanar (FGC) waveguide was employed instead of the conventional CPW with large ground planes to effectively suppress the parallel plate and higher-order modes. To eliminate coupling of CPW mode into slotline mode, the symmetry was always kept along the signal transmission lines [12]. From the literatures, the smaller diameter and larger height of the bumps and vias contribute to an inductive effect, therefore giving compensation to the capacitive part in the vertical transitions, [13]. Considering the process uniformity in the experiments, the diameters of the bump and via were fixed to 50$\mu\mathrm{m}$ and the bump height was 30 $\mu\mathrm{m}$. The physical dimensions and key parameters are summarized in Fig. 4. The parameters in investigation are the distances between ground bumps and vias (w_{ib} and w_{iv}), the metal overlaps (l_{ob} and l_{ov}), and CPW length and width on the backside of the MEMS substrate



Physical Dimensions (in μm)	
$s = 80$	$g_m = 38$
$g_s = 38$	$w_{mg} = 320$
$w_{sg} = 240$	$r_b = 50$
$r_v = 50$	$h_s = 50$
$h_m = 254$	$h_b = 30$
Key Parameters	
W_{ib}	W_{iv}
l_{ob}	l_{ov}
w_{bg}	l_{bs}

Fig. 4. Illustrations of the designed physical dimensions and key parameters (a) top-view (b) cross section and (c) list of physical dimensions and key parameters.

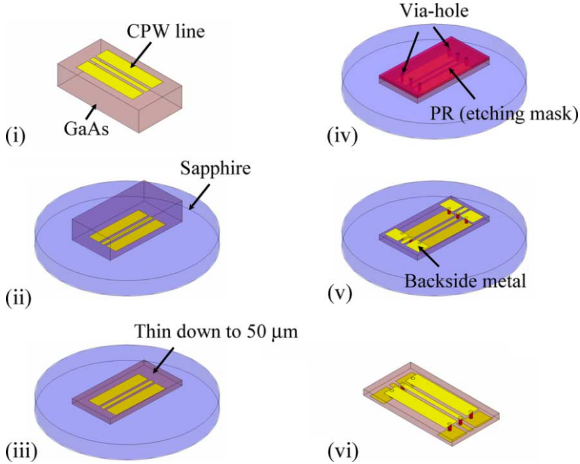


Fig. 5. The process flow of the RF-via interconnect structure.

(l_{bs} and w_{bg}). The interconnect structures with variable parameters were experimentally fabricated and RF characterized to evaluate the best parameters for packaging RF-MEMS devices through 0/1-level packages.

III. Package Fabrication

The demonstrated RF-via interconnect structure was fabricated in-house. Fig. 5 shows the process flow of the RF-via interconnect structure. The CPW transmission lines were first patterned on the front side of the GaAs MEMS substrate by photolithography and electroplating process. The GaAs substrate was then mounted on a sapphire carrier and thinned down to 50 μm. RF-via etching was performed by using inductively coupled plasma (ICP) etcher with BCl_3 and Cl_2 gas mixture, where the etching conditions such as the gases mixture ratio, pressure, and etching power were optimized to achieve high etching rate, high etching selectivity, and good etching profiles. Fig. 6 shows the cross-sectional SEM image of the etched via-hole. The backside metal was patterned on the backside of the MEMS substrate. The demounting process was to immerse the fabricated

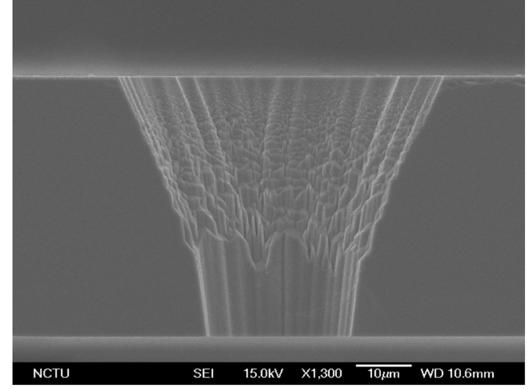


Fig. 6. Cross-sectional SEM image of the etched via-hole.

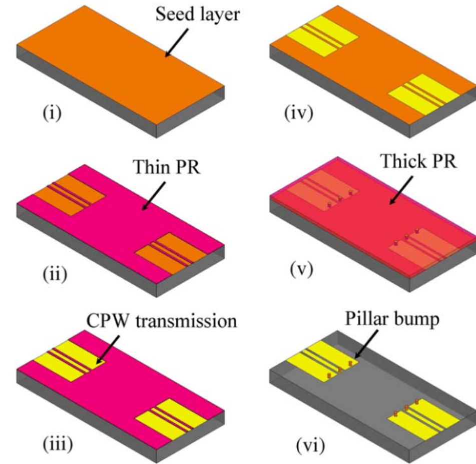


Fig. 7. The process flow of the Al_2O_3 motherboard.

interconnect structure into the stripping solution to remove the sapphire carrier.

The Al_2O_3 motherboard with Au CPW circuits and bumps were fabricated by standard Au bumping process of CSDlab, NCTU [14]. Fig. 7 illustrates the process flow step by step. In the beginning, the metal seed layers Ti and Au are deposited onto the Al_2O_3 motherboard. Then, the thin photoresists are patterned to electroplate the Au CPW transmission line. After the electroplating of the transmission line, the thin photoresists are removed. The thick photoresists are patterned. After that, the pillar bumps are electroplated and the seed layers are removed. The SEM image of the fabricated Al_2O_3 motherboard with Au pillar bumps is shown in Fig. 8.

Finally, the fabricated MEMS substrate with RF-via and the Al_2O_3 motherboard with Au bumps were assembled together by Au-to-Au thermo-compression process to complete the final interconnect structure. The bonding parameters are: bonding force $=$ 120 g (for six bumps), bonding temperature $=$ $300\,^{\circ}$C (for both sides) and bonding hold time $=$ 180 s. Fig. 9 shows the SEM image of the fabricated 0/1-level RF-via interconnect structure.

IV. Experimental Results and Discussions

The scattering parameters of the fabricated 0/1-level RF-via interconnect structures were characterized to 67 GHz using

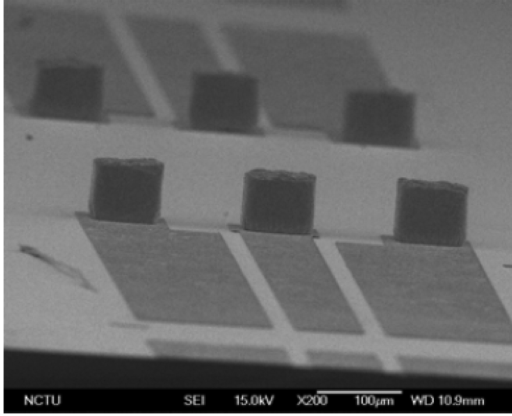


Fig. 8. SEM image of the fabricated Au bumps on Al_2O_3 motherboard.

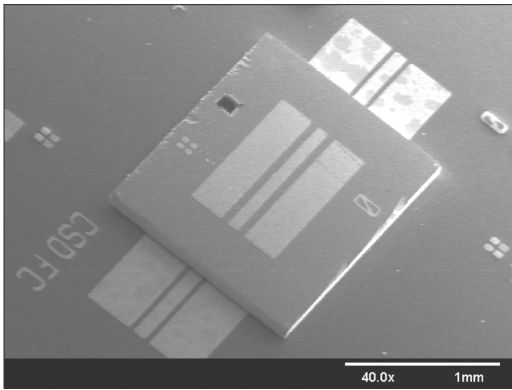


Fig. 9. SEM image of the fabricated back-to-back 0/1-level RF-via interconnect structure.

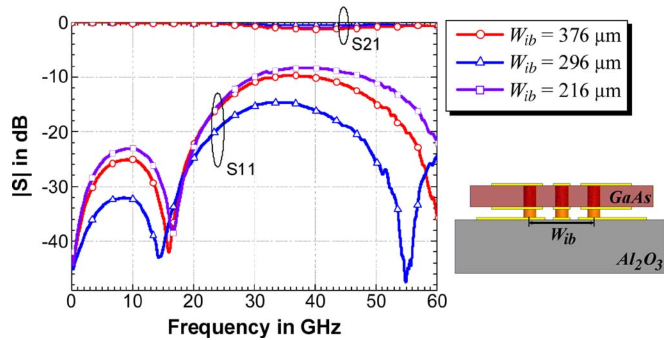


Fig. 10. Measured *S*-parameters of the interconnect structures with different distances between ground bumps (W_{ib}).

on-wafer probing measurement system with an Agilent precision network analyzer (PNA) E8361A. During the measurements, a 10-mm-thick layer of Rohacell 31 ($\varepsilon_{\rm r} = 1.04$ at 26.5 GHz) was placed between the samples and the metal chuck of the probe station to avoid the grounded backside under the substrates. For the interconnect structure, three groups of parameters, i.e., bump and via-hole positions, metal pad overlaps, and backside CPW dimensions were investigated. To validate the measured results, 3-D electromagnetic (EM) field simulation was performed with CST (Computer Simulation Technology) Microwave Studio on the same structures.

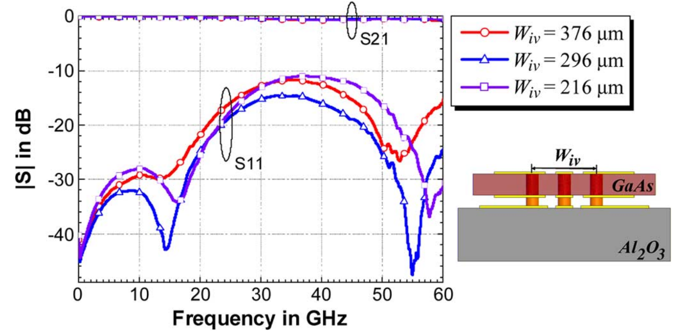


Fig. 11. Measured *S*-parameters of the interconnect structures with different distances between ground vias (W_{iv}).

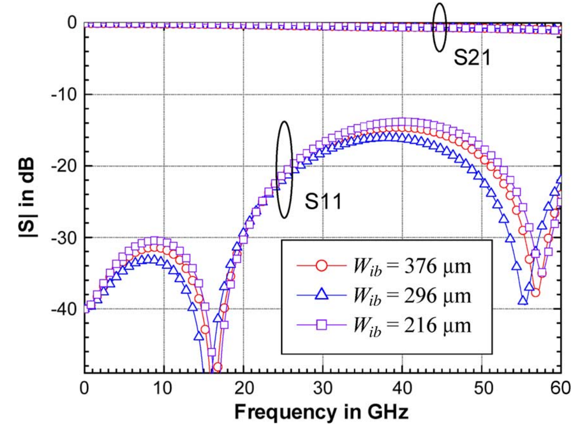


Fig. 12. Simulated *S*-parameters of the interconnect structures with different distances between ground bumps (W_{ib}).

A. Bump and Via-Hole Positions

Figs. 10 and 11 show the measured results of the interconnect structures with different distances between ground bumps and vias (W_{ib} and W_{iv}). From the measured results, as the distances between bumps and vias changed from 216 to 296 μm, the return losses were improved about 8 dB for the case of $W_{ib} = 296\ \mu\text{m}$ and about 5 dB for the case of $W_{iv} = 296\ \mu m$ at 40 GHz, which can be interpreted by the internal compensation effect at the transitions [13]. However, when the distance was further increased to 376 μm, the reflection became worse. From the simulation results shown in Figs. 12 and 13, the trends are similar. The structures with $W_{ib} = 296\ \mu\text{m}$ and $W_{iv} = 296\ \mu\text{m}$ have the best performances. It shows that there is an optimum internal compensation in the 0/1-level RF-via interconnects. Thus, to achieve the best counterbalance of the parasitic effects, the locations of the ground bumps and vias should be well-arranged in the proper positions to obtain the lowest reflection.

B. Metal Pad Overlaps

To improve the transmission characteristics, it is effective to reduce the induced capacitance by decreasing the metal pad overlap areas [13]. From the measured results in Figs. 14 and 15, when the metal pad overlaps (l_{ob} and l_{ov}) decreased from 160 to 80 μm, the measured return loss improved about 8 dB (for l_{ob}) and 6 dB (for l_{ov}) at 40 GHz. Figs. 16 and 17 show the simulation results of the corresponding interconnect structures. As can be seen from both the measured and simulated results,

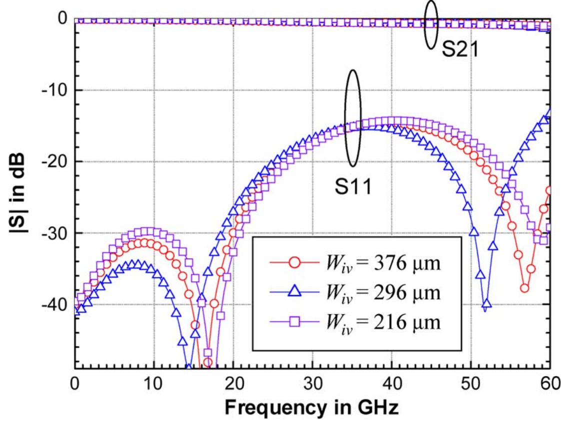


Fig. 13. Simulated *S*-parameters of the interconnect structures with different distances between ground vias (W_{iv}).

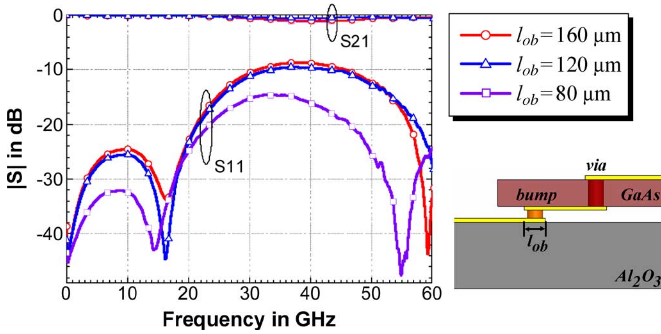


Fig. 14. Measured *S*-parameters of the interconnect structures with different bump pad overlap (l_{ob}).

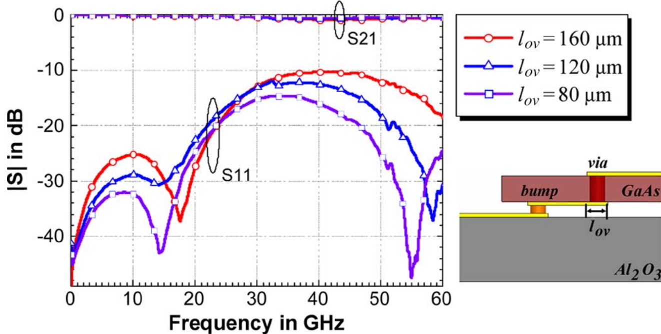


Fig. 15. Measured *S*-parameters of the interconnect structures with different via-hole pad overlap (l_{ov}).

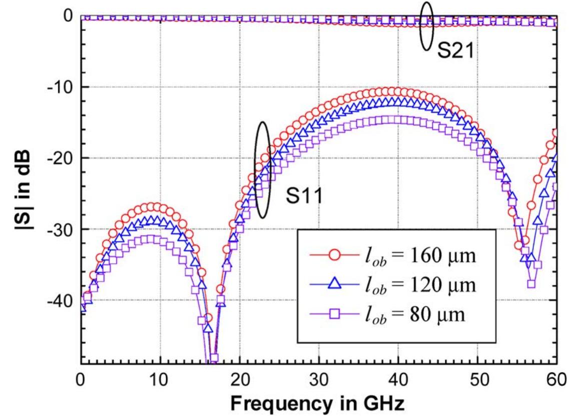


Fig. 16. Simulated *S*-parameters of the interconnect structures with different bump pad overlap (l_{ob}).

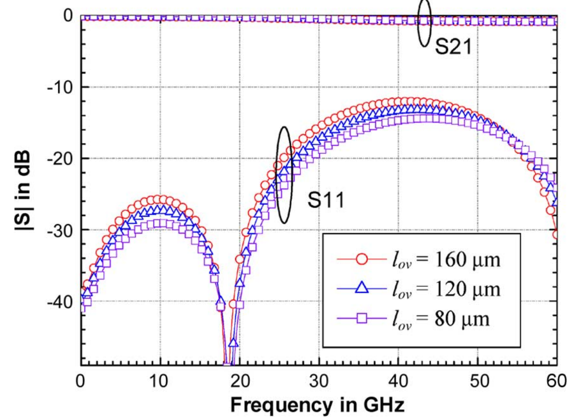


Fig. 17. Simulated *S*-parameters of the interconnect structures with different via-hole pad overlap (l_{ov}).

the reflections were effectively improved by reducing the bump and via pad overlap due to less parasitic capacitance involved. Therefore, the metal overlaps should be kept as small as possible to lower reflection at the transitions.

C. Backside CPW Dimensions

The CPW length on the backside of the MEMS substrate (l_{bs}) determines the RF-MEMS device area, which effects the final cost of the RF-MEMS devices. Shorter backside CPW length (l_{bs}) saves MEMS substrate area. As can been seen from the measured results in Fig. 18 (thick lines), when the length (l_{bs}) was increased from 80 to 150 μm, the measured return loss increased about 2 dB at 40 GHz, showing minor influence on the interconnect performance. Furthermore, the simulation results (thin lines) revealed similar trend with the measured results, indicating the backside CPW length should be kept as short as possible, which would save the MEMS substrate area without causing any degradation of the interconnect performance. For the width of the backside CPW (w_{bg}), similar phenomenon was observed. From Fig. 19, when the width (w_{bg}) was increased from 80 to 240 μm, the return loss remained almost the same for both the measurement and simulation results.

V. Optimization

The 0/1-level RF-via interconnect structure was then optimized based on the experimental results shown above. Fig. 20 shows the measured and simulated results of the back-to-back interconnect structure with the optimized parameters, i.e., $l_{ob} = l_{ov} = 80$ μm, $l_{bs} = 150$ μm, $w_{bg} = 240$ μm, and $W_{ib} = W_{iv} = 296$ μm. From the measured results, the return loss was less than 30 dB from dc to 20 GHz; from 20 to 60 GHz, the return loss was less than 15 dB. The insertion loss was within 0.6 dB from dc to 60 GHz, showing good wideband interconnect performance up to 60 GHz. The simulation results agree well below 40 GHz. Beyond 40 GHz, the simulated return loss is a little higher compared with the measured return loss due to the shift of the resonance frequency at higher frequencies. The

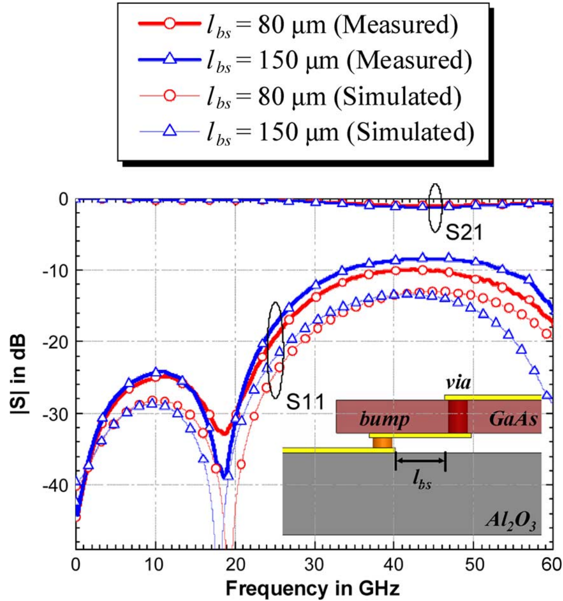


Fig. 18. Measured and simulated S-parameters of the interconnect structures with different backside CPW lengths (l_{bs}).

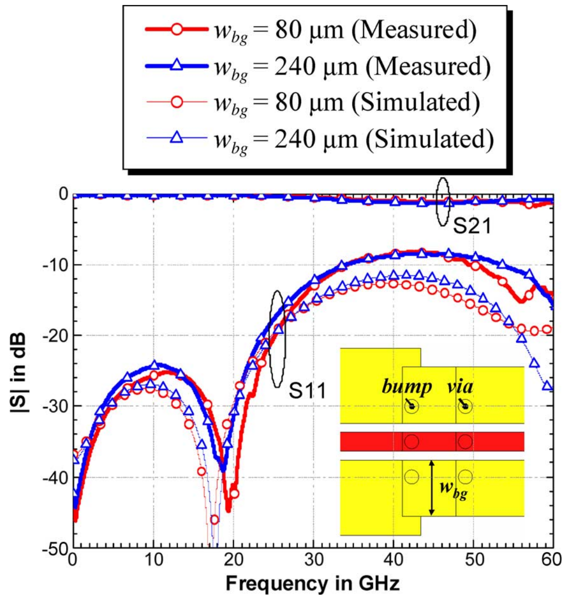


Fig. 19. Measured and simulated S-parameters of the interconnect structures with different backside CPW widths (w_{bg}).

simulated insertion loss, as a result, is higher than the measured insertion loss. Besides, the loss tangent $(\tan\delta)$ of the dielectric materials (GaAs and $\mathrm{Al_2O_3}$) and the resistivity of the metal (Gold) in the simulation models were set to be frequency independent. In reality, however, these material properties would vary with the frequency. In summary, these could be the reasons why the simulated insertion loss does not match well with the measured results after 40 GHz.

VI. Conclusion

For coplanar RF-MEMS devices packaging, the design guideline of 0/1-level RF-via interconnect are determined from the experimental results. First, to give the effective inter-compensation and to achieve low reflection at the interconnect, position of the ground bumps and vias should be considered. Second, the smaller overlap of the metal pads gives lower reflection at the interconnect due to the reduction of the induced capacitance. Third, the backside area for signal transmission from 0- to 1-level must be kept as small as possible to save the MEMS substrate area due to its minor influence on the device performance based on the experimental results. The 0/1-level RF-via interconnect structure with optimized key parameters demonstrated wideband interconnect performance from dc to 60 GHz with return loss less than 15 dB and insertion loss within 0.6 dB, showing the feasibility of such technology for RF-MEMS packaging applications up to V-band.

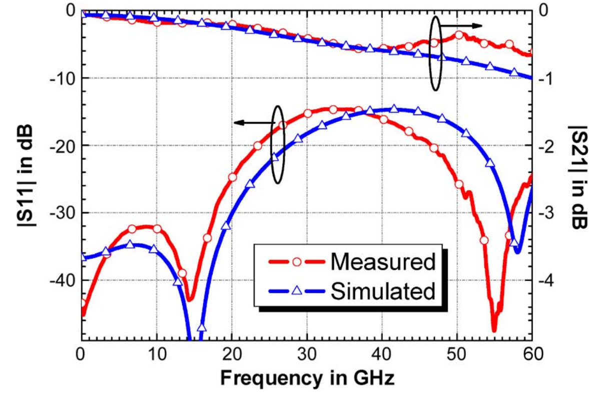


Fig. 20. Measured and simulated S-parameters of the optimized 0/1-level RF-via interconnect structure.

Acknowledgment

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