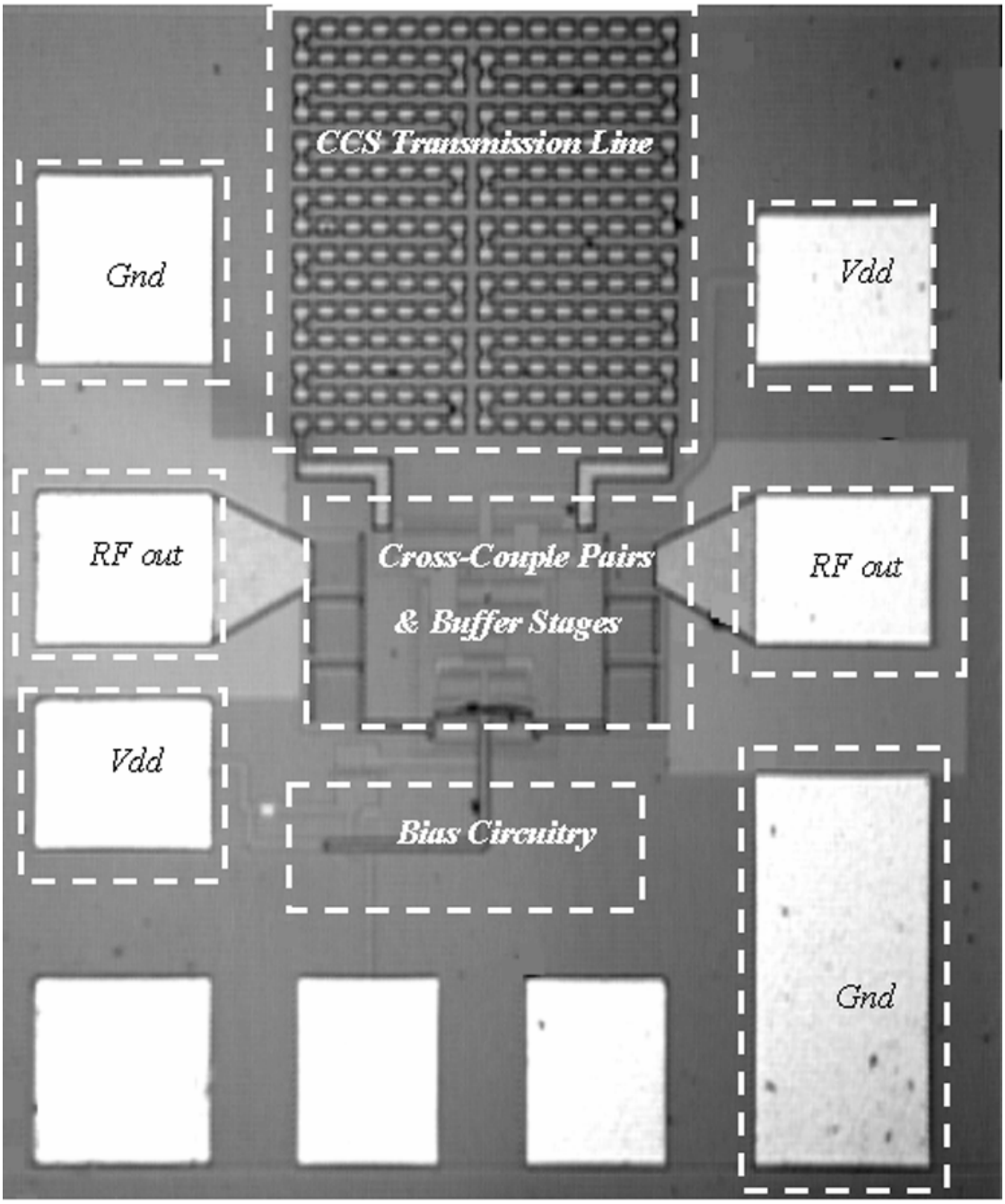
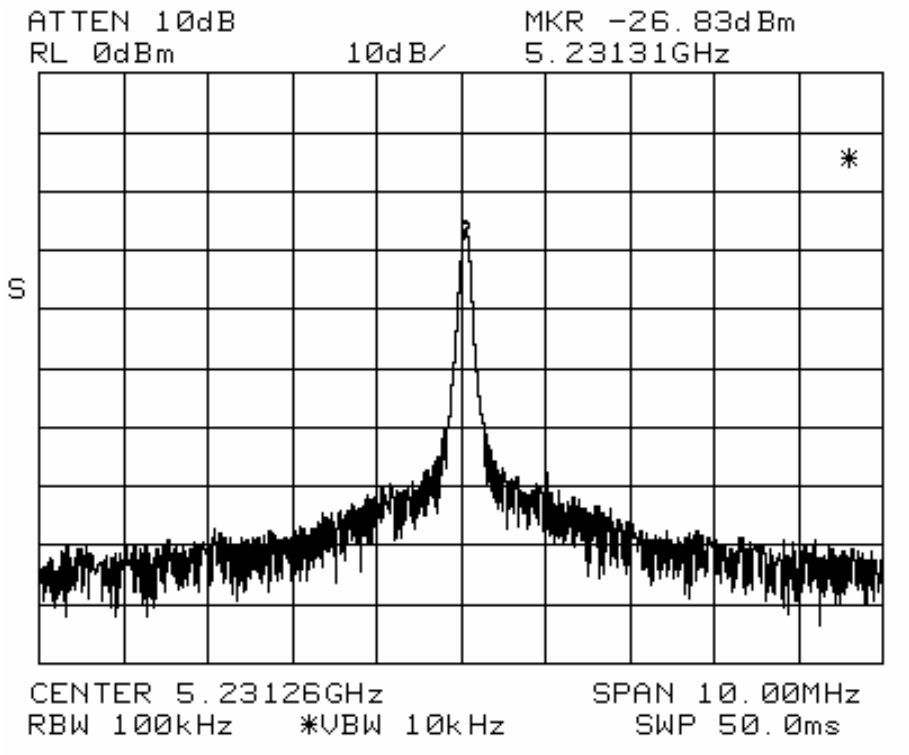
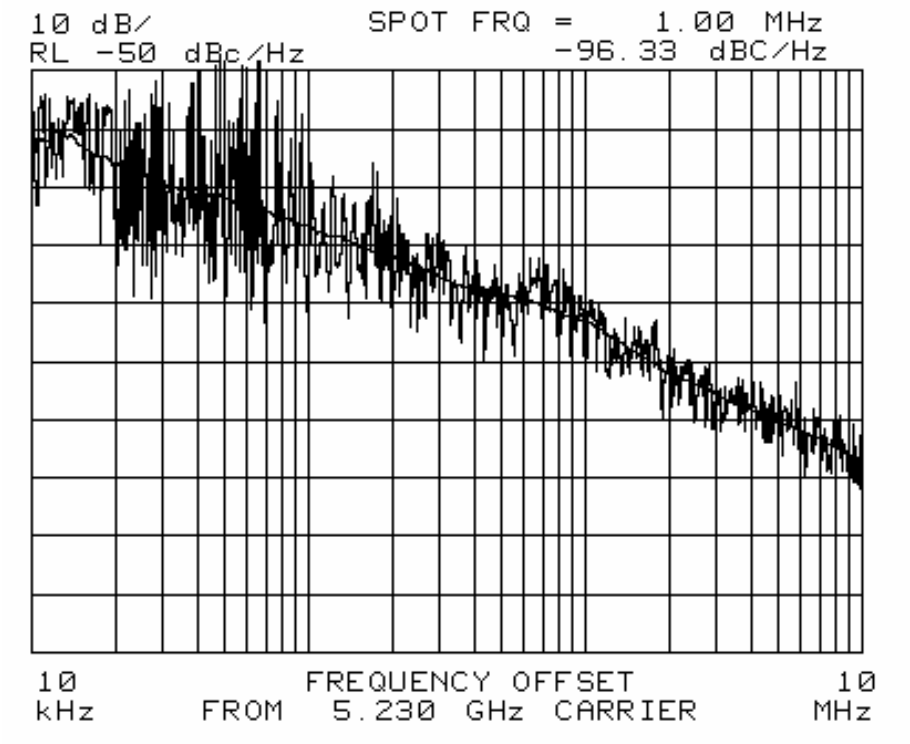


Fig. 4.7. 5.2-GHz CMOS cross-coupled oscillator based on a CCS TL resonator. Chip area: 0.5 mm × 0.6 mm (including pads), 0.225 mm × 0.21 mm (active area), and 0.225 mm × 0.225 mm (CCS TL on top).



(a) Single-ended output power spectrum



(b) Phase noise spectrum

Fig. 4.8. Measured results of the oscillator – (a) single-ended output power spectrum, (b) phase noise spectrum.

power is –25.3 dBm after adjusting the extra 1.53 dB loss. Figure 4.8(b) shows the single sideband (SSB) phase noise plot. The phase noise is –96.33 dBc/Hz at 1MHz offset from the carrier. Measured results agree well with the simulated results except a 3dB variation in the phase noise prediction. This 5.2 GHz oscillator prototype successfully demonstrates the concept of distributed circuit design based on the CCS technology in CMOS. Because the gain of the two buffers, M6 and M7, is unity, it would contribute extra noise to the oscillator and thus degrade the overall phase noise performance. In addition, according to the simulated result of the CCS, as shown in Fig. 4.5, the unloaded Q of the CCS transmission line would increase gradually with the frequencies [56]. It is believed that a low phase noise CMOS oscillator at microwave frequencies can be implemented through this new design methodology. The proper buffer stage design will be considered in the future work.

4.3 Discussion

From the practical application experiences, the dimension P of the unit cell needs to be much smaller than the operating wavelength (λ_g) that is usually 20 cells in a quarter-wavelength line. For the same dimension P, we can use less cells to design circuits in higher frequency applications. But what is the minimum number of cells in a quarter-wavelength line? The answer might depend on your design and circuit demands.

The smaller the value of P, the larger the value of ARF. The choice of P for making CCS TLs depends on the following three factors: 1) required range of the characteristic impedances of the TL; 2) minimum linewidth and line spacing of the particular integrated-circuit process; and 3) maximum current handling capability of the CCS TL. Furthermore, the making tolerance of the particular IC process must be seriously considered when the proper dimensions of P, S, W, and $W_{h,}$ are chosen. This will reduce the relative deviation of dimensions and guiding properties (Z_c, SWF) [63].