CHAPTER 4

Practical Design

The results in Chapter 3 indicate that the 2-D CCS TL can be used to synthesize a wider range of characteristic impedance, flatten propagation characteristics, and place passive TL circuits in a compact area concurrently. This chapter will present the practical design using the synthetic 2-D CCS TL. The technique will be applied to the compact HMIC and monolithic CMOS RFIC. A detailed discussion will be included in this Chapter.

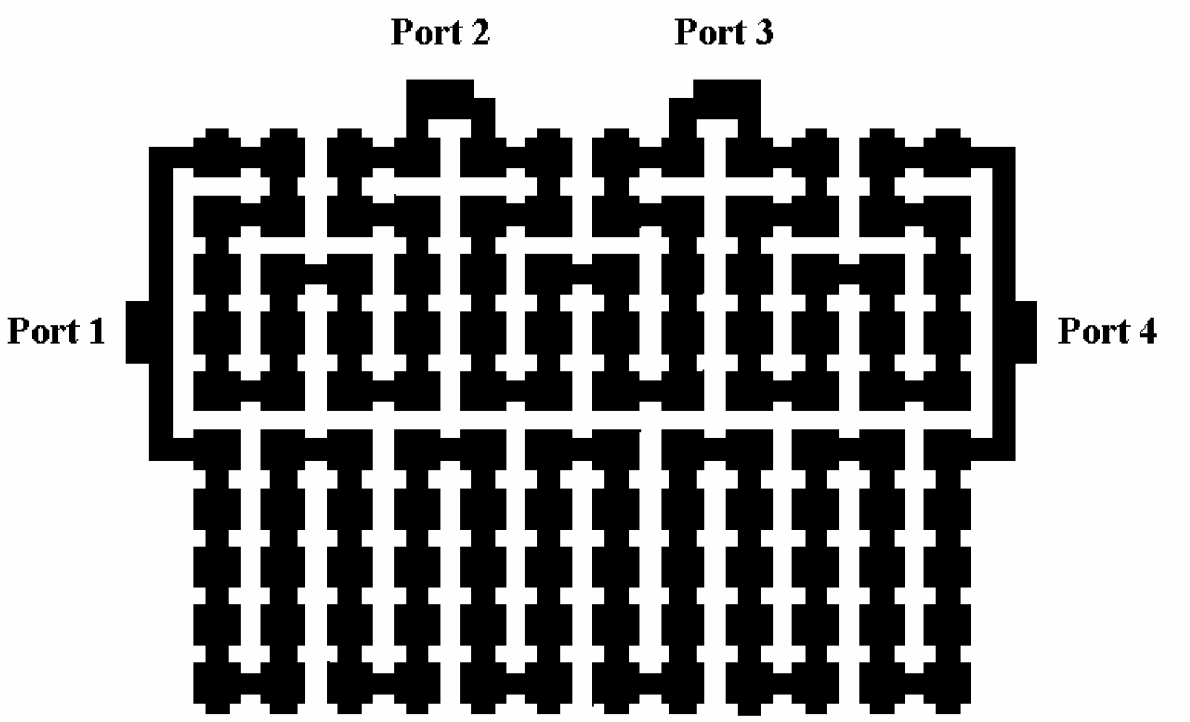
4.1 Miniaturized Rat-Race Hybrid Using CCS TLs

This section presents how CCS TLs are incorporated to designing a popular microwave rat-race hybrid that is often used in a power combiner/divider, balanced mixer/amplifier, etc. Following the design procedure of CCS TLs illustrated in Section 3.2, one may choose the 70-Ω CCS TL by compromising the SWF, loss (decibels/λ_g), current carrying capacity, and PCB design rules. The dashed line of Fig. 3.5(a) represents a 70-Ω characteristic impedance level, which intersects curves for a meandered MS, L7, L5, L4, L3, and L2. The design with larger dimensions in S and W will be less sensitive to process tolerance and capable of handling larger amount of currents. Therefore, L4 is a

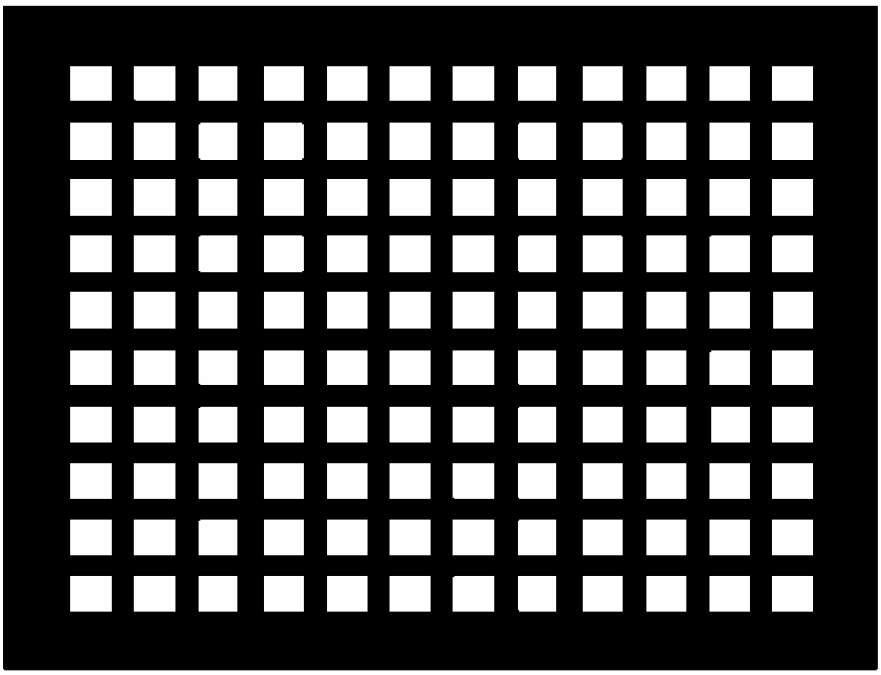
good choice. Fig. 3.5(b) and (c) further validates such a choice from the SWF and attenuation per wavelength points-of-view, both showing a good compromise among Z_c, SWF, and losses. Taking the controlling parameters of L4, namely, S = 150 μm and W_h = 300 μm, we set W = 300 μm, as seen from Fig. 3.5(a). Next, we check such a set of selected parameters in Fig. 3.6 (a)-(c) by varying the width of the connecting arm S for the purpose of fine tuning. The results shown in Fig. 3.6 indicate that Z_c can be 70 Ω for S between 150-200 μm. We select S equal to 150 μm, contemplating that this is already a good choice for Zc = 72 Ω under such condition.

For testing purpose, the four I/O ports must place on the outside of the CCS rat-race hybrid, so the trace pattern 1 and 3 of 2-D CCS TL (5 × 4) in the Fig. 3.7-3.8 can be chosen to design a CCS rat-race hybrid.

To this end the design of the CCS TL for the rat-race hybrid is complete. What follows is an interesting part of the CCS TL circuit design. The entire rat-race coupler circuit is contained in a predetermined rectangular array of 10 × 12 cells without wasting any single grid. Notice that T-junctions are required at the four ports. This can be designed by invoking field simulators for obtaining good electromagnetic models. Fig. 4.1(a) is the top layer metal of the CCS rat-race hybrid design, showing that three quarter-wavelength meandered CCS TLs (trace pattern 3) are in series connections and tapped at ports 2 and 3 by T-



(a) The top pattern

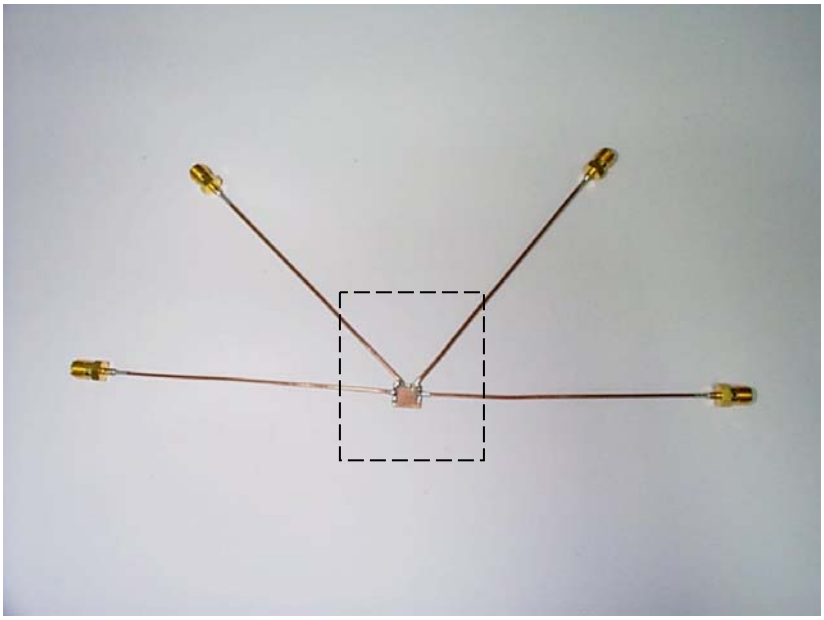


(b) The bottom pattern

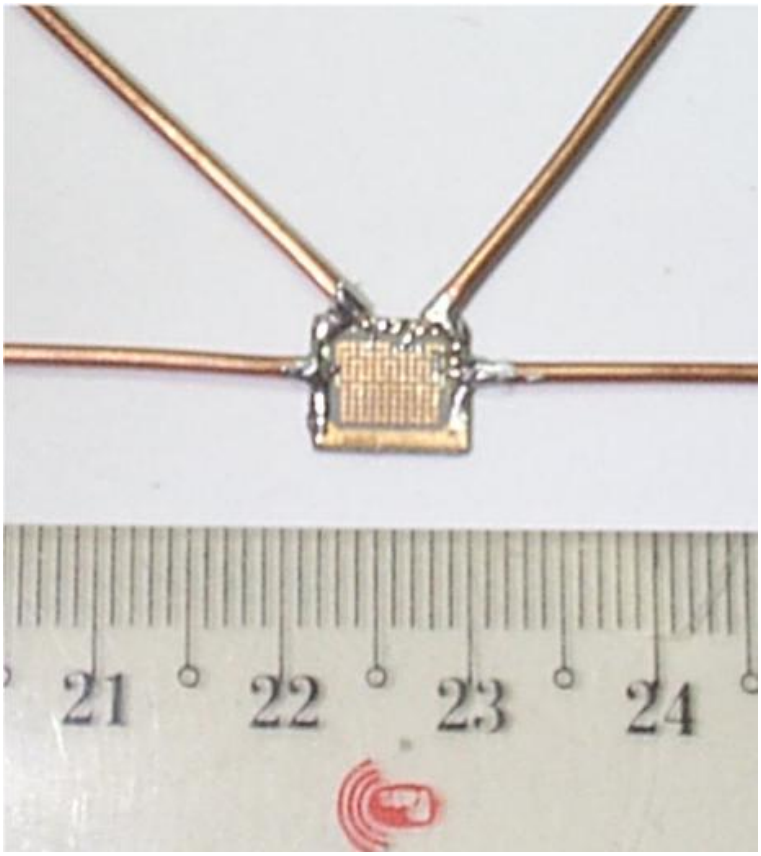
Fig. 4.1. (a) Top pattern and (b) bottom pattern of the CCS rat-race hybrid coupler.

junctions. Also shown in the lower half of Fig. 4.1(a) is the meandered CCS TL (trace pattern 1) of three quarter-wavelengths in parallel with ports 1 and 4. The bottom metal sheet of the CCS rat-race hybrid is shown in Fig. 4.1(b). The meshed ground plane is a 2-D periodic array with its etched portion complementing the top metallic layer structure.

The CCS rat-race hybrid is very small, with an area of only 5.85 mm × 4.725 mm, which is only 13% of that of the conventional MS ring-shape coupler. The available connectors, therefore, cannot be mounted directly on the rat-race hybrid. Strained by the available fixtures, we connect a semirigid coaxial cable to each port. The reference plane is then moved to the open end of the cable at each port by an open-short-load vector network analyzer (VNA) calibration procedure. Finally, ports 1-4 are soldered to the semirigid coaxial cables when needed for making good interfaces between coaxial connectors and the input/output ports of the CCS rat-race hybrid as shown in Fig. 4.2. The measured results are plotted in Fig. 4.3, superimposed by the theoretical plots between 4.6-6.2 GHz. The measured input reflection coefficients of ports 1 and 3 show better performance than the theoretical data and worse results at the high frequency side. The agreement, however, between theoretical results and measured data agree well and the measured response in its worst case is –10 dB at 6.2GHz, which is 0.8 GHz from the design center frequency. The isolation between ports 1 and 3 is kept at least +15 dB across the band. At 5.2 GHz, in



(a) Total view



(b) Enlarged view

Fig. 4.2. (a) Total view, and (b) Enlarged view of the CCS rat-race hybrid coupler measurement setup.

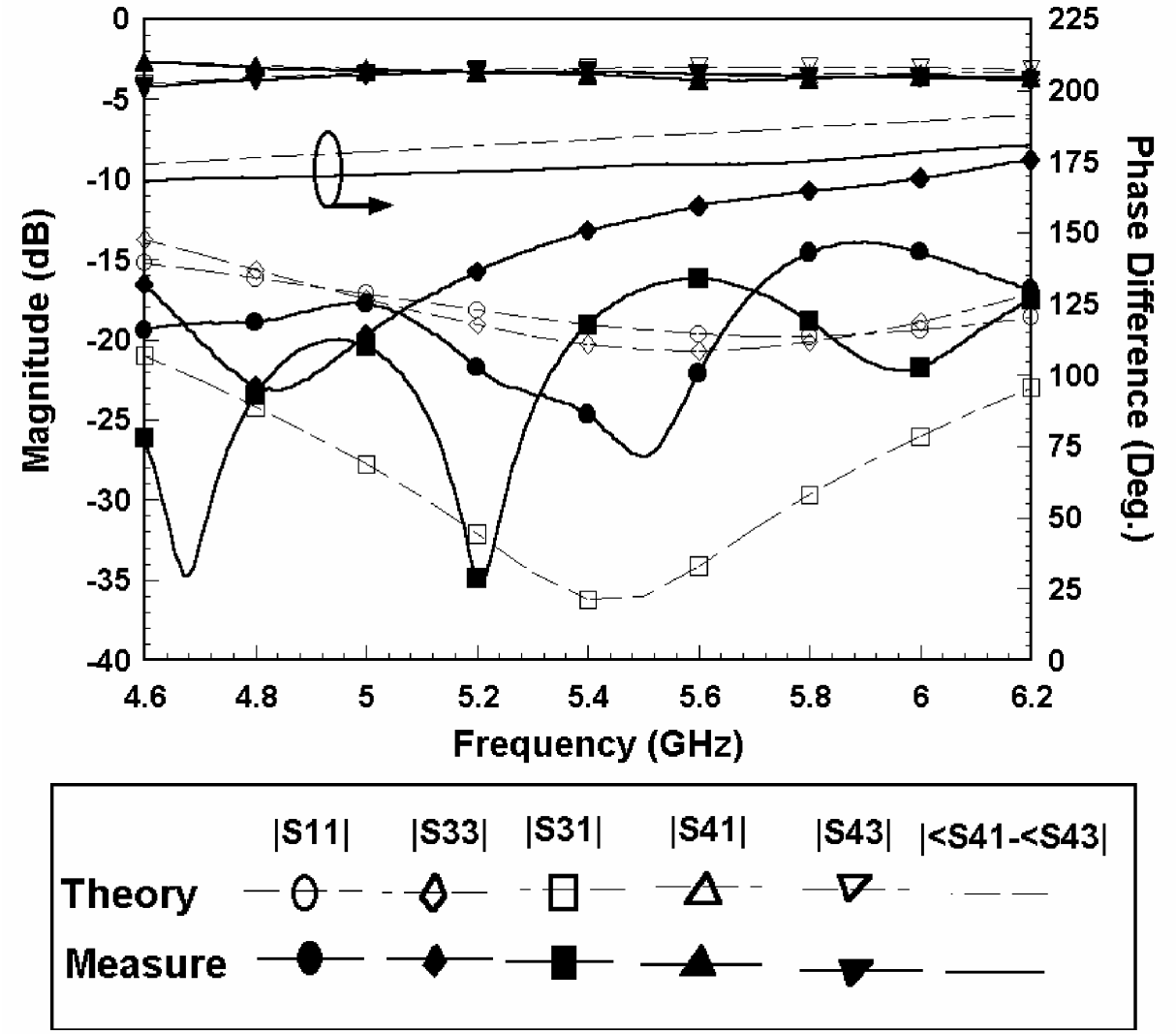


Fig. 4.3. Scattering parameters, return loss $|S_{11}|$, $|S_{33}|$, isolation $|S_{31}|$, coupling loss $|S_{41}|$, $|S_{43}|$, and phase difference $|\angle S_{41} - \angle S_{43}|$ versus frequency of the CCS rat-race hybrid prototype.

particular, the measured isolation is over 35 dB. The measured and simulated transmission characteristics $|S_{41}|$ and $|S_{43}|$ agree very well with each other, over the high-frequency band, deviating by approximately 0.3 dB for $|S_{41}|$, and 0.7 dB for $|S_{43}|$ from the theoretical values. The phase difference $|\angle S_{41}-\angle S_{43}|$ exhibits a 180° phase reversal between ports 1 and 3 and difference port (port 4), and the measured results are only 10° lower than the theoretical results throughout the band. The discrepancy in the S-parameters could be caused by etching pattern, dimension errors and a small stress influence since four longer and heavier semirigid coaxial cables are soldered to the CCS rat-race in the test fixture for S-parameters testing.

4.2 Distributed CMOS Oscillator Using CCS TLs

Lumped LC elements have been widely applied in monolithic RF CMOS and GaAs integrated circuits. The lumped elements operate in the frequency range in that the dimension of lumped elements is much smaller than the operational wavelength. This imposes a serious limit on using lumped elements for the state-of-the-art RFIC approaching millimeter waves and beyond. This section reports a basic research endeavour attempting to demonstrate that the distributed CCS TLs realized in CMOS technology can fully replace the lumped elements at no cost to chip area while achieving reasonable performance [56]. The target RF CMOS circuit is the 5.2-GHz differential cross-coupled oscillator whose LC tank circuit will be substituted by the CCS TL. Referring to Fig. 4.4, transistors M1-M4 form two pairs of negative transconductance (-gm) circuits in parallel. Between nodes X and Y, the CCS TL resonates with the terminal parasitic capacitances associated with nodes X and Y at the desired frequency. When the negative gm values can overcome the losses in the resonator, the circuit oscillates since 100% positive feedback signals are established through the cross-coupled wiring configuration. The parallel LC circuit can be replaced by a half-wavelength TL if the parasitics at nodes X and Y are negligible. Consequently, when resonance occurs at the TL, nodes X and Y are out-of-phase, keeping the oscillator running differentially. Two buffers, M6 and M7, deliver the differential output through the on-chip MIM capacitor to external 50 Ω loads.

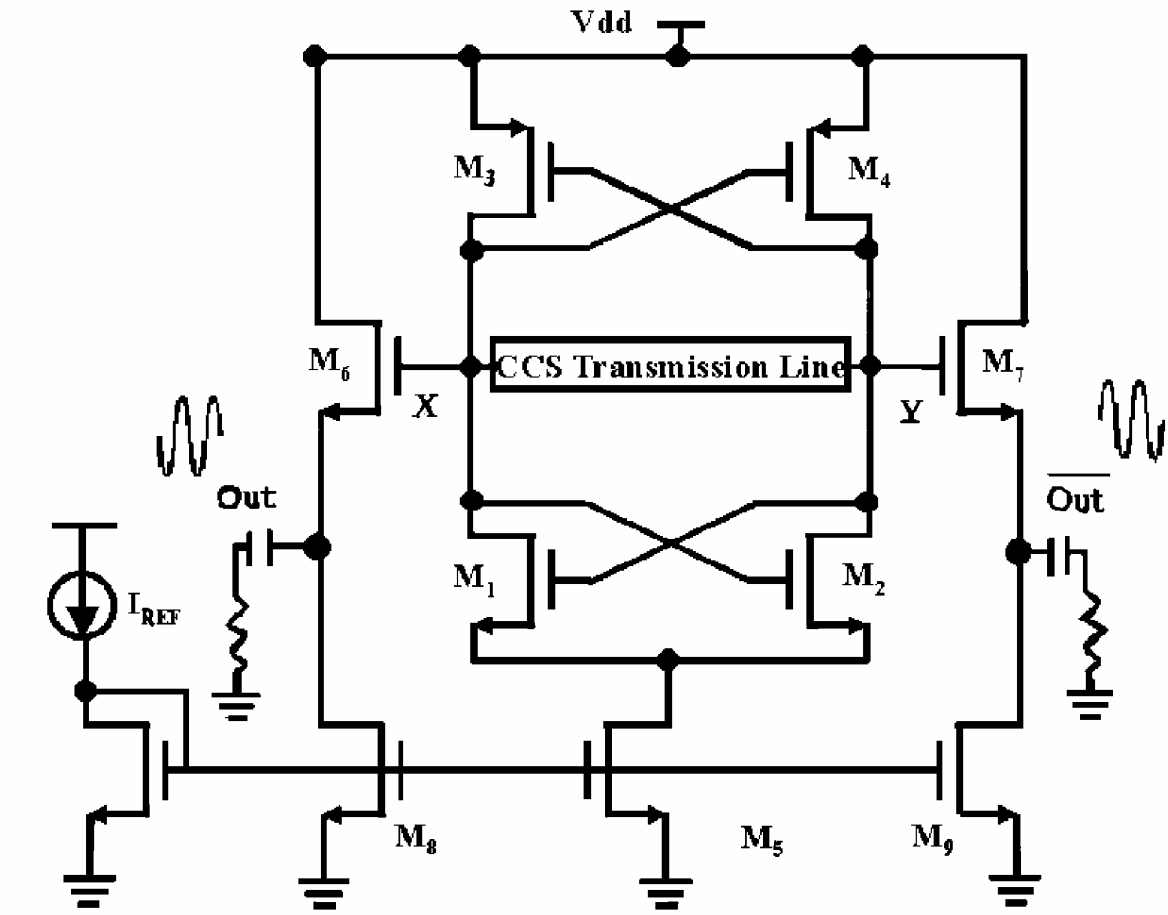


Fig. 4.4. CCS oscillator schematics.

The first step for designing the CCS-based CMOS cross-coupled oscillator is the design of 50-Ω CCS TL. Circuit simulations show that CCS TL of different values of characteristic impedance can work well for the particular design. We choose a 50-Ω line for convenience since many microwave circuits interface to external loads are referenced to 50 Ω. Fig. 4.5 shows the measured and simulated 50-Ω CCS TL based on the Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan, R.O.C., 0.25-μm 1P5M CMOS process technology, which has one poly resistor layer above the active devices and additional five metal layers stacked above the poly. The M1 to M4 layers, numbered in ascending order from bottom surface to top surface, have typical thickness of 0.57 μm, whereas the top M5 layer is 0.99 μm thick. Metals of M1-to-M4 layers made of aluminum (Al) of conductivity (σ) equal to 2.31×10^7 S/m; M5, however, has slightly better conductivity of 2.46×10^7 S/m. The dielectric height, or the metal layer spacing, is near 0.8 μm with inter-material dielectric (IMD) filling of ε_r equal to 4.1. Near the bottom metal layers M1 and M2 are connected by vias to form thicker meshed ground plane and M4 and M5 (the top metal layer) are also connected by vias to form upper signal traces, thus forming the CCS guiding structure. These vias connections reduce sheet resistance and improves the quality factor (Q) of the CCS TL. The periodicity (P) of the CCS TL is 15 μm. The upper surface has a rectangular patch of W_x = 10 μm and W_y = 8 μm and connecting arm of S = 3 μm. The lower complementary surface has rectangular hole of W_{hx} = 14 μm and W_{hy} = 10 μm.

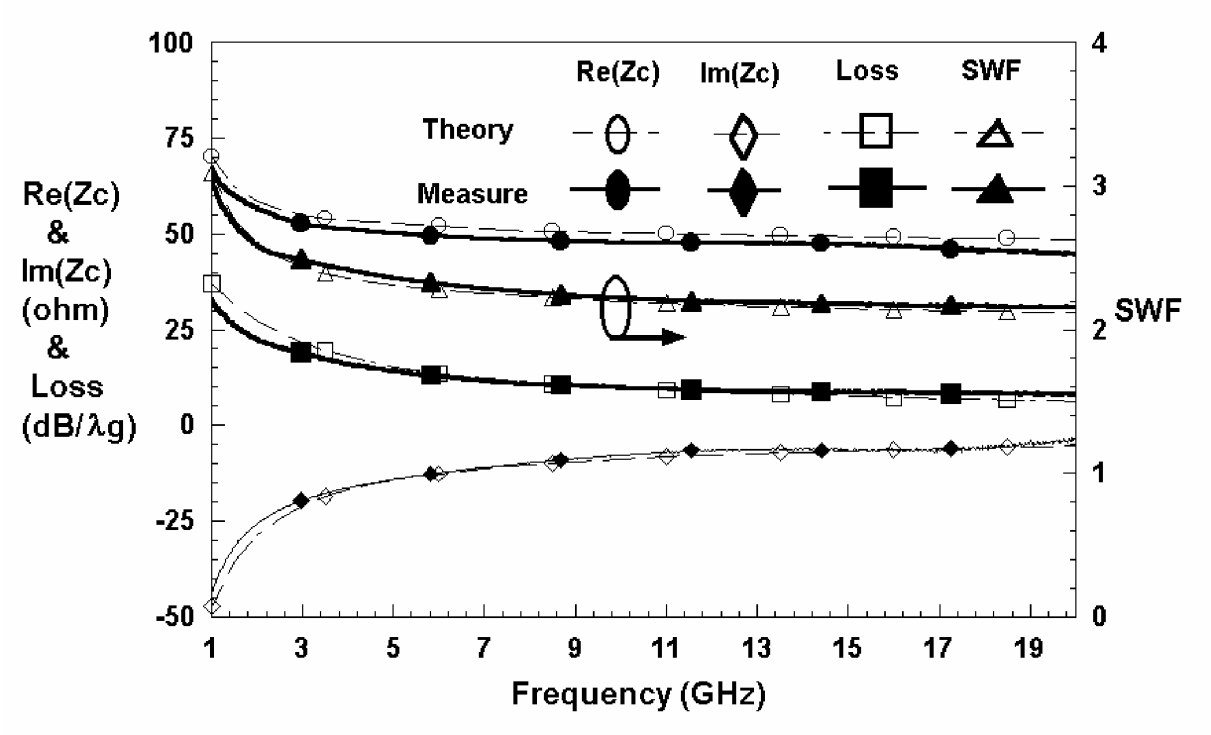
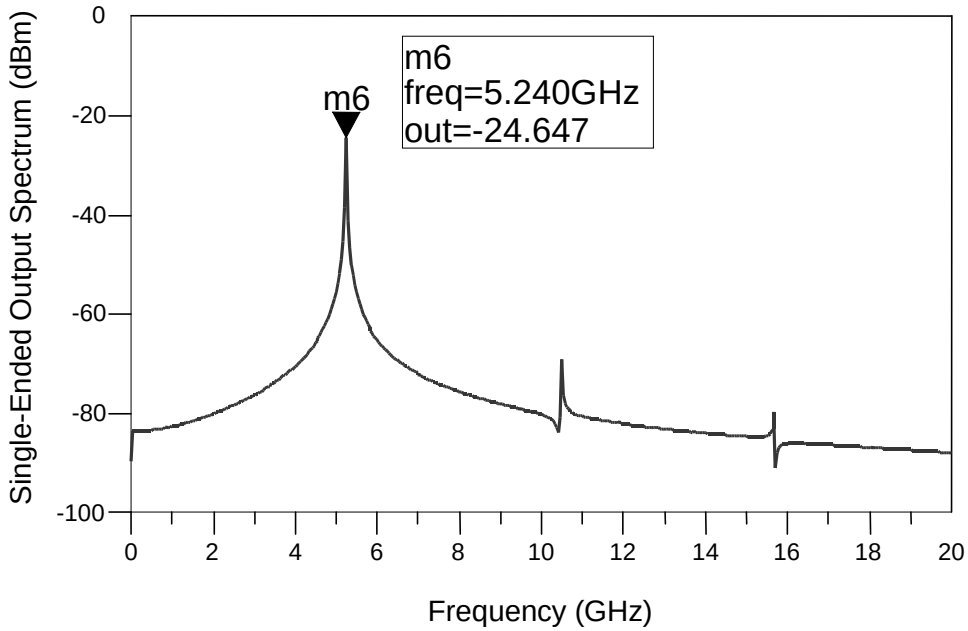


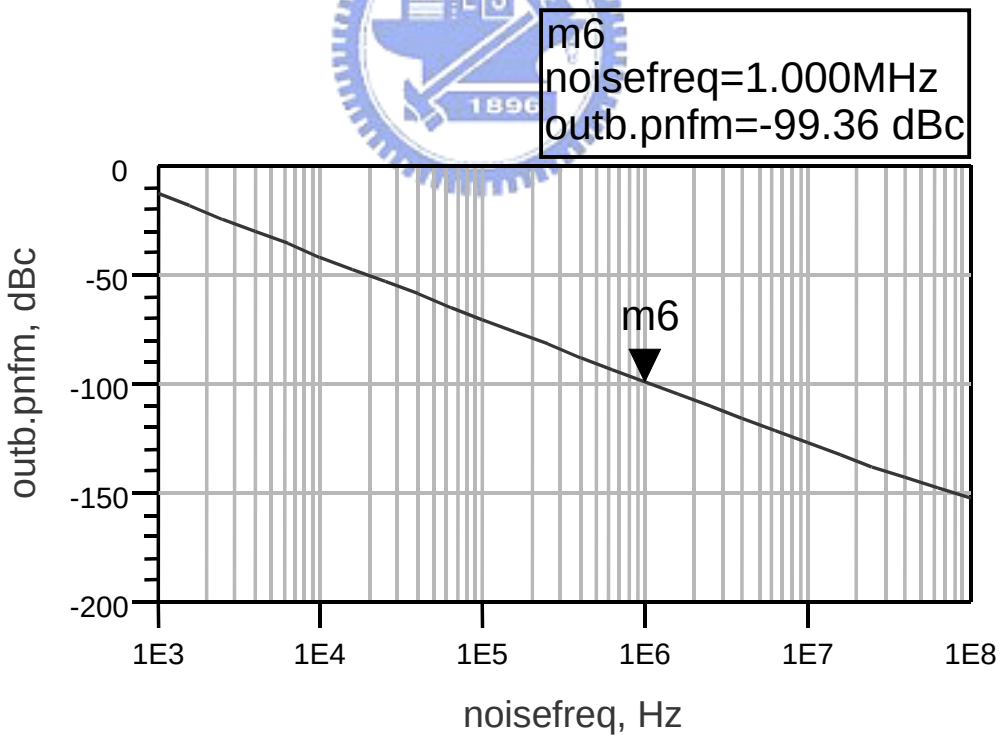
Fig. 4.5. Comparison of the theoretical and measured propagation characteristics $Re(Z_c)$, $Im(Z_c)$, Loss (decibels/λ_g), and SWF of the meandered CMOS CCS TL obtained using a TSMC 0.25-μm 1P5M CMOS process with unit-cell structural parameters P = 15 μm, S = 3 μm, W_x = 10 μm, W_y = 8 μm, W_{hx} = 14 μm, and W_{hy} = 10 μm; 2-D CCS TL (8 × 3 meander trace) and M5 and M4 are set into the top layer and M2 and M1 are set into the bottom layer. The theoretical data is simulated using IE3D^{TM}.

Figure 4.5 compares the theoretical and measured propagation characteristics of the meandered CMOS CCS TL using the TSMC 0.25-μm CMOS standard digital process. Excellent agreements of measured and theoretical data in the real and imaginary parts of Z_c (characteristic impedance) and losses in decibels/λ_g have been obtained. An on-wafer parasitic extraction procedure has been applied to alleviate the parasitic loading of probing pads, as well as the extra interconnects to the device-under-test. The results shown in Fig. 4.5 indicate that we have synthesized a 50-Ω TL across the 5-20-GHz band. The SWF is approximately 2.2 across the band. The loss of 21.5 dB/λ_g is very high at 3 GHz. It declines to 15.3 dB/λ_g at 5 GHz and reaching to 7.6 dB/λ_g at 15 GHz, reflecting the fact the CCS TL is a lossy TL at low microwave frequency range. Thus, a one-half guided-wavelength λ_g at 5.2 GHz is 12.54 mm. This length, at first sight, appears too long to be placed in a monolithic integrated circuit.

The CCS TL concept, however, can easily accommodate the half-wavelength TL resonator into a permissible area. Notice also that the corresponding Q factor of the CCS TL reported in Fig. 4.5 is approximately 1.84 at 5.2 GHz, which is not impressive as a Q factor. Nevertheless, if enough of the biased current source of M5 of Fig. 4.4 is applied, the resultant negative transconductance (–gm) will be large enough to overcome the CCS TL losses, thus forming an oscillator that is free of LC tank lumped elements. Figure 4.6



(a) Single-ended output power spectrum



(b) Phase noise spectrum

Fig. 4.6. Simulated results of the oscillator – (a) single-ended output power spectrum, (b) phase noise spectrum.

depicts the simulated results of the CMOS oscillator, that is obtained from ADS^{TM} Harmonic Balance simulation. The oscillation frequency is 5.24 GHz with an output power of –24.64 dBm. The phase noise is –99.36 dBc/Hz at 1 MHz offset from the carrier. It is believed that this new oscillator design topology is more suitable for operation at higher frequencies by properly adjusting the length of the CCS transmission line. Fig. 4.7 shows a photograph of the cross-coupled CMOS oscillator that incorporates the CCS TL as the sole resonator for defining the oscillation frequency. When taking into account the parasitic capacitance at nodes X and Y of the oscillator shown in Fig. 4.4, the actual length of the meandered CCS TL is approximately 3.375 mm (~ 0.135 λ_g at 5.2 GHz), which still appears too big for monolithic integration. This is, however, not the case for the CCS TL integration. The CMOS chip photograph shows that the CCS TL resonator occupies only 225 μm × 225 μm in chip area. The bias condition for the oscillator core is set at 20 mA from a 3 V supply. A microwave probe station equipped with coplanar signal-ground probes is used to probe the RF pads on the sides. The probes are connected to the measurement instruments through coaxial cables. An HP 8565E spectrum analyzer is used to measure the oscillation frequency and the output power. The measured insertion loss from the probes to the spectrum analyzer is 1.53 dB at 5.2 GHz. Therefore, the measured power on the spectrum analyzer should be adjusted for the extra loss. The measured single-ended output power spectrum is shown in Fig. 4.8(a). The free-running oscillation frequency is 5.23 GHz and the attenuated output