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Using Phosphorus-Doped α-Si Gettering Layers to Improve NILC Poly-Si TFT Performance

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Ni-metal-induced lateral crystallization (NILC) has been utilized to fabricate polycrystalline silicon (poly-Si) thin-film transistors (TFTs). However, the current crystallization technology often leads to trapped Ni and $NiSi_2$ precipitates, thus degrading device performance. In this study, phosphorus-doped amorphous silicon (p-α-Si) and chemical oxide (chem-SiO_2) films were used as Ni-gettering layers. After a gettering process, the Ni impurity within the NILC poly-Si film and the leakage current were both reduced, while the on/off current ratio was increased. This gettering process is compatible with NILC TFT processes and suitable for large-area NILC poly-Si films.

Key words: Ni-metal-induced lateral crystallization (NILC), polycrystalline silicon (poly-Si) thin-film transistors (TFTs), Ni-gettering layers

INTRODUCTION

High-performance low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for application in liquid-crystal displays and organic light-emitting diode displays on cheap glass substrates.[1] Various methods, including excimer laser crystallization (ELC), nickel-metal-induced crystallization (NIC), and nickel-metal-induced laterally crystallization (NILC), for fabricating high-quality poly-Si have been extensively investigated.[2,3] Among these techniques, NILC could not only obtain high-uniformity poly-Si but also reduce manufacturing costs. However, NILC poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, which increase the leakage current and shift the threshold voltage.[4–8] To improve device performance, Ni contamination inside the NILC poly-Si film should be reduced. In previous work we used an amorphous silicon (α-Si) layer and an etch-stop layer to reduce Ni residues inside NILC poly-Si.[9–11] In this study, the performance of these devices was extensively investigated.

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EXPERIMENTAL PROCEDURES

Typical top-gated NILC poly-Si TFTs were used in this study. Figure 1 shows a top view of the fabricated device. NILC/NILC boundaries were located at the middle of the channel region. Two kinds of poly-Si films were investigated in this study. One was a “NILC-Si” poly-Si film fabricated by the traditional NILC method, and the other was a “GETR-Si” poly-Si film fabricated by the same NILC method with an additional Ni-gettering process.

The basic NILC fabrication process of both poly-Si films began with 4-inch Si(100) wafer substrates, on which 500 nm wet oxide films were grown using a H_2/O_2 mixture. Silane-based α-Si films with a thickness of 100 nm were deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C. The photoresist was patterned to form the desired Ni lines, and a 5-nm-thick Ni film was deposited onto the α-Si. The samples were then dipped into acetone for 5 min to remove the photoresist and subsequently annealed at 540°C for 24 h to form the NILC-Si film. To reduce Ni contamination, unreacted Ni metal was removed by chemical etching. The active islands of poly-Si films were defined by reactive ion etching (RIE), as shown in Fig. 2a.

To fabricate the GETR-Si film, a NILC-Si film was dipped into a mixed solution of H_2SO_4 and H_2O_2 for 10 min to form a chem-SiO_2 layer on top of the

Fig. 1. Schematic illustration of the TFT device.

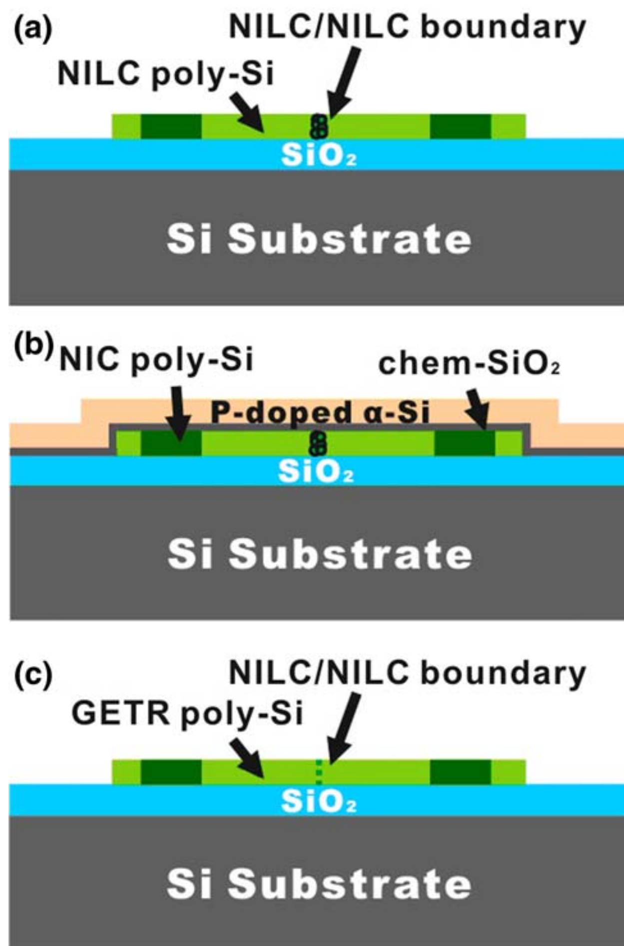

Fig. 2. Schematic illustration of the Ni-gettering process: (a) fabrication of NILC-Si, (b) capped with an etch-stop layer (chem-SiO_2) and a gettering layer (p-α-Si), and (c) removal of the gettering layer and chem-SiO_2 layer.

NILC poly-Si.[10,11] A 100-nm-thick α-Si film was then deposited onto the chem-SiO_2 layer using LPCVD at 550°C. Phosphorous ions were implanted into α-Si at a dose of 1×10^{16} cm^{-2}. The projection range of phosphorous ions was set at the middle of the α-Si film. The phosphorus-doped amorphous silicon (p-α-Si) served as a Ni-gettering layer, while the middle chem-SiO_2 film was used as an etch-stop layer. The chem-SiO_2 film was about 5 nm thick. Even though the thickness of the chem-SiO_2 was not uniform, this oxide film could be a good etch-stop layer for 5% tetramethylammonium hydroxide (TMAH) etching solution. Moreover, chem-SiO_2 also served as a diffusion interlayer during the Ni-gettering process. Ni atoms needed to diffuse from the NILC-Si through the chem-SiO_2 into the Ni-gettering layer. Despite the nonuniform thickness of the SiO_2, the gettering efficiency remained unaffected. This is because the time required for Ni to pass through the chem-SiO_2 ($\sim$5 nm thick) was much shorter than that for Ni to diffuse in the NILC-Si and p-α-Si gettering layers. Samples undergoing Ni-gettering were then annealed at 550°C for 12 h in N_2 ambient to remove unwanted Ni metal inside the NILC-Si, as illustrated in Fig. 2b. Following the annealing process, the phosphorus-doped amorphous silicon (p-α-Si) was removed using 5% TMAH, and the chem-SiO_2 was removed using 1% HF solution, as shown in Fig. 2c. For the purpose of comparison, the NILC-Si (without Ni-gettering layers) film was also subjected to an extended heat treatment at 550°C for 12 h in ambient N_2.

Then, a 100-nm-thick low-temperature oxide (LTO) was deposited by plasma-enhanced CVD (PECVD) as a gate oxide. A 100-nm-thick α-Si film was also deposited as gate material by LPCVD. After defining the gate, self-aligned 35-keV phosphorus ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. They were then activated at 600°C for 12 h. A 500-nm-thick LTO was deposited by PECVD as the isolation layer. Contact holes were formed, and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. The sintering process was performed at 400°C for 30 min.

RESULTS AND DISCUSSION

The NILC-Si film was composed of needle-like NILC poly-Si grains.[11] Figures 1, 2, and 3a show schematic illustrations of silicides observed at the boundaries where two NILC poly-Si fronts intersected (NILC/NILC boundary). When they were dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O = 4:1:50), numerous holes formed at the NILC/NILC boundary, as shown in Fig. 3b. These holes were residues of the Ni silicides that had been etched away by the silicide-etching solution. They were quite sensitive to the reduction of Ni residues in the NILC-Si film and were therefore ideal for elucidating the Ni-gettering phenomenon. After the Ni-gettering process, there were almost no silicide-etched holes found at the NILC/NILC boundaries of the GETR-Si films, as shown in Fig. 3c, indicating that many Ni atoms diffused through the chem-SiO_2 and reached the p-α-Si layer during the gettering process.

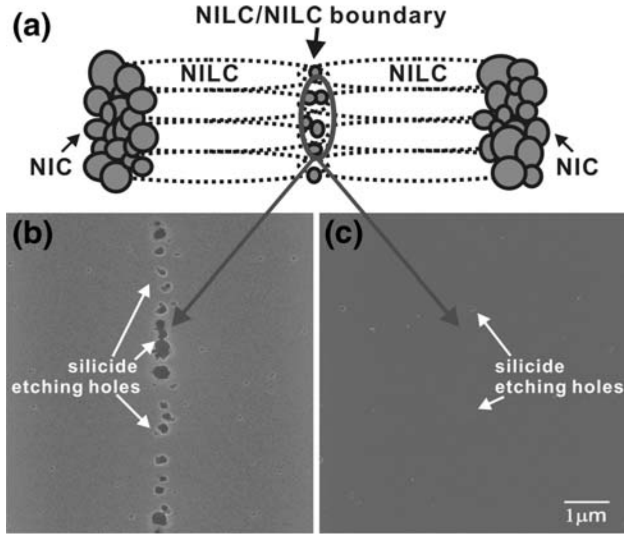

Fig. 3. Schematic illustration of (a) silicide-etched holes at NILC/NILC boundaries, and scanning electron microscopy (SEM) images of these holes in (b) NILC-Si film, and (c) GETR-Si film.

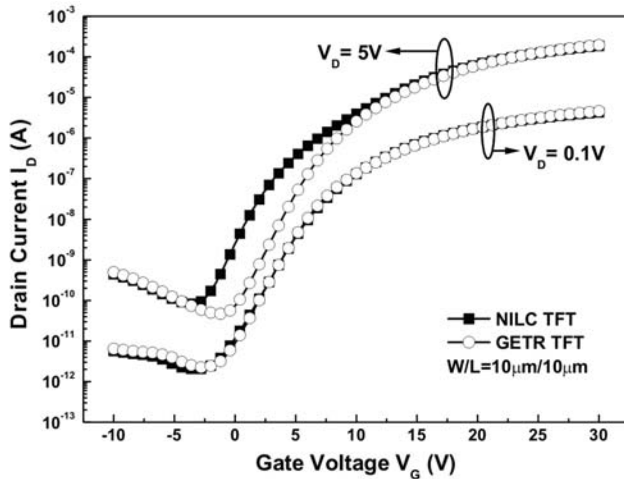

Fig. 4. Typical I_D–V_G transfer curves of NILC and GETR TFTs measured at V_D = 5 V and V_D = 0.1 V, respectively.

Figure 4 shows a typical I_D–V_G TFT transfer characteristic for W/L = 10 μm/10 μm measured at V_D = 5 V and V_D = 0.1 V, respectively. The key measured and extracted device parameters are summarized in Table I. The threshold voltage (V_{TH}) is defined at a normalized drain current of $I_D = (W/L) \times 100$ nA at V_D = 5 V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_D = 0.1 V. The minimum leakage current (I_{OFF_min}) is defined as the minimum current along the gate voltage at V_D = 5 V.

As shown in Table I, GETR TFTs exhibit lower I_{OFF_min}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC TFTs. These improvements were attributed to the reduction of the Ni concentration in the GETR-Si film. In NILC TFTs, Ni-related defects would degrade electrical performance because trap states will introduce dangling bonds and strain bonds. These defects will trap traveling carriers and reduce the mobility of NILC TFTs.[12] Since there were less Ni residues in GETR TFTs than in NILC TFTs, there were fewer defects (caused by Ni residues) in the channel of the GETR than the NILC TFTs. As a result, the mobility of the GETR TFTs was higher than that of the NILC TFTs, as shown in Table I.

Furthermore, NILC/NILC boundaries are the major source of off-state leakage current.[13] In n-type NILC poly-Si TFTs, Ni residues play the role of deep-level traps, which promote thermionic-emission-dominated leakage current.[14,15] Hence, leakage current can be easily induced at higher V_D. With the reduction of the Ni concentration, the minimum leakage current (measured at V_D = 5 V) was reduced, and the on/off current ratio of the GETR TFTs was thus increased. On the other hand, when V_D was low (0.1 V), the minimum leakage current of the GETR TFTs did not change much, as shown in Fig. 4.

In addition, as shown in Table I, the V_{TH} of the GETR TFT was 6.0 V, while that of the NILC TFT was 2.9 V. This is because Ni residues could result in a high density of positive charge at the oxide/NILC poly-Si interface.[16,17] Moreover, Ni residues promote thermionic-emission-dominated leakage current at higher V_D. With the reduction of the Ni concentration, the leakage current was reduced and the negative shift of V_{TH} was suppressed at high V_D. Compared with that of the NILC TFTs, as shown in Table I, the V_{TH} of the GETR TFTs had a positive shift at V_D = 5 V. On the other hand, when V_D was low (0.1 V), the V_{TH} of the GETR TFTs did not change much, as shown in Fig. 4.

These results are similar to the conclusions drawn in our previous study on Ni-gettering substrate fabricated by coating 100-nm-thick α-Si films

Table I. Device characteristics of the NILC and GETR TFTs

W/L = 10 μm/10 μm	NILC TFTs	GETR TFTs
Mobility (cm^2/V-s) at V_D = 0.1 V	75.7 ± 6.3	88.4 ± 4.8
Subthreshold voltage (V) at V_D = 0.1 V	1.51 ± 0.18	1.58 ± 0.12
Threshold voltage (V) at V_D = 5 V	2.9 ± 0.54	6.0 ± 0.3
I_{ON}/I_{OFF} ratio (10^6) at V_D = 5 V	2.27 ± 0.60	3.88 ± 0.33
I_{OFF_min}/W (pA/μm) at V_D = 5 V	8.4 ± 1.8	4.9 ± 0.2

on both sides of a Si wafer.[17] To form the GETR-Si film, the NILC-Si film was bonded to the Ni-gettering substrate and then annealed at 550°C for an additional 12 h. Following the gettering process, the Ni-gettering substrate was separated by using a razor blade. After the Ni-gettering process, it was also found that the number of silicide-etched holes at the NILC/NILC boundaries was greatly reduced, while the V_{TH} of the GETR TFTs was increased. The device transfer characteristics of the GETR TFTs showed an 8.5-fold increase in on/off current ratio and a 34.1-fold decrease in minimum leakage current compared with those of the NILC TFTs. However the mobility of the GETR TFTs was less than that of the NILC TFTs because the crystal quality of GETR-Si was poorer than that of NILC-Si. This is because, in our previous study on gettering substrate, the gettering of Ni in GETR-Si resulted in less complete crystallization.

In contrast, both the on/off current ratio and minimum leakage of the GETR TFTs were improved in this study, though the improvements were not as good as those previously reported.[17] This might be because, in this study, only a single 100-nm-thick p-α-Si film was used as the gettering layer, while in the study on gettering substrate, two α-Si films and a Si wafer were used as gettering layers. As a result, the gettering efficiency of gettering substrates was better than that of p-α-Si films.

Another difference from the previous study was the improvement in the GETR-Si mobility. This might also be attributed to the lower gettering efficiency of p-α-Si films than that of gettering substrates. Compared with the results in the study on gettering substrate, the Ni concentration in this study was higher; hence, the crystal quality of GETR-Si was also better.

The gettering efficiency of gettering substrates was better than that of p-α-Si films. Nevertheless, the gettering substrate method is not suitable for large-area NILC poly-Si films. On the other hand, the gettering process of p-α-Si films was compatible with NILC TFT processes and is suitable for large-area NILC poly-Si films. The gettering efficiency of p-α-Si films could be improved by increasing the α-Si thickness. This is because, during the Ni-gettering process, when more Ni atoms diffused into the gettering layer, more α-Si would be transformed into poly-Si by the NILC mechanism.[10] Since the poly-Si grain boundaries trapped Ni and $NiSi_2$ precipitates, the gettering efficiency increased with α-Si thickness.

The other important issue for poly-Si TFTs is their uniformity. Figure 5 shows the cumulative distribution parameter ΔV_{TH}, and I_{OFF_min} extracted from the I_D–V_G transfer curve. The shift of the threshold voltage (ΔV_{TH}) is defined as $V_{TH,1}$–$V_{TH,2}$, where $V_{TH,1}$ and $V_{TH,2}$ denote V_G with a drain current of $I_D = (W/L) \times 10$ nA at $V_D = 0.1$ V and 5 V, respectively. Compared with NILC TFTs, GETR TFTs showed a 2.5-V reduction in ΔV_{TH} and

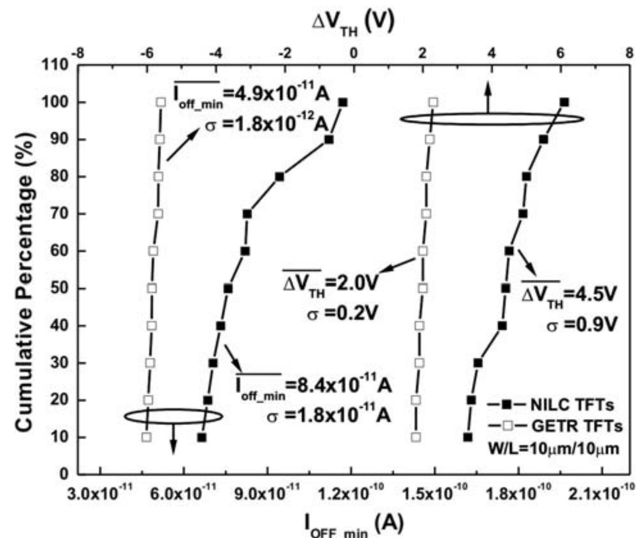

Fig. 5. ΔV_{TH} and I_{OFF_min} measured in ten TFTs to investigate device-to-device variation.

~42% decrease in I_{OFF_min}. There is a greater variation of 20% in the coefficient of variation (standard deviation/average value) of both parameters in the case of the NILC TFTs, but a smaller variation of only 4–8% in the case of the GETR TFTs. The smaller coefficient of variation of the device performance for GETR TFTs may be attributed to the reduction of Ni.

CONCLUSIONS

Investigation of the effects of Ni-gettering layers (p-α-Si/chem-SiO_2 films) on electrical characteristics of NILC TFTs led to the development of a simple and effective process for improving the electrical properties of large-area NILC TFTs. It was found that silicide-etched holes at NILC/NILC boundaries were almost eliminated after the Ni-gettering process. Compared with NILC TFTs, GETR TFTs exhibit lower I_{OFF_min}, higher I_{ON}/I_{OFF} ratio, higher μ_{FE}, and better uniformity. These improvements were all attributed to the reduction of Ni concentration in the GETR-Si film.

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