New Layout Arrangement to Improve ESD Robustness of Large-Array High-Voltage nLDMOS

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***Abstract*—In high-voltage applications, large-array n-channel lateral DMOS (LA-nLDMOS) is usually required to provide high driving capability. However, without following the foundry-suggested electrostatic discharge (ESD) design guidelines in order to reduce total layout area, LA-nLDMOS is easily damaged once the parasitic bipolar junction transistor is triggered under ESD stresses. Accordingly, the bipolar triggering of LA-nLDMOS usually limits the ESD robustness of LA-nLDMOS, particularly in the open-drain structure. In this letter, a new layout arrangement for LA-nLDMOS has been proposed to suppress the bipolar triggering under ESD stresses. Measurement results in a 0.5-μm 16-V bipolar CMOS DMOS process have confirmed that the new proposed layout arrangement can successfully increase the human-body-model ESD level of the LA-nLDMOS with effective width of 3000 μm from the original 0.75 kV up to 2.75 kV.**

***Index Terms*—Electrostatic discharge (ESD), lateral DMOS (LDMOS), open drain.**

I. Introduction

In HIGH-VOLTAGE (HV) applications, large device dimension with high driving capability is usually required for output drivers. Output n-channel lateral DMOS (nLDMOS) is often drawn in large array (LA-nLDMOS) to meet the specification. Due to the large required device dimension (W/L), LA-nLDMOS is not drawn with electrostatic discharge (ESD) design guidelines under the consideration of layout area. When the LA-nLDMOS is applied in the open-drain structures, power-rail ESD clamp circuit does not help discharge ESD current because there is no forward diode from the output pad to the power supply ($\mathrm{V_{CC}}$) lines.

From the viewpoint of 2-kV human body model (HBM) ESD robustness, ESD protection design of open-drain LA-nLDMOS can be roughly divided into two groups. When the effective gate width of LA-nLDMOS is larger than 10 000 μm, junction area of the diode inherent in the LA-nLDMOS is large enough. The LA-nLDMOS can, therefore, be self-protected against the 2-kV HBM ESD energy without triggering the bipolar junction transistor (BJT) inherent in the LA-nLDMOS. However, for medium-size LA-nLDMOS (effective gate width $< 10\,000$ μm), parasitic BJT is triggered due to the higher current density flowing through the base-emitter junction under the 2-kV HBM ESD energy. Without being drawn with ESD design guidelines, the LA-nLDMOS is easily damaged once the parasitic BJT is triggered. It is therefore challenging to devise an ESD-robust design for the open-drain LA-nLDMOS, particularly for medium-size LA-nLDMOS devices.

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II. ESD Protection Techniques for Large-Array nLDMOS With Open-Drain Structure

A traditional ESD protection method for LA-nLDMOS with open-drain structure is to adopt one additional ESD protection nLDMOS in parallel with the LA-nLDMOS. Because ESD detection circuit is inefficient to lower the bipolar trigger voltage (V_{t1}) of nLDMOS [1], trigger competition between the LA-nLDMOS and the ESD protection nLDMOS has been reported to limit ESD robustness of the open drain output [2].

Aside from the traditional ESD protection method, the embedded SCR structure has been proven as an ESD-robust design to LA-nLDMOS [3], [4]. Careful examination on the trigger voltage walk-in and the safe operating area (SOA) reduction after ESD stresses should be taken into consideration. An effective solution to the ESD-induced trigger voltage walk-in and the SOA reduction of LA-nLDMOS with embedded SCR has been studied in [5].

Because triggering of BJT is critical to LA-nLDMOS under ESD stresses, several process modifications have been proposed to suppress the turn-on behavior of parasitic BJT in LA-nLDMOS [6], [7]. These process modifications require additional process support from foundries, and the cost for production is increased [6]. Furthermore, effectiveness of such a process modification to ESD robustness of medium-size LA-nLDMOS has yet been reported. In this letter, a new layout arrangement to suppress the turn-on behavior of BJT is proposed. The proposed layout technique has been verified in a 0.5-μm 16-V bipolar CMOS DMOS (BCD) process and showed substantial improvement on ESD robustness of the medium-size self-protected LA-nLDMOS in open-drain output buffer.

III. Proposed Structure and Experimental Results

The TLP-measured current–voltage (I–V) characteristics of traditional medium-size LA-nLDMOS are shown in Fig. 1. All LA-nLDMOS devices studied in this letter have the same device dimension of 3000 $\mu\mathrm{m}/0.35$ μm. Each finger width of

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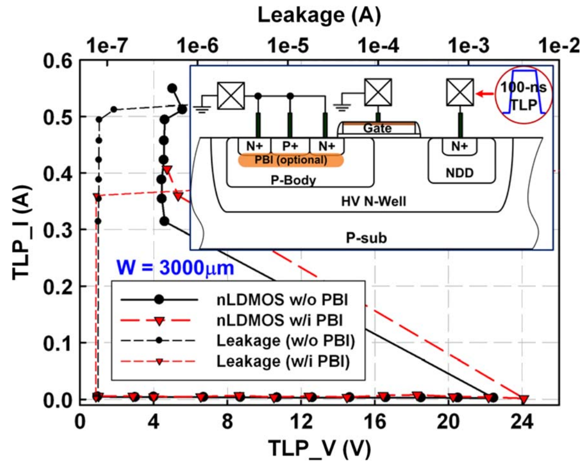

Fig. 1. TLP-measured I–V characteristics of 3000-μm LA-nLDMOS devices without and with the optional PBI implantation at the source side.

the studied LA-nLDMOS is 100 μm, and the gate terminals are externally grounded during ESD stresses. Leakage currents of all the TLP data in this letter were measured under the maximum normal circuit operating voltage, 16 V. To suppress the turn-on behavior of BJT inherent in nLDMOS, a highly doped optional P-type boron implantation (PBI) was introduced underneath the source N+ and P+ implantation, as shown in the inset of Fig. 1. From the measurement results in Fig. 1, trigger voltage (V_{t1}) of the medium-size nLDMOS is slightly increased from 22 to 24 V by the PBI implantation. However, the parasitic BJT is still triggered on at low TLP current (TLP_I) level. The TLP-measured secondary breakdown current (I_{t2}) of nLDMOS without and with the PBI implantation are 0.52 and 0.35 A, respectively. Both nLDMOS without and with the PBI implantation have almost the same HBM (MM) ESD protection level of 0.75 kV (50 V).

To effectively improve ESD robustness of medium-size LA-nLDMOS in the open-drain output buffer, the new proposed layout arrangement is shown in Fig. 2(a), in which polygate is bent to insert P+ slots. These P+ slots were connected to the grounded source through internal metal routing. To prevent P+ slots/HV N-Well junction from affecting the device breakdown voltage, P-Body was also bent with the polygate so that the P+ slots are wrapped up by the P-Body. Fig. 2(b) shows the device cross-sectional view along A-A′ line in Fig. 2(a). For LA-nLDMOS devices with the new proposed polybending layout arrangement, PBI implantation was not adopted to reduce the cost for production.

With the grounded P+ slots between the N+ drain (collector) and P+ source (base) of LA-nLDMOS, the P+ slots can shunt the avalanche-generated holes to ground during ESD stresses. The hole current to forward bias the P-Body underneath the N+ source is thereby substantially diminished. Turn-on behavior of BJT inherent in the LA-nLDMOS can, therefore, be effectively suppressed under ESD stresses.

From TLP measurement results for LA-nLDMOS with different slot spacings (d) shown in Fig. 3, the new proposed polybending layout arrangement can effectively suppress the snapback phenomenon of LA-nLDMOS. The avalanche-generated electrons and holes support the ESD discharging

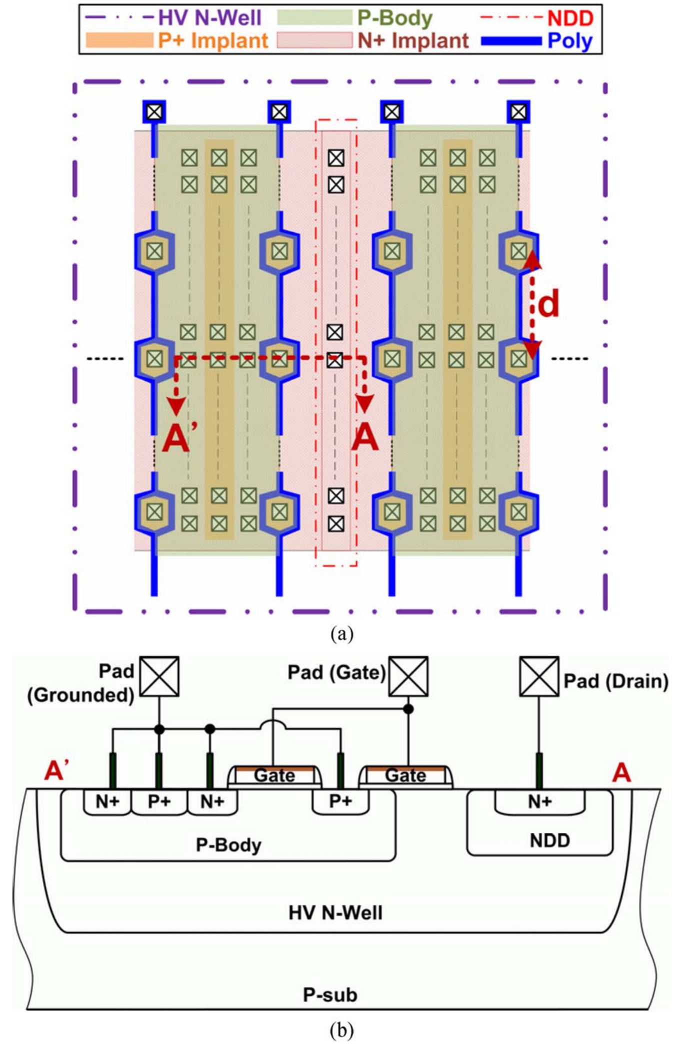

Fig. 2. (a) Layout top view of the new proposed nLDMOS with the polybending layout arrangement, and (b) device cross-sectional view along A-A′ line of the nLDMOS with polybending layout arrangement.

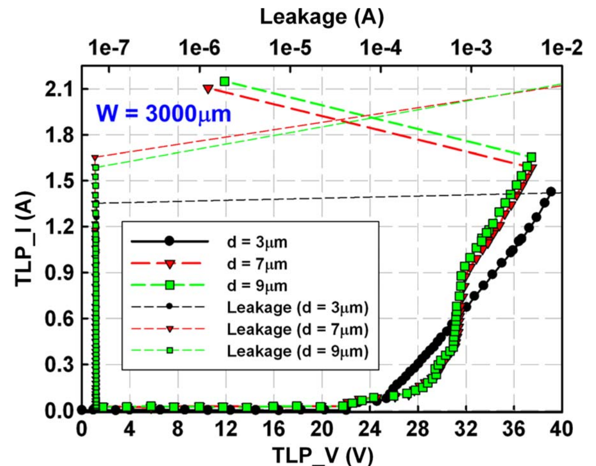

Fig. 3. TLP-measured I–V characteristics of LA-nLDMOS with polybending and different slot spacings. All LA-nLDMOS devices have the same effective width of 3000 μm.

current without inducing snapback of the LA-nLDMOS, which avoids nonuniform triggering of BJT and increases ESD robustness of the LA-nLDMOS. From the TLP measurement

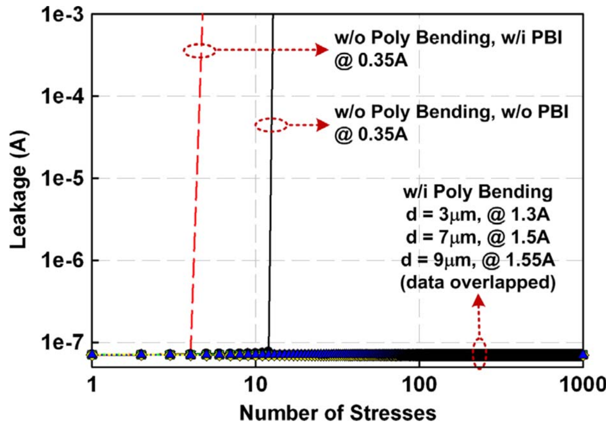

Fig. 4. Multiple iterative TLP stresses on LA-nLDMOS devices under fixed TLP current levels.

results in Fig. 3, LA-nLDMOS is burned out once snapback happens. When the spacing (d) between two adjacent P+ slots in the layout equals 3, 7, and 9 μm, the measured I_{t2} is 1.42, 1.58, and 1.65 A, respectively. A shift of turn-on resistance ($R_{\rm on}$) under TLP measurement is observed in Fig. 3 for $d = 7$ and 9 μm. Initially, when the avalanche breakdown happens at HV N-Well/P-Body junction, the larger d spacing mitigates the effectiveness of the grounded P+ slots to shunt avalanche-generated holes. For TLP_V higher than 28 V, a dramatically reduced $R_{\rm on}$ is therefore observed on LA-nLDMOS with $d = 7$ and 9 μm. With avalanche junction being shifted to drain region at high current level by the kirk effect [1], hole current is mainly absorbed by the P+ slots because the P+ slots are closer to the drain region than the P+ source (smaller resistance to ground). The spacing d therefore is found to have small impact on $R_{\rm on}$ when TLP_I is higher than 0.9 A. Comparable $R_{\rm on}$ for LA-nLDMOS devices are observed in Fig. 3 when TLP_I is larger than 0.9 A. Due to the smaller $R_{\rm on}$ at low TLP_I for LA-nLDMOS with d of 7 and 9 μm, these two LA-nLDMOS exhibit superior ESD robustness than that of LA-nLDMOS with d of 3 μm. Measured HBM (MM) ESD robustness for the new proposed LA-nLDMOS with d of 3, 7, and 9 μm are 2.5 (175), 2.75 (225), and 2.75 kV (225 V), respectively.

To examine the trigger voltage walk-in and the stability against multiple ESD stresses, LA-nLDMOS devices were stressed by consecutive TLP pulses under fixed TLP current levels. The leakage current under 16-V bias was monitored after every TLP stress, as shown in Fig. 4. For both LA-nLDMOS devices without polybending, the TLP test current was fixed at 0.35 A, which corresponds to their early snapback stages under TLP stresses. For LA-nLDMOS with polybending, TLP test currents were fixed at ~90% of the I_{t2} values measured in Fig. 3. Without the polybending structure, LA-nLDMOS with and without PBI showed leakage current over 1 μA after 5 and 13 stresses, respectively. However, all LA-nLDMOS devices with polybending layout can pass 1000 stresses without failure or trigger voltage walk-in. This has further verified the effectiveness of the new proposed polybending structure on improving ESD robustness of medium-size LA-nLDMOS.

Compared with the traditional LA-nLDMOS with PBI, the polybending layout with d of 3, 7, and 9 μm resulted in the degradation (increase) of 52.8% (63.1%), 17.7% (18.7%), and 12% (14.9%) on driving current (turn-on resistance) under the same gate bias of 3 V (16 V).

Recently, a dotted-channel structure was reported to substantially increase the SOA of LDMOS [8]. Such a dotted-channel structure was implemented on LDMOS with body nonisolated to the P-substrate. The dotted sites are inserted between the drain and source by increasing the length of polygate [8]. In some HV processes, the P-Body implantation is isolated from the P-sub by N-Well implantation or n-type epitaxial layer, and is fabricated after the formation of polygate [9]. The dotted channel scenario cannot be implemented in these technologies because the insertion of dotted sites by increasing the polygate length will make these dotted sites being placed within the HV N-Well instead of the P-Body. On the other hand, the new proposed polybending layout arrangement with grounded gate slots can still be applicable in those processes.

IV. Conclusion

Without using the ESD design guidelines and the power-rail ESD clamp circuit, it is difficult to design ESD-robust LA-nLDMOS in the open-drain output buffer. In this letter, a new layout arrangement for LA-nLDMOS with polybending has been proposed. The new proposed layout arrangement can effectively suppress the turn-on behavior of BJT inherent in nLDMOS by using the grounded P+ slots to shunt avalanche-generated holes, which has been successfully verified in a 0.5-μm 16-V BCD process. The TLP-measured secondary breakdown current for the gate-grounded LA-nLDMOS with a total channel width of 3000 μm was increased from 0.52 to 1.65 A. The HBM (MM) ESD protection level was improved from 0.75 (50) to 2.75 kV (225 V) by using the new proposed layout arrangement.

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