A Low-Power Self-Forward-Body-Bias CMOS LNA for 3–6.5-GHz UWB Receivers

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***Abstract*—A low-power low-noise amplifier (LNA) implemented in 0.18 μm CMOS technology utilizing a self-forward-body-bias (SFBB) technique is proposed for UWB low-frequency band system. By using the SFBB technique, it reduces supply voltage as well as saves additional bias circuits, which leads to low power consumption of 4.5 mW with low supply voltage of 1.06 V for two drain-to-source voltage drops. The complementary architecture and direct coupling technique between the first two stages also save bias circuits. The measurement result shows that the proposed LNA presents a maximum power gain of 16 dB with a good input impedance matching ($S11 < -12$ dB) and an average noise figure of 2.65 dB in the frequency range of 3–6.5 GHz.**

***Index Terms*—CMOS, forward body bias (FBB), low noise amplifier (LNA), low power, ultra-wideband (UWB).**

I. Introduction

ULTRA-WIDEBAND (UWB) communication techniques have attracted great interest in both academia and industry in the past few years for applications in short-range and high-speed wireless mobile systems, and that data rate of up to 480 Mb/s can be obtained using only the low-frequency band of UWB. One of the most critical blocks in a UWB receiver is the low-noise amplifier (LNA) because it needs to provide low noise and high gain with good input impedance matching over a broad frequency range. The LNA should consume as little dc power as possible while achieving acceptable performance for most applications.

Several CMOS LNA design techniques have been reported for wideband communication applications, which include current-reused [1], input-band-pass-filter wideband matching [2] and resistive feedback [3]. The current-reused LNA is composed of two common-source configuration stages under common-current structure that can save power consumption effectively. However, its chip area is large, since it usually contains many inductors for wideband response. In the input- band-pass-filter technique, the band-pass ladder filter is employed for wideband input matching. However, the parasitic resistance of the filter degrades the noise performance. The resistive feedback LNA increases the bandwidth at the cost of gain. Therefore, for higher gain, more amplifier stages are need, which increases the dc power consumption.

Manuscript received July 14, 2009; revised November 02, 2009. First published January 26, 2010; current version published February 10, 2010. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Grant 97-2219-E-009-012 and the National Chip Implementation Center (CIC).

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Digital Object Identifier 10.1109/LMWC.2009.2038526

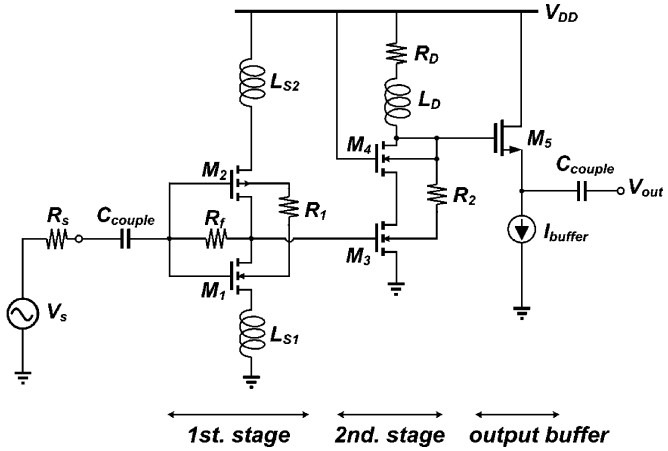

Fig. 1. Schematic of the proposed LNA with SFBB technique.

In this letter, we propose a low-power low-noise amplifier (LNA) utilizing self-forward-body-bias (SFBB) technique for wideband applications. The threshold voltage of the MOSFET can be lowered by means of SFBB technique, and then, with the same current amount, the higher supply voltage (1.8 V) supplied in the conventional LNAs in 0.18 μm CMOS technology is not needed. The supply voltage of the proposed LNA is only 1.06 V for two drain-to-source voltage drops of the MOSFETs. With regard to the design of system, biasing the bulk of the MOSFET by the self-bias technique saves dc power consumption as well.

II. Circuit Design and Analysis

The proposed low-power CMOS LNA for 3-6.5 GHz is shown in Fig. 1. It consists of two stages and the output buffer. The first stage uses the complementary architecture with the inductive source degeneration to amplify the received signal with wideband input impedance matching and low noise figure, and the second stage employs the cascode architecture to compensate the gain at the high frequency band of interest, 3–6.5 GHz.

The low power technique in our LNA design is by means of self-forward-body bias (SFBB). To differ from conventional FBB technique [4], as can be seen from Fig. 2, SFBB using an ultra-low power self-bias approach improves the conventional FBB technique that needs an additional bias circuit to supply the bulk terminal of the MOSFET for obtaining a forward bulk-source bias.

In the SFBB approach, as shown in Fig. 2(b), we can achieve ultra-low power self-bias loop since the P-N junction (parasitic diode) between the bulk and source in the MOSFET is treated

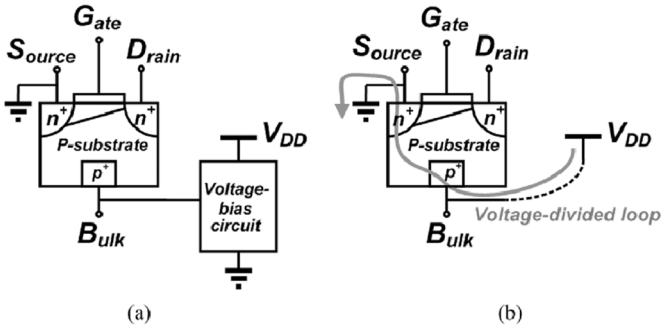

Fig. 2. (a) Conventional FBB with additional bias circuit. (b) Self-FBB.

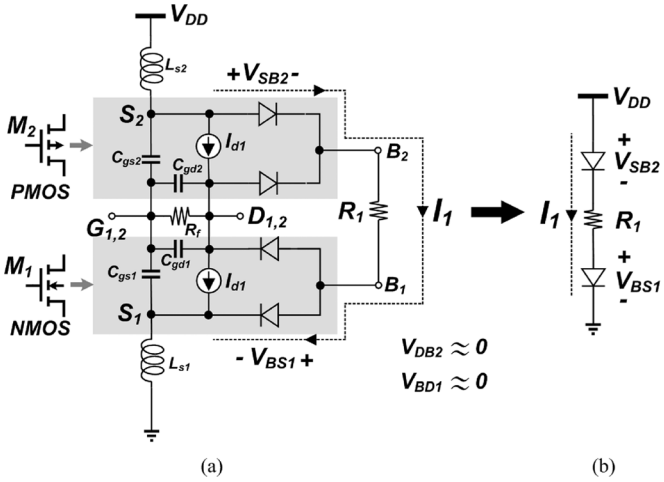

Fig. 3. (a) First stage with the MOSFETs model. (b) Self-bias voltage-divided loop.

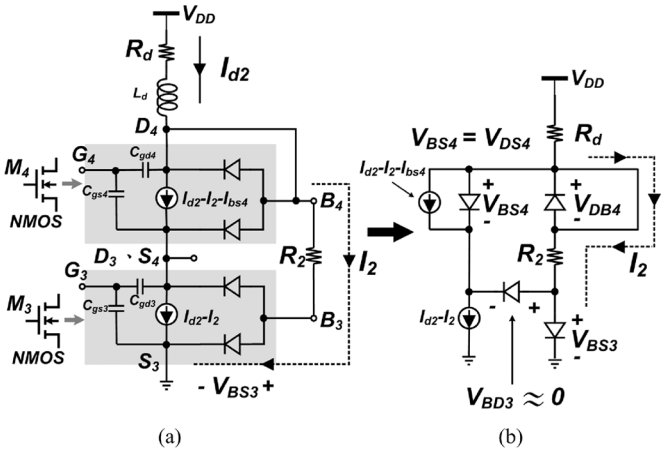

Fig. 4. (a) Second stage with the MOSFETs model. (b) Self-bias voltage-divided loop.

as a component in a voltage-divided loop, and only working in its cut-off region, in which the P-N junction voltage is lower than the cut-in voltage $V_{\mathrm{cut,in}}$ (typically about 0.5 V). The well-known P-N junction I-V characteristic equation is given by

$$I_{\mathrm{PN}} = I_S\left(e^{\frac{V_{\mathrm{PN}}}{\eta V_T}} - 1\right) \tag{1}$$

where η is the ideality factor, V_T the thermal voltage, and I_S denotes the reverse-bias leakage current. In the cut-off region ($0 < V_{\mathrm{PN}} < V_{\mathrm{cut,in}}$), the current through the P-N junction is very small (about a few μA), that leads to a self-bias loop with ultra-low power consumption (about a few μW).

The ultra-low power self-bias loop employed in the two stages of the proposed LNA is analyzed and evaluated as follows. In Fig. 3(a), the first stage using the complementary architecture that consists of an N- and a P-MOSFET is shown. In order to provide the bulk-source P-N junction voltage (V_{BS1} and V_{SB2}) of both transistors, M_1 and M_2, to form a voltage-divided loop with forward bias, a resistor R_1 is employed to connect between their bulk terminals. To be simple, the self-bias voltage-divided loop is individually shown in Fig. 3(b). In this loop, R_1 is properly selected to yield the bulk-source P-N junction voltage drops of both transistors operating in the cut-off region that can achieve ultra-low power self-bias loop. The formula of R_1 is derived as follows, which starts with the voltage equation of the self-bias voltage-divided loop, $V_{\mathrm{DD}} = V_{\mathrm{BS1}} + V_{\mathrm{SB2}} + I_1 R_1$. According to (1), the loop current I_1 can be expressed in terms of V_{BS1} or V_{SB2}

$$I_1 = I_{S1}\left(e^{\frac{V_{\mathrm{BS1}}}{\eta V_T}} - 1\right) \text{ or } I_1 = I_{S2}\left(e^{\frac{V_{\mathrm{SB2}}}{\eta V_T}} - 1\right). \tag{2}$$

Here, I_{S1} and I_{S2} denote the reverse-biased leakage current of the bulk-source P-N junction of the N- and P-MOSFET in the first stage, respectively. Then, substituting (2) into the voltage equation of the self-bias voltage-divided loop, we obtain

$$V_{\mathrm{DD}} = V_{\mathrm{BS1}} + V_{\mathrm{SB2}} + I_{S1}\left(e^{\frac{V_{\mathrm{BS1}}}{\eta V_T}} - 1\right) R_1 \tag{3}$$

thus

$$R_1 = \frac{V_{\mathrm{DD}} - V_{\mathrm{BS1}} - V_{\mathrm{SB2}}}{I_{S1}\left(e^{\frac{V_{\mathrm{BS1}}}{\eta V_T}} - 1\right)}. \tag{4}$$

The second stage uses the cascode architecture shown in Fig. 4. Similarly, in order to form a self-bias loop, we exploit a resistor R_2 to connect between their bulk terminals. The principle and analysis method of the SFBB technique in the second stage is similar to that of the first stage, so we only show what the value of R_2 we need while the bulk-source P-N junction voltage, V_{BS3}, is operating at cut-off region, and V_{BS4} is equal to V_{DS4} about 0.45 V. The design values of R_1 and R_2 are 7 KΩ and 25 KΩ, respectively.

$$R_2 = \frac{V_{\mathrm{DD}} - I_{d2}R_d - V_{\mathrm{BS3}}}{I_{S3}\left(e^{\frac{V_{\mathrm{BS3}}}{\eta V_T}} - 1\right)}. \tag{5}$$

III. Experimental Results

The proposed LNA has been fabricated in TSMC 0.18 μm 1P6M CMOS process. The die micrograph with a chip area of 0.97 mm $\times$ 0.64 mm including pads is shown in Fig. 5. The measured S-parameters and noise figure (NF) of the proposed

TABLE I
MEASURED PERFORMANCE SUMMARY AND COMPARISON

Ref.	CMOS Technology	3-dB BW (GHz)	S11 (dB)	Gain* (dB)	NF (dB)	IIP3 (dBm)	supply voltage (V)	Power (mW)
This work	**0.18-μm**	**3.0−6.5**	**< −12**	**16**	**1.9−3.4**	**−13 @ 4 GHz**	**1.06**	**4.5**
[5]	0.18-μm	2−8.5	< −10	13	4.1−4.8	−13.5 @ 3 GHz	1.8	9.3
[6]	0.18-μm	3−5	< −10	13	4.6−5	+0.1 @ 4 GHz	1.8	14.6
[7]	0.18-μm	3−6	< −8.7	13.6	3.6−5	−5 @ 4 GHz	1.8	12.5
[8]	0.13-μm	2−4.6	< −10	9.5	3.5−6.6	−0.8 @ 3 GHz	1.5	16.5
[9]	90-nm	0.1−8	< −10	16	3.4−5.8	−9	1.4	16

* Maximum power gain.

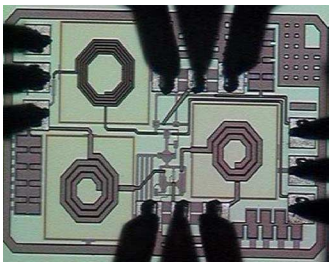

Fig. 5. Die micrograph of the proposed LNA.

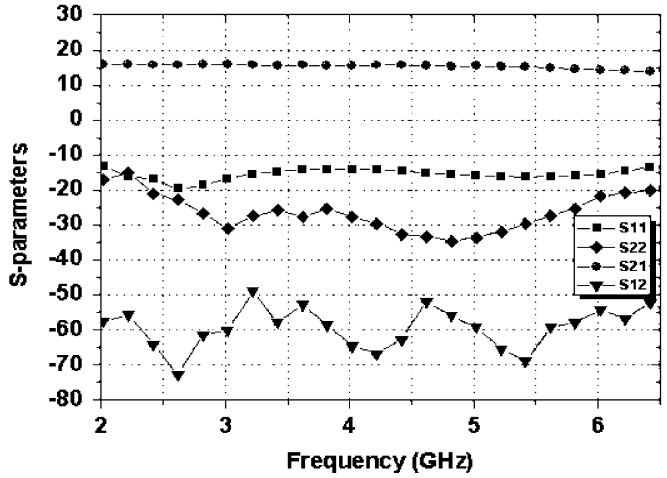

Fig. 6. Measured S-parameters of the proposed LNA.

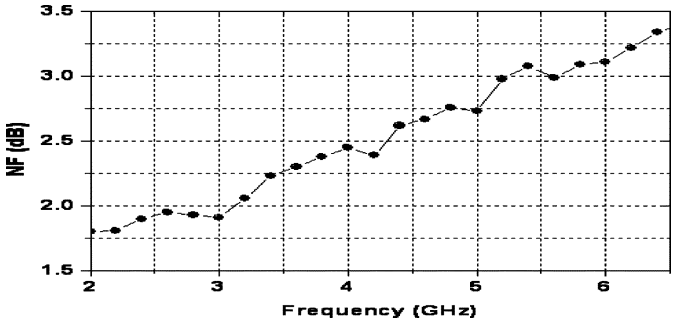

Fig. 7. Measured noise figure of the proposed LNA.

LNA are shown in Figs. 6 and 7, respectively. The maximum measured power gain is 16 dB with −3 dB bandwidth from 3.0 to 6.5 GHz, and S11 and S22 are better than −12 dB and −20 dB, respectively. The proposed LNA uses two inductive source degenerations in parallel to achieve a low noise figure of 1.9–3.4 dB in the frequency range 3–6.5 GHz. The third-order input intercept point (IIP3) is measured by applying two-tone test with 1-MHz spacing. The measured IIP3 is −13 dBm at 4 GHz. The LNA core consumes only 4.5 mW power from a 1.06 V supply voltage. A summary of the performance of the LNA is given in Table I [5]–[9].

IV. CONCLUSION

A low-power LNA for wideband applications has been demonstrated in 0.18 μm CMOS process. By utilizing SFBB techniques, we can achieve a low power consumption of 4.5 mW with low supply voltage of 1.06 V for two drain-to-source voltage drops as well as save additional bias circuits.

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