A New Simulation Model for Plasma Ashing Process-Induced Oxide Degradation in MOSFET

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Abstract— **Plasma ashing process-induced oxide damage is studied quantitatively in this paper. To simulate thin gate-oxide damage due to plasma ashing process, a new equivalent circuit model is proposed by including a differential capacitance, a parasitic resistance, an offset flatband voltage, and the effects of feedback on the interface-state and trapped oxide charge densities generated during plasma ashing process. According to this new model, computation of gate oxide charging current is performed by correlating to the latent interface-state density. The test n-MOSFET devices including different antenna-ratios are measured, and excellent agreement is obtained as compared with measured results. Moreover, the deficiency of the previous model is stated and compared. In addition, the effects of substrate doping concentration on plasma-induced oxide damage are also investigated as well as those of plasma ion density, plasma uniformity, thin gate-oxide thickness. Therefore, the relationships between interface states/oxide traps and antenna ratio are linked to provide a guideline for circuit designers and the plasma ashing process-induced damage can be predicted.**

I. Nomenclature

$J_t(t)$	Gate current density, including gate displacement current and Fowler–Nordheim tunneling current.
J_g	Fowler–Nordheim tunneling current density.
$C_{\rm ox}$	Gate oxide capacitance per unit area.
C_p	Parasitic capacitance per unit area, composed of Metal I, Metal II, poly-Si, etc.
$C_d(t)$	Substrate depletion capacitance per unit area.
R	Bulk series resistance.
V_{FB}	Flatband voltage.
V_{sh}	Potential barrier for electron current; sheath potential.
V_p	Plasma potential.
$V_1(t)$	Potential drop from the gate to the bulk.
$V_g(t)$	Potential across the gate oxide.
$V_s(t)$	Potential across $C_d(t)$.
E_c (E_a)	Cathode (anode) electric field.
E_m	Electric field in the middle region.
A_p	Area of parasitic capacitance, composed of Metal I, Metal II and poly-Si etc.; antenna area.
$A_{\rm wafer}$ (A_G)	Area of the wafer exposed in plasma ambient (gate oxide).
u_B	Bohm velocity of plasma ions $(= (qT_e/m_i)^{1/2})$.
u_e	Electron mean thermal velocity $(= (8qT_e/\pi m)^{1/2})$.
$\epsilon_{\rm ox}$	Permittivity of SiO_2.
N_t (N_{it})	Pre-existing trap (interface-state) density.
$n_t^-(t)$ ($n_t^+(t)$)	Electron (hole) trapped density.
n_{it}	Interface-state density.
x_n (x_p)	Distance from Si substrate to electron (hole) trap centroid.
$g(J_g)$	Generation rate of trapped charge.
σ (σ_g)	Capture cross section of the pre-existing traps (the generated traps).
σ_{it}	Capture cross section of the pre-existing interface states.
m (m_i)	Free electron (plasma ion) mass.
m^*	Effective mass of the tunneling electrons in oxide (0.5 m).
η	Trapping efficiency.
ϕ_b	Si-SiO_2 barrier height.
N_{AB}	Substrate doping concentration.
q	Elementary charge.
$T_{\rm ox}$ (T_f)	Gate(field) oxide thickness.
k (h)	Boltzmann (reduced Planck) constant.
T_e	Electron temperature.

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II. Introduction

PLASMA processes are very important in modern IC fabrication for polysilicon etching, oxide and metal etching, and photoresist stripping. However, potential is built up on the exposed wafer surface by collected charges in plasma ambient, resulting in electrical stress on thin gate oxide. This problem becomes serious in multi-layer metal technologies because the charges introduced by plasma process can be built up through not only floating polysilicon but also polysilicon electrically connected to interconnection metal/polysilicon lines. Moreover, the exposed wafer in plasma environment will suffer from ions bombardment, resulting in physical damage. Many evidences have shown that the plasma process-induced oxide damage occurs only in nonuniform plasma ambient [1]–[4], where plasma charges are collected by the top surface of the gate or metal/polysilicon patterns during the photoresist ashing and collected by the sidewall of gate/interconnection metal layer or by the surfaces that are not covered by photoresist during plasma etching process or plasma overetching. The collected charges will build up high potential on thin gate oxide, generating interface states and oxide traps, and degrading breakdown voltage of thin gate oxide [5]–[9].

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Some researchers had proposed the equivalent circuit model to simulate the charging damage generated by plasma ashing process [10]–[12]. However, it is found that the gate-oxide current calculated by the previous model is overestimated due to the lack of consideration for the feedback effects on the interface-state and trapped oxide charge densities generated during plasma ashing process. Moreover, the substrate resistance and the flatband voltage were neglected in the previously proposed models. It is shown that there exists a voltage drop in the substrate when the semiconductor surface is in the depletion mode, and a smaller voltage drop when the semiconductor surface is in the accumulation mode.

In this paper, an equivalent circuit model to quantitatively simulate the charging and discharging thin gate oxide is proposed. In our plasma ashing model, the differential capacitance, the substrate resistance, the flatband voltage, and the effects of feedback on the interface-state and trapped oxide charge densities generated during plasma ashing process are considered in the equivalent circuit model and the simulated results for these damages are presented. The Fowler–Nordheim (FN) constant-current stress is used to release the latent annealed interface states and oxide traps, and the charge-pumping method is used to measure the generated interface states and oxide traps. Consequently, the interface states and oxide traps related to different antenna ratios are investigated, and the simulated gate-oxide current and measured results will be correlated.

III. Surface Charging Model

A. Plasma Charging Model

During plasma ashing processing, the gate electrode will be charged due to the local unbalanced ions and the electron current over the RF cycle in nonuniform plasma environment and a potential will be built up on the gate electrode. This high gate voltage will force anomalous gate-oxide current flowing through the thin gate oxide, which would deteriorate the thin gate oxide severely. In nonuniform plasma ambient, the plasma current seen by a wafer placed on the electrode can be expressed by [12], [13]

$$J_i = 0.6 q n_i u_B \tag{1}$$

$$J_e = -0.25 q n_e u_e \ \exp(-qV_{sh}/kT_e). \tag{2}$$

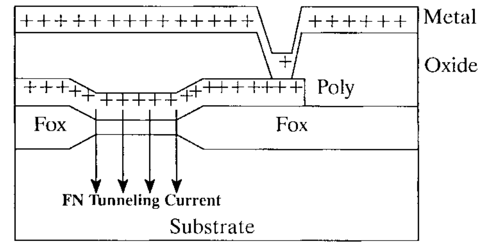
Multiplied by the area of the wafer exposed in plasma ambient, the plasma charging current $I_p(t)$ can be rewritten as

$$I_p(t) = I_i - I_e \ \exp(qV_1(t)/kT_e) \tag{3}$$

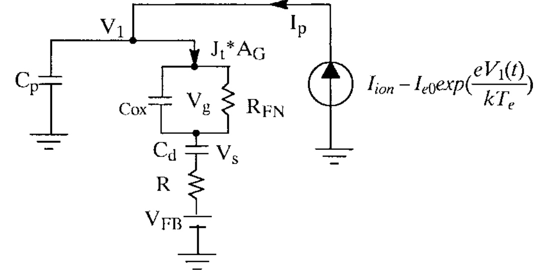
where $I_i = A_{\text{wafer}} J_i; I_e = A_{\text{wafer}} J_e \ \exp(-qV_p/kT_e)$.

B. The Equivalent Circuit Model

The cross section of the wafer in plasma ambient is shown in Fig. 1(a) and the equivalent circuit is shown in Fig. 1(b). Note that the testing samples are "area" type and, therefore, this model does not take the electron shading effect into account [14]. Using KCL and KVL for the circuit shown in Fig. 1(b),



(a)



(b)

Fig. 1. (a) The cross section of the silicon wafer during plasma ashing process. (b) The new equivalent circuit during plasma ashing process.

we obtain

$$I_p(t) = J_t(t)A_G + A_p C_p \frac{d}{dt} V_1(t) \tag{4}$$

$$J_t(t) = J_g + C_{\text{ox}} \frac{d}{dt} V_g(t) \tag{5}$$

$$J_t(t) = \frac{d}{dt} C_d(t) V_s(t) \tag{6}$$

$$V_1(t) = V_g(t) + V_{FB} + V_s(t) + RA_G J_t(t) \tag{7}$$

where $C_d(t)V_s(t) = Q_D + Q_{ss}, Q_D$ is the depletion region charges per unit area, and $Q_{ss} = qn_{it}$. Note that the flatband voltage is the fresh flatband voltage. The plasma-induced oxide-trapped and interface-state charges are excluded from the fresh flatband voltage. Therefore, the fresh flatband voltage V_{FB} during plasma process is kept constant.

The interface states and oxide traps will be generated by hot electrons through breaking the weak bonds at the Si/SiO_2 interface and the weak spots in the oxide. If the gate-oxide current is large enough, not only the latent oxide traps and Si/SiO_2 interface states could be released but also the extra oxide traps and interface states could be generated. Due to the existence of electron traps and hole traps in the gate oxide, the potential distribution in the gate oxide will be perturbed and this will then influence the gate current in the next lapse. The potential distribution in the gate oxide is shown in Fig. 2.

It is shown that the hole traps would lower the potential near the cathode and the electron traps would raise the potential near the anode. Therefore, by Gauss's Law the electric fields across the oxide are expressed as [15], [16]

$$E_c(t) = \frac{V_g(t)}{T_{\text{ox}}} - \frac{qn_t^-(t)}{\epsilon_{\text{ox}}}\left(1 - \frac{x_n}{T_{\text{ox}}}\right) + \frac{qn_t^+(t)}{\epsilon_{\text{ox}}}\left(1 - \frac{x_p}{T_{\text{ox}}}\right) \tag{8}$$

$$E_m(t) = E_c(t) - \frac{qn_t^+(t)}{\epsilon_{\text{ox}}} \tag{9}$$

$$E_a(t) = E_m(t) + \frac{qn_t^-(t)}{\epsilon_{\text{ox}}}. \tag{10}$$

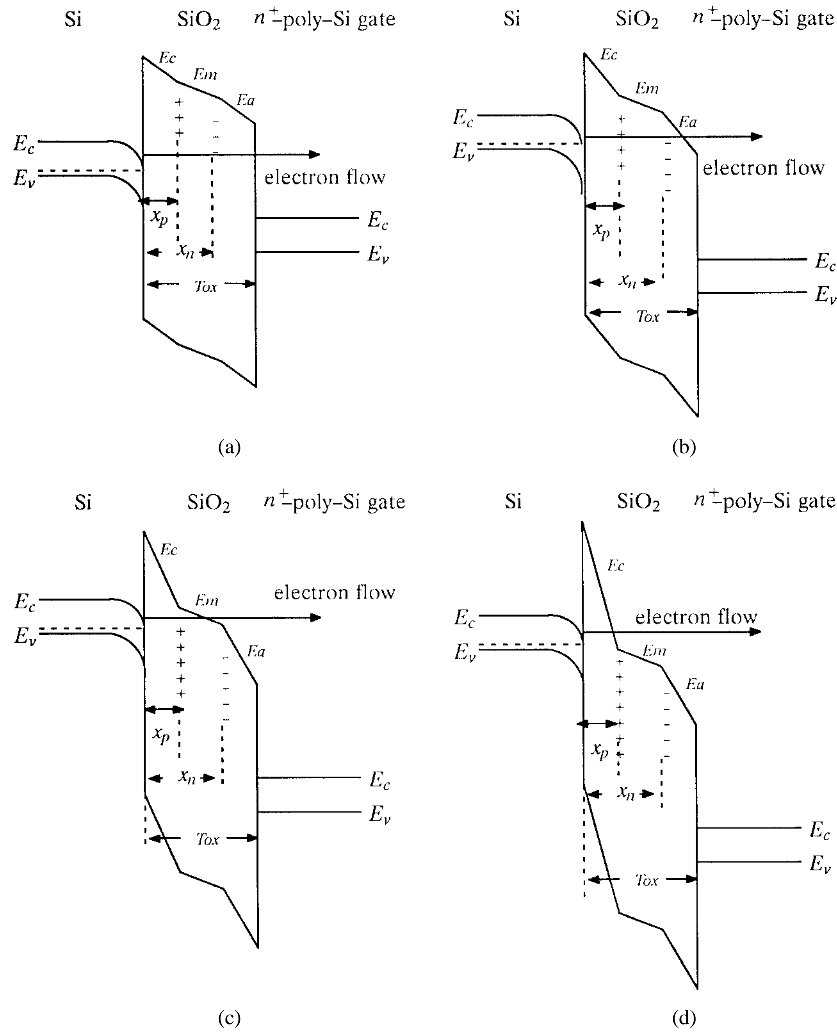


Fig. 2. The MOS energy diagrams showing the existence of electron traps and hole traps.

Note that the image-force lowering effect on the barrier height is also considered. The FN tunneling current density across the potential barriers shown in Fig. 2(a)–(d) has the following form:

$$J_g(t) = \frac{q^2 m E_c(t)^2}{16\pi^2 hm * \phi_b(E_c)} \cdot T_p(t) \tag{11}$$

and the tunneling probability $T_p(t)$ for Fig. 2 can be calculated by using the WKB approximation in [14].

We assume that $n_t^-(t)$ and $n_t^+(t)$ are equal to zero at initial, i.e., the test samples were annealed, $J_g(0)$ could be determined by solving (4)–(11). Once J_g is determined, $n_t^-(t)$ and $n_t^+(t)$ can be resolved by using the electron trapping model [15], [17]

$$\begin{aligned} n_t^-(t) =& N_t(1 - e^{-\int_0^t \sigma J_g\, dt/q}) + 1/q \int_0^t g(J_g) J_g(t)\, dt \\ & - \frac{g(J_g)}{\sigma_g}(1 - e^{-\int_0^t \sigma_g J_g\, dt/q}). \end{aligned} \tag{12}$$

The density of the trapped holes near the cathode is given by

$$n_t^+(t) = \eta/q \int_0^t J_g(t)(M_w - 1)\, dt \tag{13}$$

where the multiplication factor in the weak area M_w can be expressed as

$$M_w = 1 + \int_{T_t}^{T\text{ox}} \alpha(E)\, dx \tag{14}$$

and the impact ionization coffcient $\alpha(E)$ has the following form:

$$\alpha(E) = \alpha_0 e^{-H/E}. \tag{15}$$

Note that $H = 78$ MV/cm and $\alpha_0 = 3.3 \times 10^6$ at room temperature [15]. The interface-state density can also be determined by the first-order kinetics

$$n_{it}(t) = N_{it}(1 - e^{-\int_0^t \sigma_{it} J_g\, dt/q}). \tag{16}$$

As n_t^-, n_t^+, and n_{it} are determined, J_g is then resolved in the next lapse from (4) to (11), and so on and so forth. The surface potential and the gate-oxide current of the wafer exposed in nonuniform plasma ambient could then be calculated during plasma processing. The rest of parameters used are listed in Table I. Some parameters listed in Table I are selected to be the same as previous papers [12], [16]. The ion current density is measured by using probe technique [12]. The photoresist was

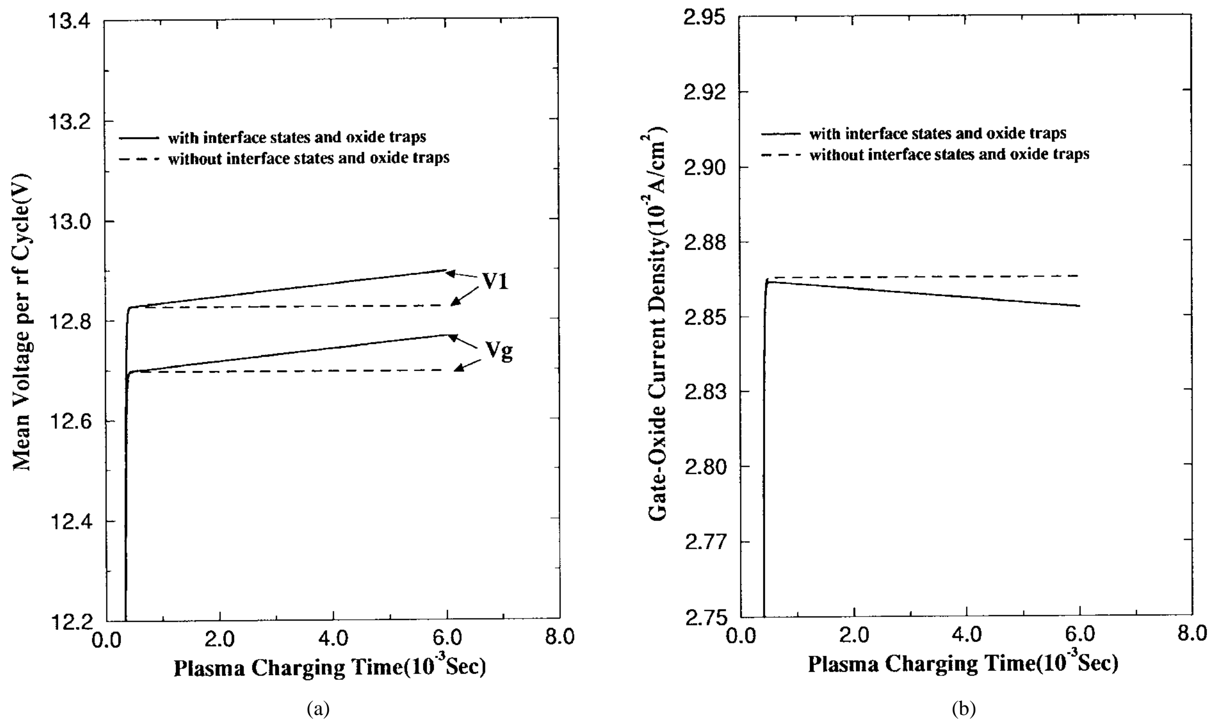


Fig. 3. (a) The mean voltage per rf cycle during plasma ashing process. (b) The mean gate-oxide current density per rf cycle during plasma ashing process.

TABLE I
THE PARAMETERS USED IN OUR MODEL

$\phi_b(eV)$	3.15	$J_e(A/cm^2)$	4.4×10^{-6}
$X_n(A^0)$	85	$T_e(eV)$	6
$X_p(A^0)$	25	$N_t(cm^{-2})$	6.3×10^{12}
$T_{ox}(A^0)$	140	$N_{it}(cm^{-2})$	1.0×10^{13}
$T_f(A^0)$	7500	$\sigma_{it}(cm^2)$	1.5×10^{-17}
$V_{FB}(V)$	-0.906	$\sigma(cm^2)$	4.7×10^{-17}
$R_B(\Omega - cm)$	3.5	$\sigma_g(cm^2)$	1.5×10^{-15}
$J_i(A/cm^2)$	1.8×10^{-4}	g	3.0×10^{-7}

removed by $O_2 + N_2$ plasma asher in our studies and the RF power of this asher is 400 W. Note that the plasma damage of ashing process is significant in the overetch step rather than main step, owing to the large exposed area of polysilicon pad in plasmas.

IV. RESULTS AND DISCUSSION

As the fabricated wafers are exposed in plasma ambient, these wafer surfaces are charged by plasma charging current initially, and then the wafer surface potential will rise and it will shrink the plasma sheath, in turn lowering the plasma charging current. Furthermore, due to the increasing potential of the wafer, the gate-oxide current would increase. While the gate-oxide current is equal to the plasma charging current, the wafer surface potential will be saturated as the gate-oxide current. The simulated gate voltage and gate-oxide current are shown in Fig. 3(a)–(b). The gate-oxide current density will gradually decrease due to accumulated trapped electrons during cycle by cycle. However, the potential across the oxide will gradually increase (making the slight damage) and becomes constant (steady state, making the most serious damage due to the largest electric field) during the plasma current charging in each cycle. Therefore, the plasma-induced damage is almost caused by the steady-state charging current in each cycle and the used steady-state value is acceptable. The gate-oxide current density shown in Fig. 3 is the steady-state value for each cycle and the transient behavior isn't shown in this figure. The electron traps, hole traps and interface states generated during plasma process are shown in Fig. 4. From Fig. 4, one can see that there exist a large number of generated electron traps. These oxide-trapped electron charges would impede gate-oxide current passing through oxide further and cause the gate-oxide current decrease, as shown in Fig. 3(b). To reach the saturation condition (i.e., the plasma charging current = gate-oxide current), the potential across the gate oxide (V_g) should increase further to force electrons passing through the gate oxide.

To correlate the simulated results with the measured results, the following experiment was performed. To release the latent gate oxide traps and Si/SiO_2 interface states, the constant-current stress with current density of 1 mA/cm^2 and stress time of 1200 s is used. The n-channel MOSFET's with four antenna ratios (10, 100, 400, 1000) are measured. The gate-oxide thickness is 14 nm, the channel width is 5 μm, the channel length is 0.8 μm, and the substrate resistivity is about 2.5–3.5 Ω·cm. To characterize the released gate oxide traps and Si/SiO_2 interface states, the charge-pumping method is adopted. The curves of interface states versus different antenna ratios are shown in Fig. 5, in which the strong

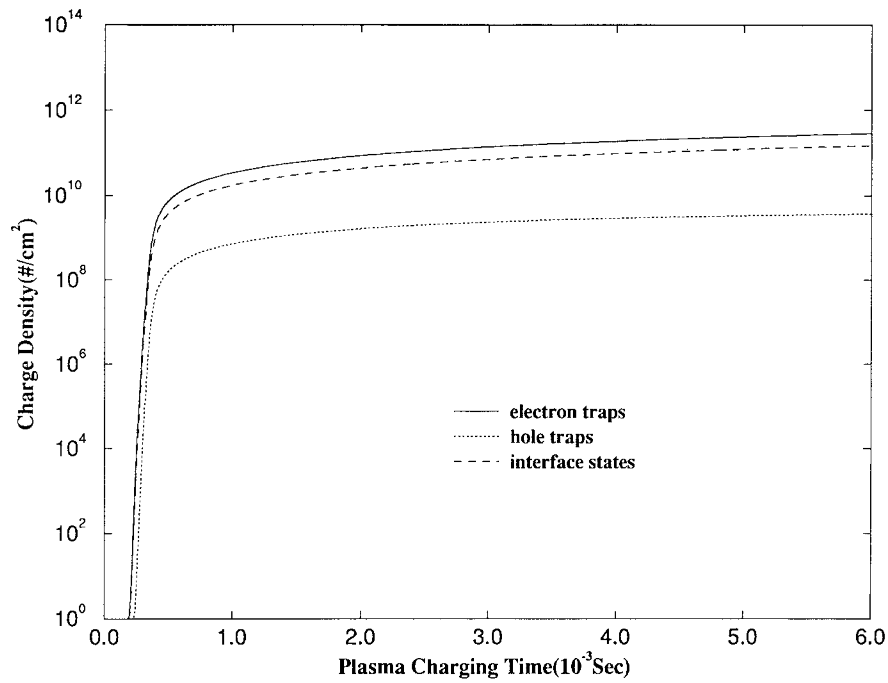


Fig. 4. The electron/hole traps in the oxide and Si/SiO_2 interface states generated during plasma ashing process.

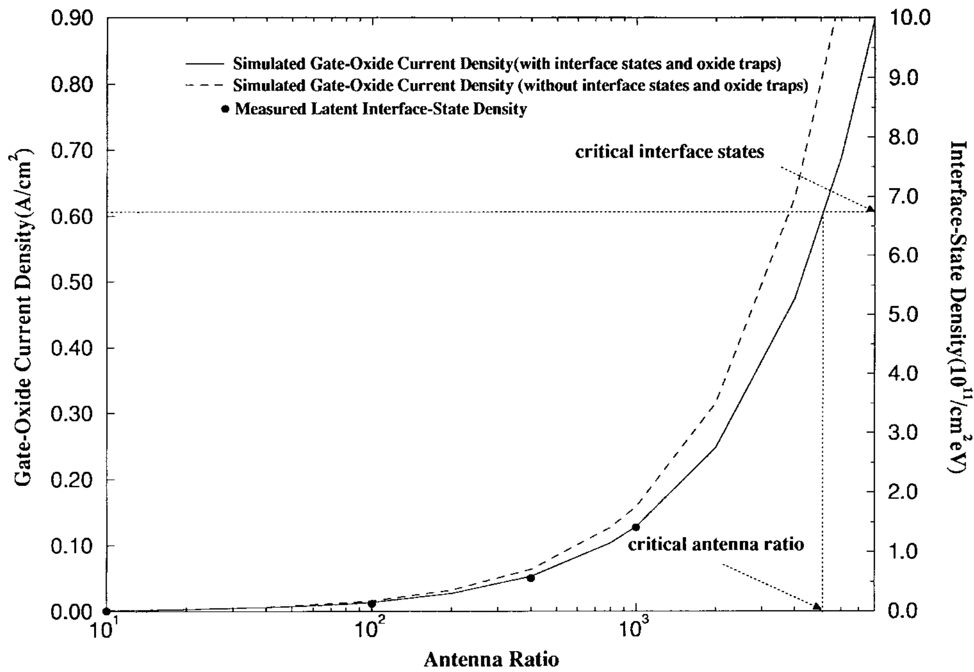


Fig. 5. The correlation of the simulated oxide current density to the measured latent interface-state density for diffferent antenna ratios, and the synthetic guideline for predicting the gate oxide reliability from our simulated results.

correlation of the calculated time-averaged oxide current to measured Si/SiO_2 interface states is obvious with a constant fitting number of about 9.0×10^{-13}. Therefore, the proposed physical model could provide the design rules for layout designer. For example, one can measure the interface states and obtain the correlation curve between antenna ratio and latent interface states. The simulated time-averaged gate-oxide current is then fitted and the fitting parameter is obtained. The critical interface states can then be extrapolated, and the critical antenna ratio is obtained. The synthetic guideline is indicated in Fig. 5. Note that the critical interface-states is defined as one which causes 10% degradation of MOS device transconductance. From Fig. 5, if the effect of feedback on interface states and trapped electrons is not taken into account, the critical antenna ratio would be underestimated due to the overestimated gate-oxide current density. Therefore, the feedback effect should be taken into consideration for the accurate prediction of the critical antenna ratio.

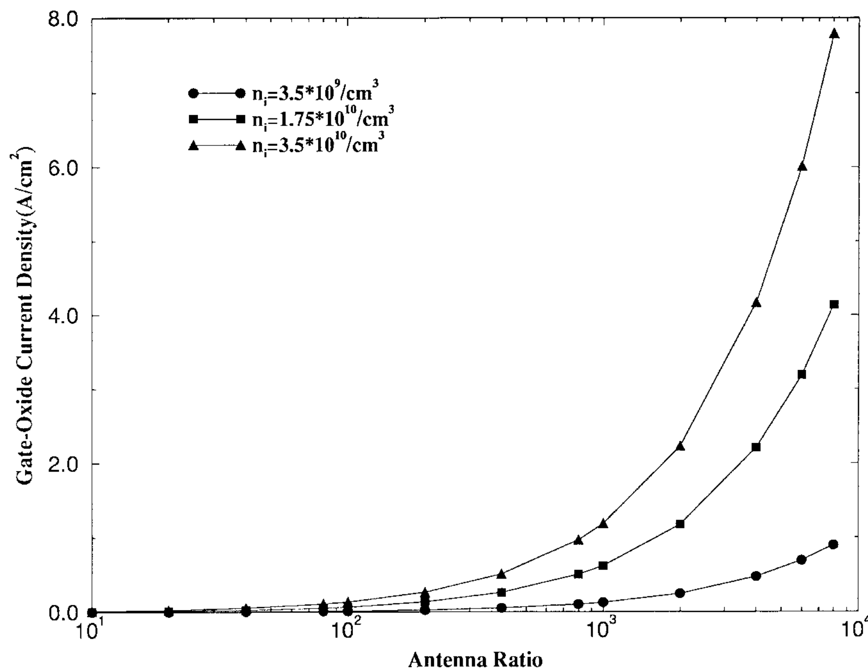


Fig. 6. The simulated gate-oxide current densities related to different antenna ratios for different ion densities.

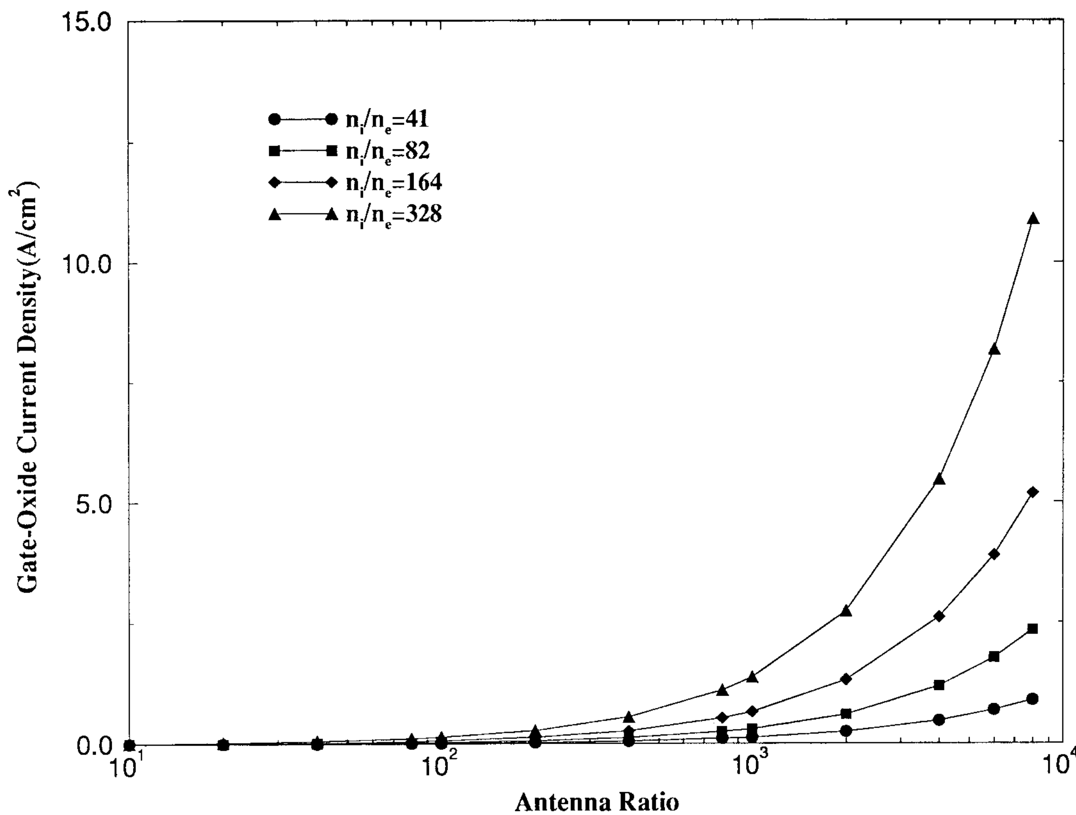


Fig. 7. The simulated gate-oxide current densities related to different antenna ratios for different plasma uniformities.

Moreover, the dependences of different process parameters on gate-oxide current and plasma-induced oxide damage are investigated, which include plasma ion density, plasma uniformity, gate-oxide thickness, and substrate doping concentration.

A. Plasma Ion Density

While the MOS device is scaled down to the deep submicron era, plasma ion density needs to be increased to delineate fine line pattern. According to the simulated results shown in Fig. 6, the gate-oxide current would increase if plasma ion density increases. Note that the plasma uniformity, i.e., n_i/n_e, is maintained to be constant, and the only change is the plasma density. Therefore, damage due to plasma process used in VLSI manufacturing becomes more serious and how to eliminate this damage also becomes more important.

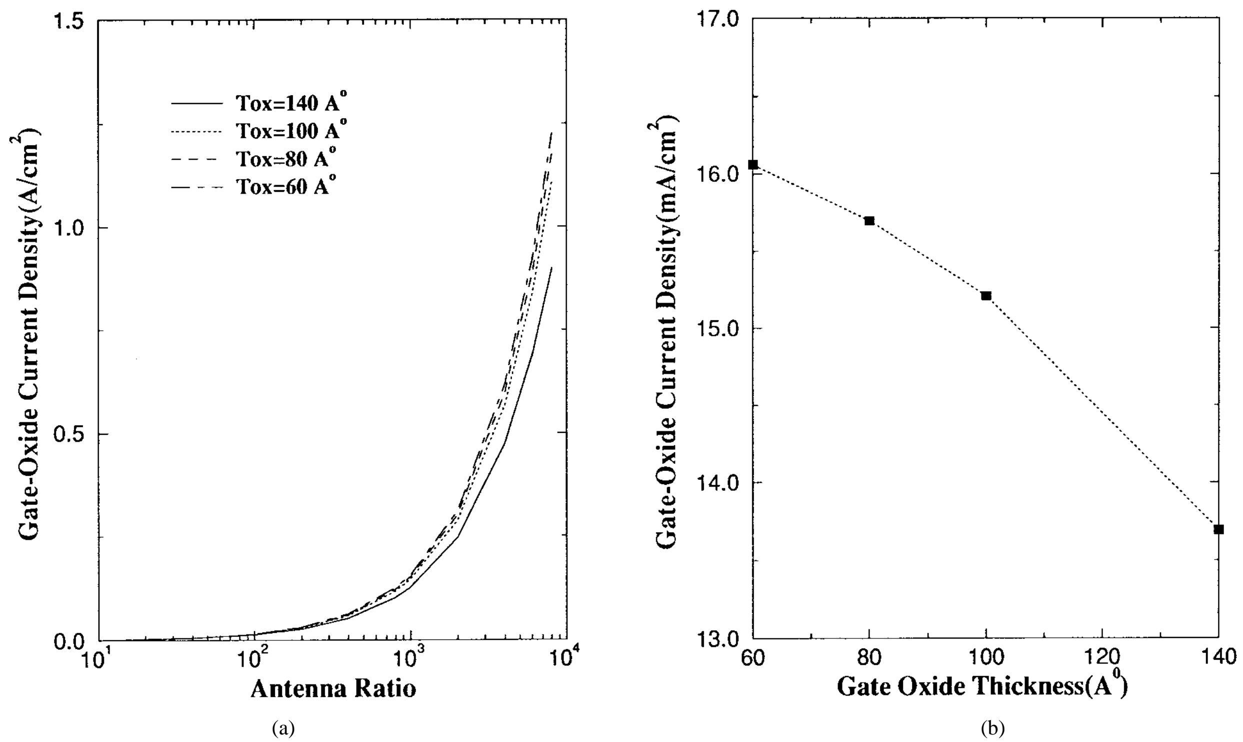


Fig. 8. (a) The simulated gate-oxide current densities related to different antenna ratios for different gate-oxide thicknesses. (b) The gate-oxide current density related to the gate oxide thickness. The antenna ratio used is 100.

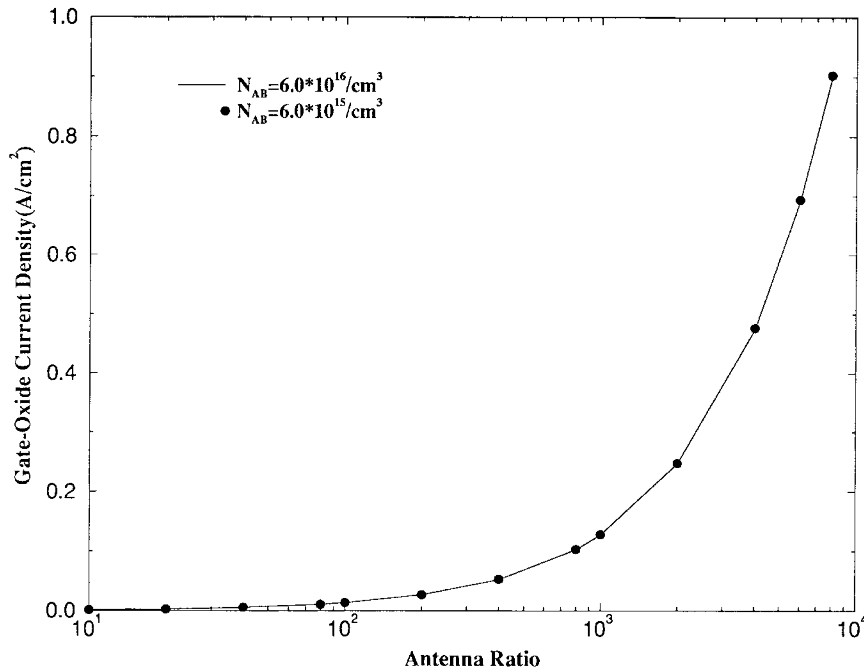


Fig. 9. The simulated gate-oxide current densities related to different antenna ratios for different substrate doping concentrations.

B. Plasma Uniformity

Plasma process-induced oxide damage occurs only in nonuniform plasma ambient, and different plasma uniformities cause different degrees of damage. We define plasma uniformity as n_i/n_e and observe the relationship between plasma damage and plasma uniformity. Note that the electron density is assumed to be constant, and the plasma ion density is changed. As shown in Fig. 7, the plasma uniformity influences the gate-oxide current significantly. How to maintain plasma uniformity of the etcher/asher becomes very important.

C. Gate-Oxide Thickness

As the gate-oxide thickness is scaled down, the simulated oxide current during plasma processing becomes larger, as

shown in Fig. 8(a). Note that the centroid of trapped holes is set to be 2.5 nm and the centroid of trapped electrons is evalued by $0.6T_{\mathrm{ox}}$ as used in [15]. For thinner gate oxide (<14 nm), the above method can be used. The calculated gate-oxide current shown in Fig. 8(b) would be saturated as the gate-oxide thickness becomes thinner, which agrees well with the result reported previously [10]. Note that the field oxide thickness is also scaled with the gate-oxide scaling in our simulated results.

D. Substrate Doping Concentration

From Fig. 9, we can see that the increasing substrate doping concentration has little effect on the gate-oxide current during plasma processing. One can see that the gate-oxide voltage is about 8–16 V, depending on the gate-oxide thickness, and the sum of the voltage across the substrate depletion capacitor and the substrate is merely 1–2 V. Therefore, the variation of substrate doping concentration only slightly affects the change of plasma damage.

From our model, not only the plasma ion density but also the plasma uniformity play a major role in causing the plasma-induced oxide damage. The effect of gate-oxide thickness in causing the plasma-induced oxide damage would be saturated while the gate-oxide thickness is scaled. The surface potential variation due to substrate doping concentration variation during plasma processing is small, and the variation very slightly affects the gate-oxide current. Therefore, in addition to improving the plasma process [18], [19], realizing uniform plasma ambient is the major issue in reducing the plasma process-induced oxide damage.

V. Conclusion

The plasma ashing process-induced oxide damage has been extensively studied. In our models, the gate-oxide current density, interface-state and oxide-trapped charges can be accurately calculated by considering the feedback effects, the substrate resistance and the flatband voltage. Owing to the correct calculation of interface-state and oxide-trapped charges, the devices fabricated in plasma ambient can be well-characterized prior to breakdown. Moreover, the influences of some parameters adopted in deep submicron fabrication are also investigated and the trends are presented. Therefore, our simulator is useful in accurately predicting the plasma ashing process-induced damage.

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Ching-Yuan Wu (S'72–M'75), for a photograph and biography, see this issue, p. 205.