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Comparative Study of Multigate and Multifin Metal–Oxide–Semiconductor Field-Effect Transistor

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In this work, we explore the effects of the number of fins and fin structure on the device DC, dynamic behaviors, and random-dopant-induced characteristic fluctuations of multifin field-effect transistor (FET) circuits. Multifin FETs with different fin aspect ratios [AR ≡ fin height (H_{fin})/fin width (W_{fin})] and a fixed channel volume are simulated in a three-dimensional device simulation and the simulation results are experimentally validated. The multi-fin FinFET (AR = 2) has better channel controllability than the multifin trigate (AR = 1) and multi-fin quasi-planar (AR = 0.5) FETs. A six-transistor (6T) static random access memory (SRAM) using multi-fin FinFETs also provides the largest static noise margin because it supports the highest transconductance in FinFETs. Although FinFETs have a large effective device width and driving current, their large gate capacitance limits gate delay. The transient characteristics of an inverter with multi-fin transistors are further examined, and compared with those of an inverter with single-fin transistors. The multi-fin inverter has a shorter delay because it is dominated by the driving current of the transistor. With respect to random-dopant-induced fluctuations, the multifin FinFET suppresses not only the surface potential but also its variation because it has a more uniform surface potential than the multifin trigate and quasi-planar FET, and so the effects of random dopants on the circuits are attenuated. The results of this study provide insight into the DC, and circuit characteristics of multifin transistors and associated random dopant fluctuations.

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1. Introduction

When the gate length of a bulk metal–oxide–semiconductor field-effect transistor (MOSFET) decreases below 32 nm, the performance of the device is degraded by serious short-channel effects (SCEs). This problem has complicated technological ramifications in the semiconductor industry.[1)] Therefore, diverse approaches to enhancing device performance have been proposed, such as the use of strain silicon,[2)] high-κ/metal gate materials,[3)] and MOSFETs with vertical channels.[4–8)] Among these promising approaches, vertical channels have attracted much attention because of their many interesting characteristics.[9–12)] Various studies of devices with multigate structures have been published.[13)] We presume that multigate devices with multifins will further enhance driving capability. However, no DC characteristic simulation[14)] of multi-gate and multi-fin devices has yet been comprehensively performed; moreover, studies of the behavior and random-dopant-induced fluctuation of their circuits are still lacking.

In this work, a coupled device-circuit simulation[15–18)] is performed to study the device and circuit characteristics of single- and multi-fin devices with fins of different shapes (FinFET, trigate, and quasi-planar MOSFETs). The estimated electrical characteristics include threshold voltage (V_{th}), gate capacitance (C_g), the delay time of the inverter, and the static noise margin (SNM) of a six-transistor (6T) static random access memory (SRAM). Random-dopant-induced fluctuations in the aforementioned characteristics are further discussed with respect to the different ARs. The results of this study indicate that structures with multifins and a large AR may exhibit excellent characteristics and fluctuation suppression. The accuracy of the three-dimensional (3D) quantum drift-diffusion device simulation performed was experimentally verified.[18)]

This article is organized as follows. In §2, we describe the devices and circuits of interest, and the simulation settings. In §3, we present their DC and dynamic characteristics, including their variations. Finally, In §4, we present the conclusions drawn in this study and suggest future works.

2. Multigate and Multifin Devices and Circuits

As shown in Fig. 1(a), 16-nm-gate triple-fin silicon-on-insulator (SOI) FETs are examined. Figure 1(b) shows a cross-sectional view of the devices with different ARs, and Fig. 1(c) shows the tested 6T SRAM and inverter circuit with the adopted triple-fin devices. Table I shows a summary of the specifications of the devices. The physical channel length is assumed to equal the effective channel length, and the thickness of the sidewall spacer thickness is neglected. For fair comparison, the cross-sectional area of the silicon fins in the devices of interest is fixed at 128 nm^2. Additionally, the threshold voltages of the 32-nm-gate devices are initially calibrated to 200 mV for the V_{th} roll-off characteristics. The similarity among cross-sectional areas and V_{th} values ensure that the control volumes of the device channels are the same under the same operating conditions. To study random-dopant-induced fluctuations, dopants are generated randomly with AR = 2, as shown in Fig. 2. A total of 379 dopants are randomly generated in an $80 \times 40 \times 80\,nm^3$ cube, yielding an equivalent doping concentration of $1.48 \times 10^{18}\,cm^{-3}$. The $80 \times 40 \times 80\,nm^3$ cube is then partitioned into 125 subcubes of $16 \times 8 \times 16$ nm^3. The number of dopants in the cubes varies from zero to nine with an average of three. The 125 subcubes are equivalently mapped into the channel region to simulate the sensitivity of the device to the position and number of dopants. Similarly, the 125 subcubes of $11.3 \times 11.3 \times 16$ and $8 \times 16 \times 16\,nm^3$ are mapped into the channel region for the trigate (AR = 1) and the quasi-planar (AR = 0.5) structures.

In estimating circuit characteristics, since no well-established compact model of nanoscale devices is available, a coupled device-circuit simulation is adopted to capture the random-dopant-position-induced fluctuation.[9,15–17)] The nodal equations of the tested SRAM and inverter are formulated (by applying the current and voltage conserva-

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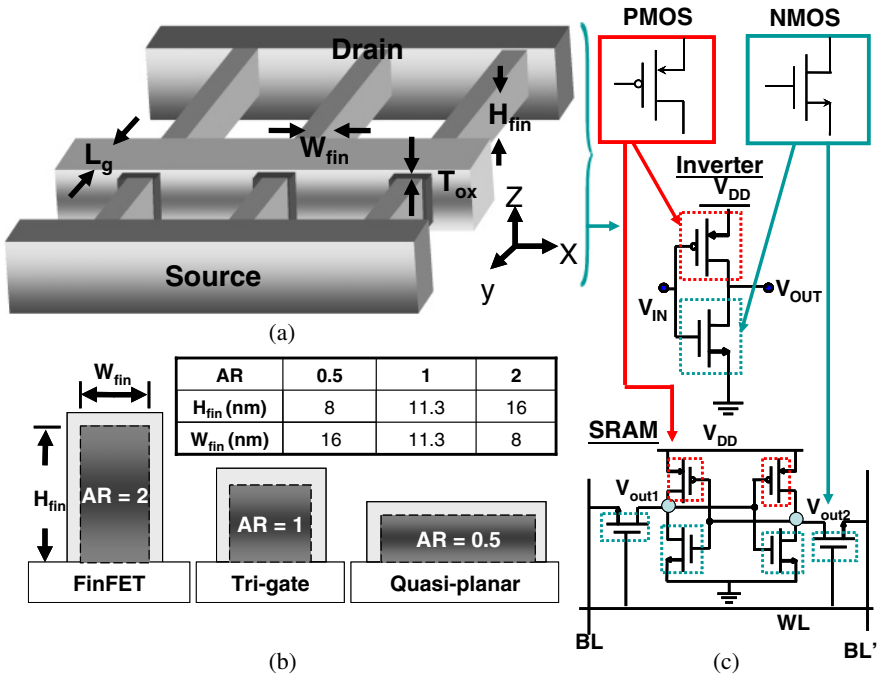


AR	0.5	1	2
H_{fin} (nm)	8	11.3	16
W_{fin} (nm)	16	11.3	8

Fig. 1. (Color online) (a) Schematic plot of the triple-fin MOSFET. (b) The cross-sectional plots of the three studied fin shapes are FinFET (AR = 2), trigate (AR = 1), and quasi-planar (AR = 0.5). The parameter settings for H_{fin} and W_{fin} are listed in the inset table. (c) Inverter and SRAM are tested as the test circuits. BL and BL′ denote bit lines; WL denotes word line.

Table I. Parameters of triple-fin FinFET (AR = 2), trigate (AR = 1), and quasi-planar (AR = 0.5) MOSFETs.

	Quasi-planar	Trigate	FinFET
$V_{th,lin}$ (V)	0.15	0.15	0.15
$V_{th,sat}$ (V)	0.208	0.198	0.193
I_{on} (A)	2.055×10^{-5}	3.126×10^{-5}	4.694×10^{-5}
I_{off} (A)	1.672×10^{-9}	1.213×10^{-9}	1.101×10^{-9}
DIBL	0.058	0.048	0.043
Oxide thickness (nm)	1.2	1.2	1.2
Width (nm)	16	11.3	8
Work function (eV)	4.4	4.4	4.4
Channel doping concentration (cm^{-3})	1.48×10^{18}	1.48×10^{18}	1.48×10^{18}
Body doping concentration (cm^{-3})	1×10^{15}	1×10^{15}	1×10^{15}
Source/drain doping concentration (cm^{-3})	1.7×10^{19}	2.5×10^{20}	3×10^{20}
Effective fin width (nm)	32	33.9	40
V_{DD} (V)	1	1	1

tion laws, Kirchhoff's current law and Kirchhoff's voltage law) and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are solved simultaneously to obtain the circuit characteristics. The device characteristics, such as potential and current density, obtained by the 3D device simulation are utilized in the circuit simulation using circuit nodal equations. The effects of discrete dopants in the transistor on circuit characteristics are thus appropriately estimated. The physical models adopted in the 3D device transport equations were calibrated for the fabricated and measured samples to maximize accuracy.[18)]

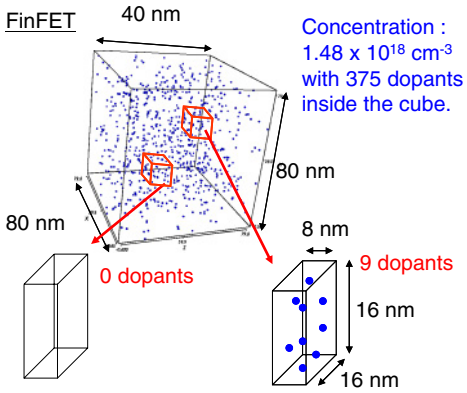


Fig. 2. (Color online) Generated discrete models of FinFET, which follow a Gaussian distribution and range from 0 to 9, with an average of value is 3. Similarly, we also have models of the trigate and quasi-planar FETs.

3. Results and Discussion

Figures 3(a) and 3(b) show plots of the V_{th} roll-off characteristics for single- and triple-fin MOSFETs at different ARs, with the gate length scaled from 32 to 16 nm. The results of this study reveal that the triple-fin FinFET with AR = 2 is less sensitive to the scaling of the gate length because it has a larger effective device width [$W_{eff} = n \times (2 \times H_{fin} + W_{fin})$], where n is the number of fins. Effective device width increases with the number or height of fins. Hence, a moderate V_{th} roll-off of FinFETs exhibits excellent channel controllability and high resistance to intrinsic parameter variations. Figure 4(a) shows plots of the gate capacitances of the 16-nm-gate single- and triple-fin devices. Notably, the threshold voltages of these 16-nm-gate devices (FinFET, trigate FET, and quasi-planar FET) are calibrated to 150 mV to compare their performances. The C_g of the

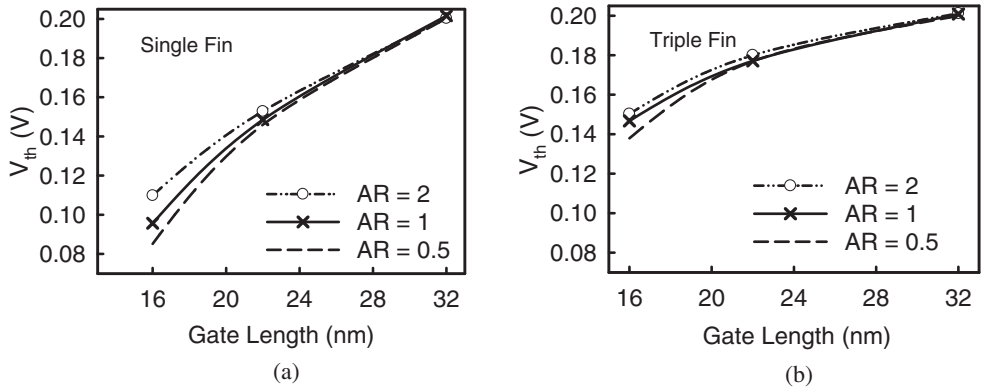


Fig. 3. Plots of $V_{th,sat}$ roll-off characteristics for (a) single-fin and (b) triple-fin MOSFETs for different ARs.

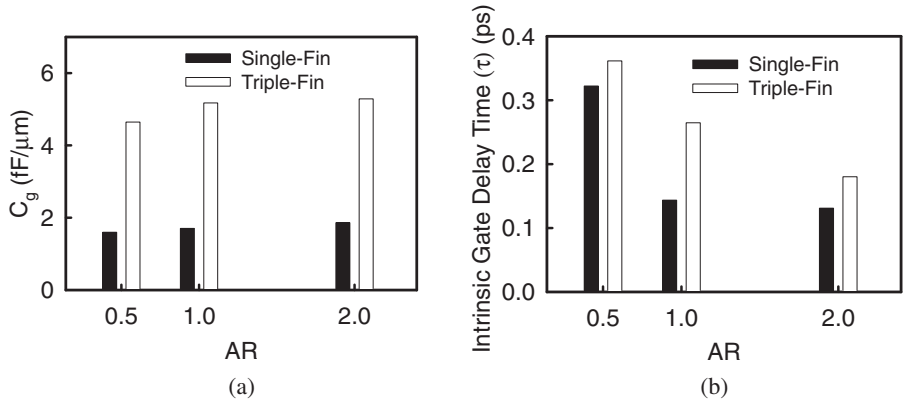


Fig. 4. (a) Device gate capacitances and (b) intrinsic gate delay time for the studied single- and triple-fin transistors with different ARs.

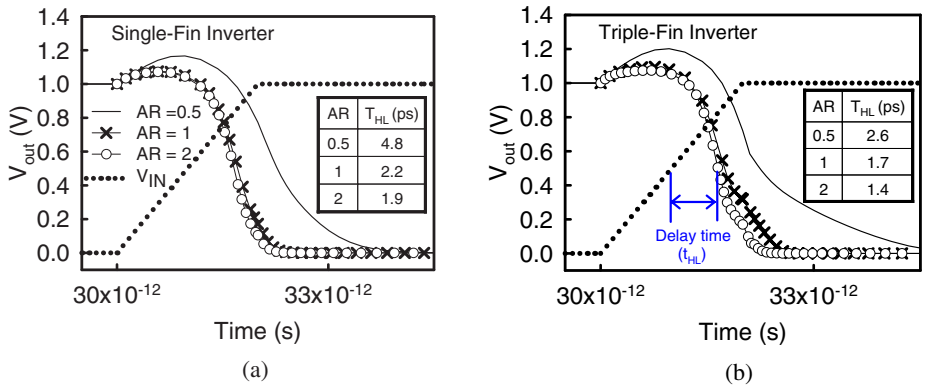


Fig. 5. (Color online) Transient characteristics of (a) single- and (b) triple-fin inverters, where the extracted rise time, fall time, and hold time of the input signal are 2, 2, and 30 ps, respectively.

triple-fin FinFET is 3.7 times that of the triple-fin quasi-planar device. The large C_g of the triple-fin transistor with a high AR enhances charge control; nevertheless, the increased C_g affects the operational speed of the transistors. In the trade-off between I_{on} and C_g, the intrinsic gate delay of the transistor ($\tau = C_g V_{DD}/I_{on}$) is calculated, as shown in Fig. 4(b). The results show that a single-fin FinFET has a τ 1.1 and 2.5 times smaller than those of the trigate FET and quasi-planar FET, respectively, because of its smaller C_g.

Figures 5(a) and 5(b) respectively show plots of the high-to-low transition characteristics of both single- and triple-fin inverters at various ARs, with a power supply voltage of 1 V. The three solid lines represent the output signals of the devices with different fin structures and the dotted line represents the input signal. The high-to-low delay time (t_{HL}) is defined as the time difference between 50% points of the input and output signals during the falling of the output signals. The insets in Figs. 5(a) and 5(b) respectively show plots of the high-to-low delay times (t_{HL}) of the studied single- and triple-fin transistors, which are affected by the shape of the fins. As expected, both single- and triple-fin FinFET inverters have the smallest t_{HL} for various ARs, indicating the advantages afforded by FinFET in terms of both DC and dynamic characteristics. Although the gate

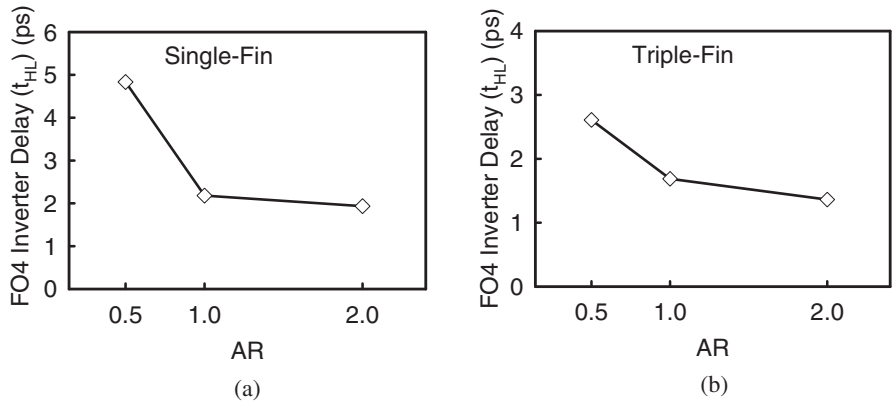


Fig. 6. Gate delay plots of the inverter with fan-out of 4 (FO4) using (a) single- and (b) triple-fin structures.

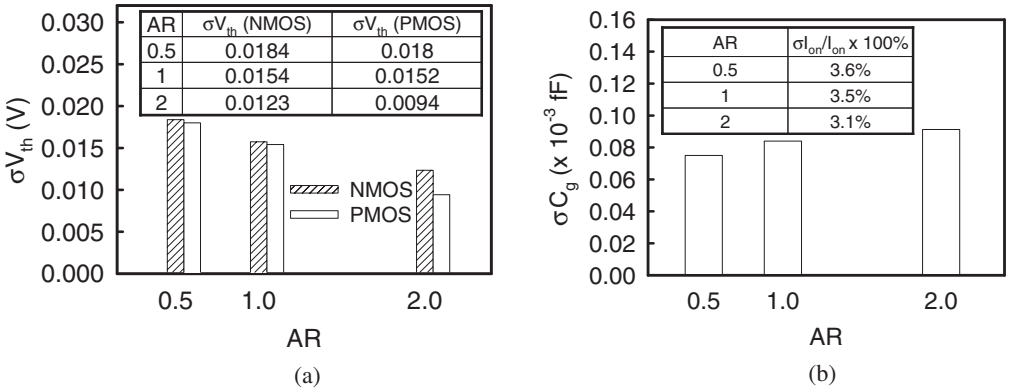


Fig. 7. (a) σV_{th} and (b) σC_g induced by random dopants vs AR for the triple-fin structure. The two insets show the summarized σV_{th} and normalized on-state current fluctuation ($\sigma I_{on}/I_{on}$ × 100%).

capacitance of the triple-fin transistor is larger than that of the single-fin transistor, it provides a smaller transition delay because the increase in drive current is larger. Figure 6 shows a comparison of the single-fin and triple-fin FinFETs for AR = 0.5, 1, and 2 in terms of the fan-out of 4 (FO4) inverter delay. For the single-fin transistor, as shown in Fig. 6(a), delay time decreases substantially as AR is increased. Increasing the number of fins and AR enhances driving ability; allowing delay time to be further reduced, as shown in Fig. 6(b). The delay time of the triple-fin FinFET inverter is about 1.4 times smaller than that of the single-fin FinFET inverter, for example.

Figure 7 shows the random-dopant-induced threshold voltage fluctuation (σV_{th}), and the gate capacitance fluctuation (σC_g) of the studied triple-fin devices. σV_{th} is derived as

$$\sigma V_{th} = \frac{q}{C_{ox}}\sqrt{\frac{N_a W_{dm}}{3LW}}, \quad (1)$$

where W_{dm} denotes the maximum depletion width, N_a denotes the background doping concentration, L and W are the gate length and width, respectively, and C_{ox} is the oxide capacitance.[19] Because σV_{th} is proportional to depletion width, the σV_{th} of p-FET is lower than that of n-FET because the depletion depth is small. The σV_{th} values of n- and p-type FinFETs are 1.5 and 1.9 times, respectively, smaller than that of quasi-planar structures, as shown in Fig. 7(a), suggesting that, for the same channel volume, FinFET has a more uniform surface potential. The σC_g of triple-fin FinFETs is slightly higher than triple-fin trigate and quasi-planar MOSFETs because their gate area is larger, as shown in Fig. 7(b); the inset in Fig. 7(b) shows a plot of the normalized on-state current fluctuation ($\sigma I_{on}/I_{on} \times 100\%$). Although the σC_g of the triple-fin FinFETs is slightly higher than triple-fin trigate and quasi-planar MOSFETs, the large on-state current reduces the $\sigma\tau$ of triple-fin FinFETs, as shown in Fig. 8(a). Figure 8(b) shows the σt_{HL} and σt_{LH} of triple-fin device inverters. σt_{HL} and σt_{LH} are dominated by n-FET and p-FET, respectively. Thus, σt_{HL} exceeds σt_{LH} because n-FETs have a large σV_{th}.

Figure 9(a) shows a plot of the SNM of the triple-fin device SRAM cells, where cell ratio and pull-up ratio are assumed to be unity in this determination. The relation between the device transconductance and SNM of SRAM could be expressed as

$$\mathrm{SNM} \propto \sqrt{1 - \frac{I_{nx}}{g_{m,pmos}}} - \frac{I_{ax}}{g_{m,nmos}}, \quad (2)$$

where I_{nx} is the saturation drain current of the driver transistor of SRAM and I_{ax} is the saturation drain current of the access transistor.[20] The calculated transconductances for AR = 0.5, 1, and 2 are 0.0284, 0.0536, and 0.0752 mA/V, respectively. Consequently, among the explored three structures, FinFET has the largest SNM owing to its having the largest transconductance, as shown in Fig. 9(a).

Figure 9(b) shows the random-dopant-induced SNM fluctuation (σ_{SNM}) of the triple-fin device SRAM cells.

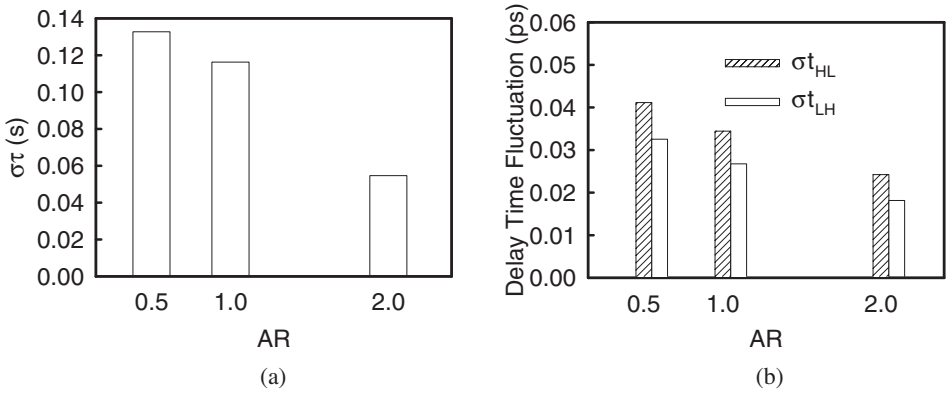
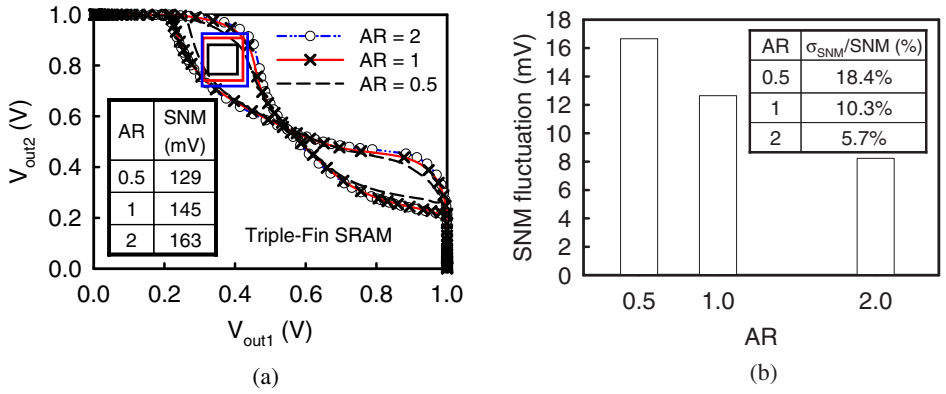


Fig. 8. (a) $\sigma\tau$ of triple-fin transistors. (b) σt_{HL} and σt_{LH} values of the tested inverter with AR = 2, 1, and 0.5.



AR	SNM (mV)
0.5	129
1	145
2	163

AR	σ_{SNM}/SNM (%)
0.5	18.4%
1	10.3%
2	5.7%

Fig. 9. (Color online) (a) Plots of static transfer characteristics for AR = 2, 1, and 0.5; SNM is calculated from the length of the side of a square having the longest diagonal. (b) SNM fluctuations of the examined SRAM with AR = 2, 1, and 0.5. The normalized σ_{SNM} (σ_{SNM}/SNM × 100%) is summarized in the inset of (b).

Triple-fin FinFETs have the smallest σ_{SNM} because they have the smallest σV_{th}. The table inset in Fig. 9(b) shows the normalized σ_{SNM}.

4. Conclusions

The DC characteristics and dynamic behavior of multigate and multifin devices and circuits with different ARs, including random-dopant-induced fluctuations were simulated. Increasing the number of fins and AR improves device performance by suppressing SCE and moderately enhancing the current drive. The multi-fin FinFET has better SCE, driving current, timing characteristic, SNM, and fluctuation resistivity than the trigate FET and quasi-planar FET. We are currently studying the optimal number of channel fins and optimal pinch distance for manufacturing multi-fin FinFETs. The parasitic capacitances of these devices are crucial for advanced multigate and multifin transistor design. We note that devices with intrinsic channels could suppress random-dopant-induced characteristic fluctuation, and that the selection of a metal gate material with an appropriate work function is promising for adjusting threshold voltage. However, completely intrinsic channels may encounter a pronounced short-channel effect, such as punch-through, and additional processes are required to integrate a selected metal gate material. With this consideration, the use of a device with doped channels is still one of the potential solutions to adjusting threshold voltage.[21,22] Thus, the adopted channel doping concentration in this work is empirically assumed to be $1.48 \times 10^{18}\,\mathrm{cm}^{-3}$ to evaluate the effect of random channel doping on the characteristics of the SOI-based FinFET and tri-gate and quasi-planar structures. Nevertheless, we presume that more studies on choosing metal gate materials and optimizing channel doping are necessary for the further scaling of devices.

Acknowledgments

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