Discrete-Dopant-Induced Power-Delay Characteristic Fluctuation in 16 nm Complementary Metal–Oxide–Semiconductor with High Dielectric Constant Material

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Discrete-Dopant-Induced Power-Delay Characteristic Fluctuation in 16 nm Complementary Metal–Oxide–Semiconductor with High Dielectric Constant Material

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In this work, we carry out an experimental validated three-dimensional "atomistic" device-circuit coupled simulation to study the discrete-dopant-induced power and delay fluctuations in 16-nm-gate complementary metal–oxide–semiconductor (CMOS) circuits. The equivalent gate oxide thicknesses (EOTs) of planar CMOS range from 1.2 nm to 0.2 nm. SiO_2 is used at gate oxide thicknesses of 1.2 and 0.8 nm, Al_2O_3 at an EOT of 0.4 nm, and HfO_2 at an EOT of 0.2 nm. Under the same device threshold voltage, as EOT decreases from 1.2 to 0.2 nm, the fluctuations of threshold voltage and gate capacitance for CMOS transistors are reduced by 43 and 55%, respectively. For the state-of-art nanoscale circuits using high-dielectric constant (high-κ) materials, the delay time fluctuation is suppressed significantly from 0.1 to 0.03 ps. For the power characteristics, although the nominal powers of circuits using high-κ dielectrics are increased owing to the increased EOT, the fluctuations of dynamic power, short circuit power, and static power are reduced by 40, 70, and 30%, respectively.

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1. Introduction

Variability in the characteristics of nanoscale complementary metal–oxide–semiconductor (CMOS) field-effect transistor (FET) becomes a major challenge in scaling down and integration. Local device variation and the uncertainty of signal propagation time have become crucial for the variation of system timing and the determination of clock speed.[1–5] Yield analysis and optimization, which take into account manufacturing tolerances, model uncertainties, variations in process parameters, and so forth, are known as indispensable components of circuit design. Diverse approaches have recently been proposed to study fluctuation-related issues in semiconductor devices[6–23] and circuits.[3–5,24–27] To suppress random-dopant-induced fluctuations, various approaches such as those using vertical channel devices,[13,18,19] channel engineering,[9–11,14,21] and high-dielectric constant (high-κ) materials[20,23,28] have been proposed. However, little attention has been focused on the existence of delay and power fluctuations in active devices owing to random dopant placement. Moreover, the effectiveness of using high-κ materials as gate dielectrics against delay and power fluctuations is of great interest and may benefit the nano-device technology.

In this study, we for the first time analyze the random dopant effect on delay and power fluctuations for nanoscale CMOS circuits with high-κ gate materials. Due to the randomness of dopant position in the devices, the fluctuations of device gate capacitance are nonlinear and difficult to model with current well-known compact models.[24,26] Thus, a device-circuit coupled simulation approach[4,5,26,29] is employed. Then, the relationship between equivalent gate oxide thicknesses (EOT) and the fluctuations of device DC and circuit power/delay characteristics are investigated. The accuracy of the developed analyzing technique has been quantitatively verified using the experimentally measured characteristics of 20 nm devices.[20]

The paper is organized as follows. In §2, we describe the analyzing technique for studying the random dopant effect in nanoscale devices and circuits. In §3, we examine the discrete-dopant-induced characteristic fluctuations of the 16-nm-gate device and inverter circuit. Finally, we draw conclusions and suggest future work.

2. Simulation Technique

The nominal channel doping concentration of the devices studied is $1.48 \times 10^{18}\,cm^{-3}$. Outside the channel, the doping concentrations in the source/drain and background are 1.1×10^{20} and $1 \times 10^{15}\,cm^{-3}$, respectively. These devices have a 16 nm gate length, a 16 nm gate width, and a TiN metal electrode with a work function of 4.4 eV. The EOTs of planar n-type MOS (NMOS) FET range from 1.2 to 0.2 nm. SiO_2 is used at gate oxide thicknesses of 1.2 and 0.8 nm, Al_2O_3 at an EOT of 0.4 nm, and HfO_2 at an EOT of 0.2 nm. The generating approach to discrete dopants follows that in our previous work.[17–20] Dopants (758) are first randomly generated in a large cube with a size of $(80\,nm)^3$, in which the equivalent doping concentration is $1.48 \times 10^{18}\,cm^{-3}$, as shown in Fig. 1(a). The large cube is then partitioned into sub-cubes with a size of $(16\,nm)^3$, as illustrated in Figs. 1(b)–1(d), and then equivalently mapped into the channel region of the device channel for the three-dimensional (3D) device simulations with discrete dopants, as shown in Fig. 1(e). On the basis of the statistically generated large-scale doping profiles, we perform device simulation by solving a set of 3D drift-diffusion equations with a density-gradient quantum correction method,[30–32] which is conducted using a parallel computing system.[33,34] Notably, in "atomistic" device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in Coulomb potential.[16] The potential becomes too steep when using a fine mesh; therefore, majority carriers are nonphysically trapped by ionized impurities, and mobile carrier density is reduced.[16] Thus, density-gradient approximation is used to handle discrete charges by properly introducing related quantum-mechanical effects, and cou-

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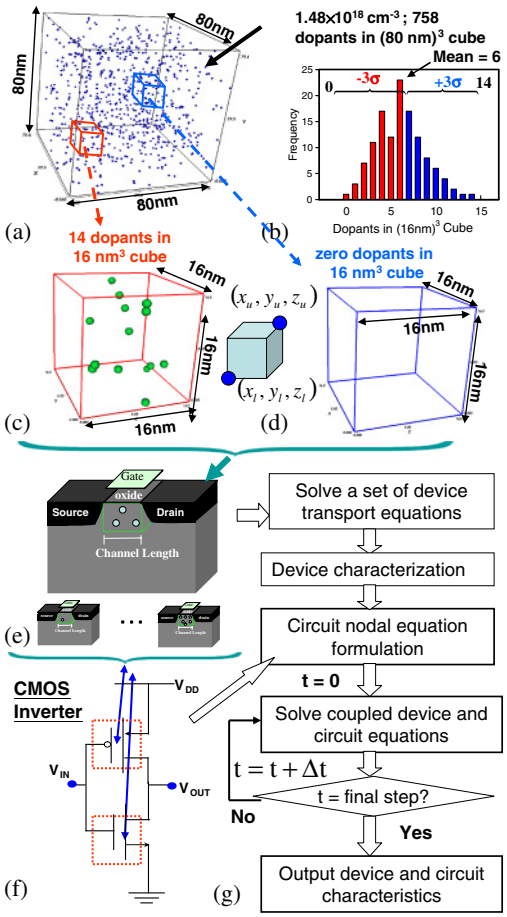

Fig. 1. (Color online) (a) Discrete dopants randomly distributed in the large cube with a size of $(80\,\text{nm})^3$ at an average concentration of $1.48 \times 10^{18}\,\text{cm}^{-3}$. There are 758 dopants within the large cube, but the number of dopants in sub-cubes with a size of $(16\,\text{nm})^3$ varies from zero to 14 (with an average of 6) [(b)–(d)]. The sub-cubes are equivalently mapped into the channel region for dopant-position/number-sensitive device simulation and device-circuit coupled simulation [(e)–(g)], where the inverter is used as a test circuit for timing and power variation estimation.

pled with device transport equations. The accuracy of the simulation technique was confirmed by comparing simulated fluctuation results with measurements of experimentally fabricated 20 nm devices.[20] Figure 1(f) shows the CMOS inverter circuit used as the test circuit for exploring the power/delay characteristic fluctuations in nanoscale CMOS circuits. Similarly, we can generate discrete-dopant-fluctuated devices for p-type MOS (PMOS) FET following the flow illustrated in Figs. 1(a)–1(d). Then, pairs of discrete-dopant-fluctuated NMOS and PMOS devices are randomly selected and are used for the examination of circuit characteristics fluctuations. To fairly compare the NMOS-/PMOS-induced characteristic fluctuations and eliminate the effect of transistor size on the fluctuations, the dimensions, channel doping concentration, and threshold voltage (V_{th}) of the NMOS and PMOS devices are the same. Similarly, to compare the devices of different EOTs on the same basis, the V_{th} of the explored devices are adjusted to 140 mV by changing the source and drain doping concentration. Since there is no well-established compact model for such ultra-small nanoscale devices, and for capturing the discrete-dopant-position-induced fluctuations, a device-circuit-coupled simulation approach[4,5,26,29] is used, as shown in

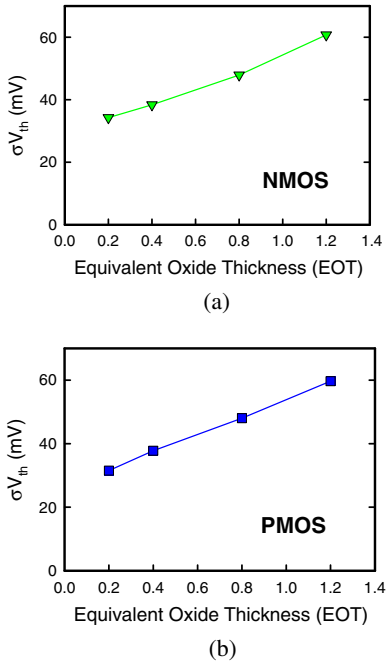

Fig. 2. (Color online) Threshold voltage fluctuations with different high-κ materials for (a) NMOS and (b) PMOS.

Fig. 1(g). The circuit nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations) solved simultaneously to obtain the circuit characteristics.

3. Results and Discussion

In this section, the device and circuit characteristic fluctuations are investigated in terms of V_{th}, and gate capacitance (C_{g}), delay, and power. We then compare the dependence of characteristic fluctuations on equivalent oxide thickness. Figures 2(a) and 2(b) show the threshold voltage fluctuation (σV_{th}) as a function of EOT for 16-nm-gate NMOS and PMOS transistors, respectively. The results show that the random-dopant-induced fluctuations can be suppressed by decreasing equivalent oxide thickness. Our result does not follow the analytic formula:[12]

$$\sigma V_{\text{th,RDF}} = 3.19 \times 10^{-8} \frac{t_{\text{ox}} N_{\text{A}}^{0.401}}{\sqrt{WL}},$$

because the V_{th} of the explored transistors are calibrated to 140 mV. The tendency is still the same with a different slope. Since the channel doping concentrations of the studied devices are the same, the drain-induced barrier lowering (DIBL) is suppressed using high-κ dielectrics, as shown in Fig. 3. The RDF-fluctuated gate capacitance fluctuation (σC_{g}) with different EOTs are presented in Figs. 4(a)–4(d), where the solid line is the nominal device characteristics with 16-nm-gate length and width, $1.48 \times 10^{18}\,\text{cm}^{-3}$ channel doping, 4.4 eV workfunction, and the dashed lines are devices characteristics with fluctuations. As EOT decreases, the diversity of C–V curves is reduced. Figures 5(a)–5(b), 5(c)–5(d), and 5(e)–5(f) show the summaries of nominal C_{g}, σC_{g}, and normalized σC_{g}, respectively. The drain and gate biases are 0.5 and 1 V. The nominal C_{g} of different high-κ materials increases as the equivalent oxide thickness

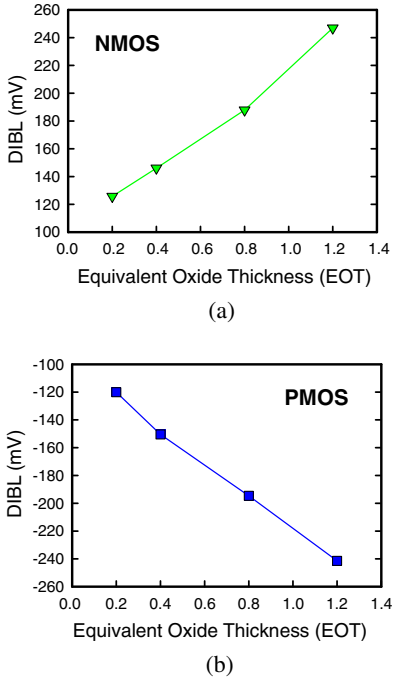

Fig. 3. (Color online) Drain-induced barrier lowering (DIBL) with different high-κ materials for (a) NMOS and (b) PMOS.

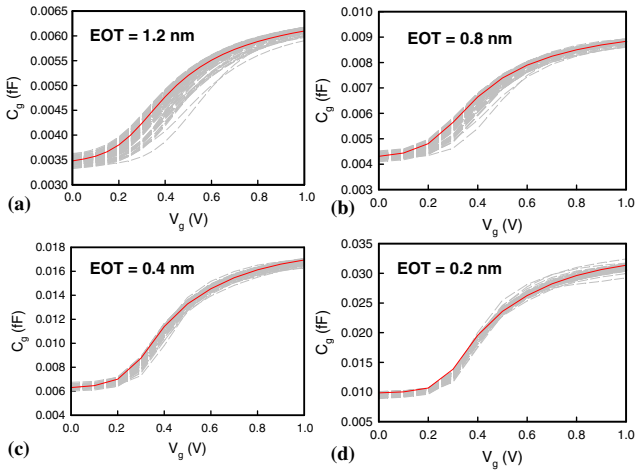

Fig. 4. (Color online) *C*–*V* characteristics for transistors of (a) 1.2, (b) 0.8, (c) 0.4, and (d) 0.2 nm EOTs.

decreases. Although the magnitude of σC_g increases with increasing C_g, normalized σC_g is reduced due to the enhanced channel controllability by the decreased EOT. The use of high-κ dielectrics is effective to suppress both device DC and AC characteristic fluctuations.

Figures 6(a) and 6(b) present the nominal high-to-low delay time (t_{HL}), low-to-high delay time (t_{LH}) of inverters with different EOTs. Both the delay times are reduced due to the larger driving current induced by smaller equivalent gate oxide thickness. Notably, we herein use the gate capacitance of transistor as the load capacitance (C_{load}) and focused on the device intrinsic parameter fluctuations induced circuit variability. The result of the nominal propagation delay may be changed as we take an additional load capacitance into consideration. High-to-low delay time, low-to-high delay time fluctuations ($\sigma t_{HL}/\sigma t_{LH}$) and normalized $\sigma t_{HL}/\sigma t_{LH}$ with respect to different EOTs are shown in Figs. 6(c)–6(f). Since the t_{HL} and t_{LH} are dependent on V_{th} for NMOS and PMOS transistors, the trend of $\sigma t_{HL}/\sigma t_{LH}$ follows the $\sigma V_{th,NMOS}$ and $\sigma V_{th,PMOS}$, respectively. Therefore, as shown in Fig. 6, the delay time fluctuation is

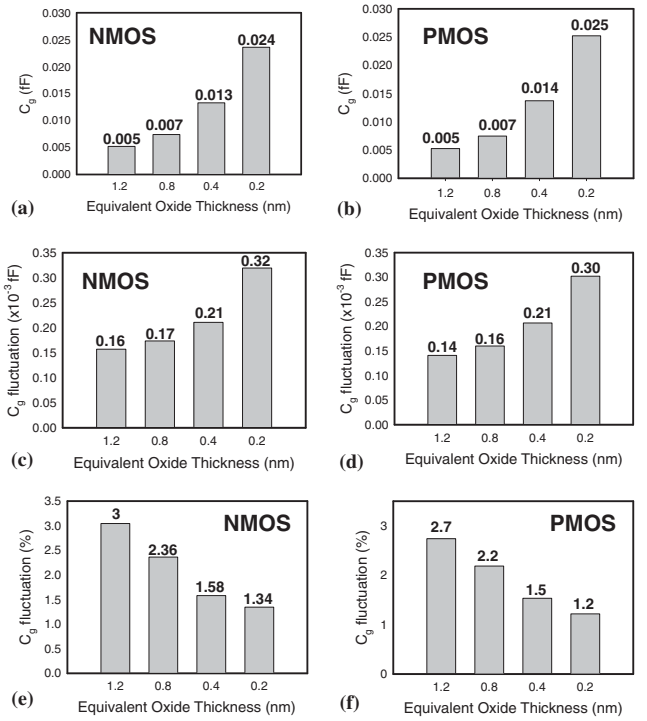

Fig. 5. [(a) and (b)] nominal gate capacitance, [(c) and (d)] gate capacitance fluctuation, and [(e) and (f)] normalized gate capacitance fluctuation for NMOS and PMOS with different high-κ materials.

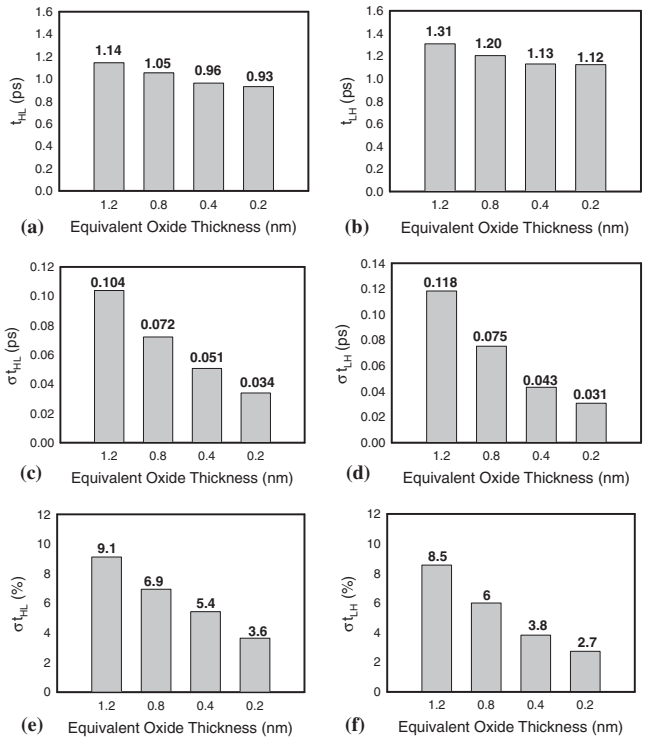

Fig. 6. t_{HL}/t_{LH} [(a) and (b)], $\sigma t_{HL}/\sigma t_{LH}$ [(c) and (d)], and normalized $\sigma t_{HL}/\sigma t_{LH}$ [(e) and (f)] of inverters with different high-κ materials.

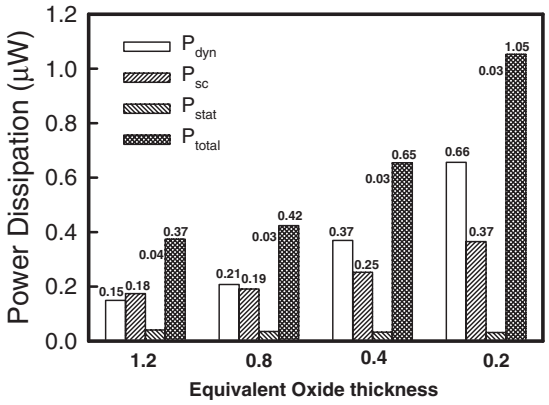

Fig. 7. Summarized power dissipations for the explored 16-nm-gate CMOS inverter.

suppressed as EOT decreased. As EOT decreases from 1.2 to 0.2 nm, the normalized σt_{HL} and σt_{LH} are suppressed by factors of 2.5 and 3.1, respectively. Figure 7 exhibits the nominal power dissipation for the studied inverters. Total power (P_{total}) consists of dynamic power (P_{dyn}), short circuit power (P_{sc}), and static power (P_{stat}). Their definitions are given by

$$P_{dyn} = C_{load} V_{dd}^2 f_{0\to1}, \tag{1}$$

$$P_{sc} = f_{0\to1} V_{DD} \int_T I_{sc}(\tau)\, d\tau, \tag{2}$$

$$P_{stat} = V_{DD} I_{leakage}, \tag{3}$$

where $f_{0\to1}$ is the clock rate. I_{sc} is the short circuit current, which is observed as both NMOSFET and PMOSFET are turned on resulting in a DC path between the power rails. T is the switching period. $I_{leakage}$ is the leakage current that flows between the power rails in the absence of switching activity. Short circuit power is determined by the time of existence of the DC path between the power rails and short circuit current. Since V_{th} for the explored devices are calibrated, P_{sc} is then determined by I_{sc}, and I_{sc} is dependent on the saturation current of the devices. P_{dyn} and P_{sc} are the two significant factors in total power consumption, and they increases as EOT decreases owing to the increased device gate capacitance. The corresponding power fluctuations are further explored in Fig. 8. Figures 8(a) and 8(b) show the dynamic power fluctuations (σP_{dyn}) and normalized σP_{dyn} of the bulk planar MOSFET inverter circuits. Similar to the trend of gate capacitance fluctuation, σP_{dyn} increases and normalized σP_{dyn} decreases as the EOT decreases. Figures 8(c) and 8(d) display the short circuit power fluctuation (σP_{sc}) and normalized σP_{sc}. Short circuit power is defined by the time of existence of the DC path between the power rails and short circuit current, and depends on the threshold voltage of NMOS and PMOS. The trend of short circuit power fluctuations is therefore similar to that of σV_{th}. Figures 8(e) and 8(f) show the static power fluctuation (σP_{stat}) and the normalized σP_{stat}. Since leakage current is an exponential function of V_{th} ($I_{leakage} \propto \exp(-qV_{th}/nkT)$), static power fluctuation becomes significant even though static power is not an important part in total power dissipation.[35] Our result shows that the use of a high-κ material can not significantly reduce delay time and power fluctuations at the same time.

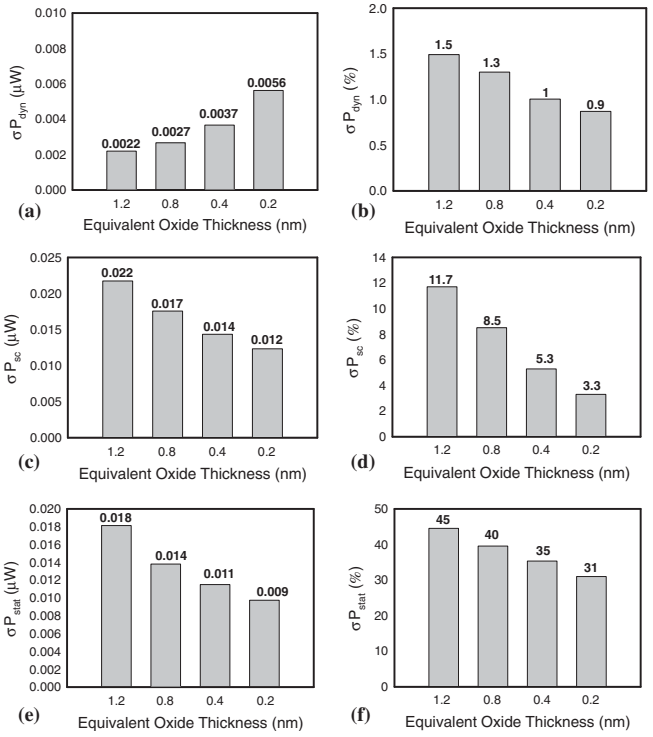

Fig. 8. Fluctuations of (a) dynamic power, (b) short circuit power, (c) static power, and their normalized values [(d)–(f)] for CMOS inverter of different ETOs.

4. Conclusions

In this study, we have investigated the random-dopant-induced delay and power characteristic fluctuations in nanoscale CMOS circuits of different EOTs. Under the same device threshold voltage, as EOT decreases from 1.2 to 0.2 nm, the fluctuations of threshold voltage and gate capacitance for CMOS transistors are reduced by 43% and 55%, respectively. Although the nominal value of gate capacitance increases with increasing dielectric constant, their normalized fluctuations induced by discrete dopants are decreased due to the enhanced channel controllability. For the delay time and power fluctuations, as EOT decreases from 1.2 to 0.2 nm, the normalized σt_{HL} and σt_{LH} are suppressed by factors of 2.5 and 3.1, respectively. The trend of $\sigma t_{HL}/\sigma t_{LH}$ follows those of $\sigma V_{th,NMOS}$ and $\sigma V_{th,PMOS}$. For the power characteristics, although the nominal powers of circuits fabricated using high-κ dielectrics are increased due to the increased EOT, the fluctuations of dynamic power, short circuit power, and static power are reduced by 40, 70, and 30%, respectively.

Acknowledgments

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