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Tungsten Oxide Resistive Memory Using Rapid Thermal Oxidation of Tungsten Plugs

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A complementary metal oxide semiconductor (CMOS)-compatible WO_x based resistive memory has been developed. The WO_x memory layer is made from rapid thermal oxidation of W plugs. The device performs excellent electrical properties. The switching speed is extremely fast (~2 ns) and the programming voltage (<1.4 V) is low. For single-level cell (SLC) operation, the device shows a large resistance window, and 10^8-cycle endurance. For multi-level cell (MLC) operation, it demonstrates 2-bit/cell storage with the endurance up to 10000 times. The rapid thermal oxidation (RTO) WO_x resistance random access memory (RRAM) is very promising for both high-density and embedded memory applications.
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1. Introduction

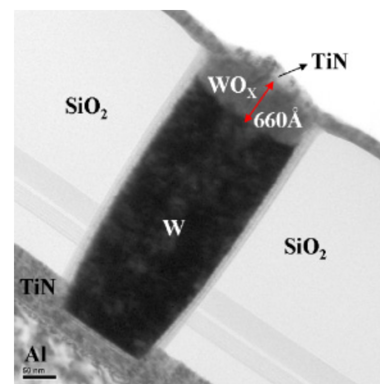
Recently, resistance-based memories have attracted much attention for high-density memory applications because of its simple structure, small cell size, high speed operation, low power consumption, and potential for three dimension (3D) stacking.[1)] Many transition metal oxides, such as TiO_x,[2,3)] MoO_x,[4)] NiO_x,[1,5)] CuO_x, TaO_x, and CoO_x,[6)] have been investigated. WO_x is attractive because it requires only one extra mask with no new equipment or new material needed.[7)] Besides, WO_x resistance random access memory (RRAM) element is easily fabricated in a self-aligned process by converting a portion of the W plug into WO_x. Moreover, the process is compatible to both aluminum and copper back-end-of-line (BEOL) processes. These make the WO_x RRAM suitable for both stand-alone memory and embedded applications. In this work,[8)] we report a new WO_x RRAM formed by rapid thermal oxidation (RTO) of the W plugs. The new device preserves the low voltage and high speed operation of plasma oxidized WO_x, but in addition provides tighter resistance distribution and larger resistance window.

2. Experimental Methods

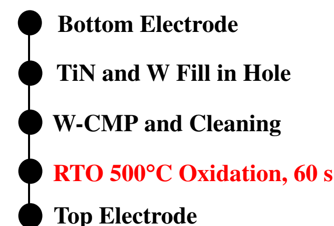
Figure 1(a) shows the cross sectional transmission electron microscope (TEM) image of a RTO WO_x resistive memory cell. The WO_x fabrication process, as shown in Fig. 1(b), follows the conventional back-end-of-line (BEOL) W-plug process. The RTO process converts the top portion of the W plugs into the WO_x memory layer. The oxidation step is 60 s in oxygen ambient at 500 °C. The temperature ramping rate is 10 °C/s, and the cooling rate is 15 °C/s. The thickness of WO_x under the above RTO condition is about 660 Å. We noticed that the top portion of the adhesion TiN layer is also converted into high resistive $TiNO_x$. Since the initial resistance of the WO_x RRAM is around 500 Ω, the much higher parallel resistance of $TiNO_x$ has no effect on the WO_x switching behaviors.

3. Results and Discussion

It was reported that the WO_x RRAM devices using plasma oxidation WO_x require a forming process to reduce the operation voltages.[7)] Similarly, the new memory device using RTO WO_x also requires a forming process before it exhibits RRAM switching behavior. After applying a forming pulse (3.5 V/50 ns) to the cells, the resistance increases from the initial 500 Ω to several tens of kΩ. The programming voltage then decreases to 1 V, where the device resistance starts to increase from the low resistance state (LRS) to the high resistance state (HRS), as shown in Fig. 2. The resistance saturates at ~60 kΩ when the programming voltage exceeds 1.8 V. The resistance window of the new RTO WO_x device is 10× of the plasma oxidation WO_x device,[9)] a clear indication of strong dependence of the oxidation process.



(a)



(b)

Fig. 1. (Color online) (a) The cross sectional TEM image of a 500 °C RTO WO_x device. (b) The process flow for the self-aligned RTO WO_x RRAM.

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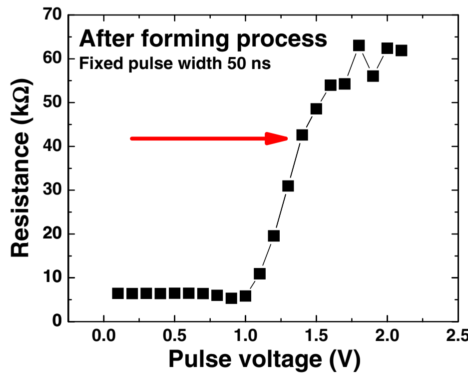

Fig. 2. (Color online) *R*–*V* characteristics of a RTO WO_x RRAM device after the forming process. The forming process can reduce the operation voltages to as low as 1 V. The device cell size is 0.16 μm diameter, the cell area is 0.020 μm^2.

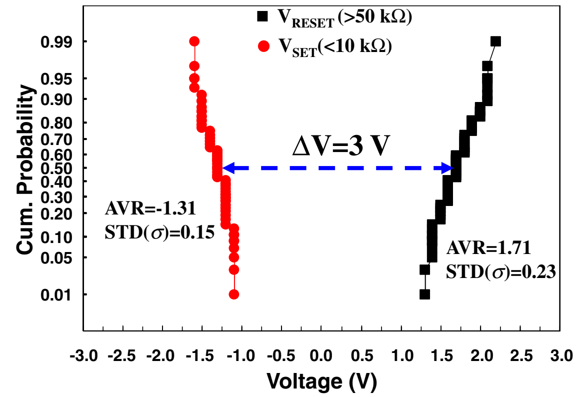

Fig. 4. (Color online) Voltage distributions from 50 memory cells for successful RESET and successful SET operations. The memory cells are at different locations on the same wafer. The RESET and SET pulses are 50 ns. The device cell size is 0.16 μm diameter, the cell area is 0.020 μm^2.

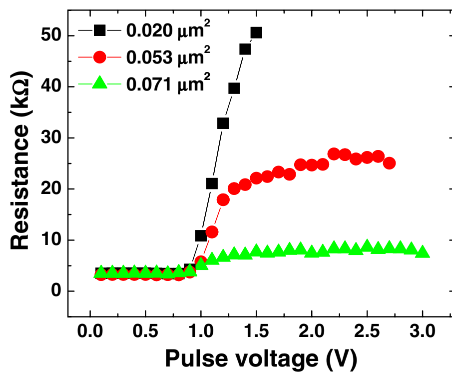

Fig. 3. (Color online) The resistance window increases as the contact size shrinks. All the devices are treated with the forming process (3.5 V/ 50 ns) before the test.

Figure 3 shows the resistance vs voltage (*R*–*V*) curves from the cells with different contact sizes. The contact sizes were measured after contact etching. All the cells received the same forming process before their *R*–*V* curves were collected. The cell with a smaller contact shows a lager resistance window while the cell with a larger contact size shows very little resistance change after the programming pulses. From our previous work[7] by plasma oxidation method, there are WO_2, W_2O_5, and WO_3 coexisted. Although the devices in this work are fabricated by RTP method, the film structure might be similar. The resistivity of WO_3 is significant higher than those of WO_2, and W_2O_5. After forming, we believe that a shallow WO_3 rich high resistance layer is formed at the interface of the WO_x and the top electrode. The resistance can be given by the equation, $R = \rho L/A$, where ρ is the resistivity, L is the length, and A is cross-sectional area. Assuming the resistivity and the layer keeps the same; theoretically the resistance is reverse proportional to the cross-sectional area is higher. In Fig. 3, a resistance after forming is lower when the cross-sectional area is larger. Anyway, some offset is also observed. The micro-structural fluctuation in film thickness and composition may be the reason the offset.

To further test the cell distribution across a wafer, we measured 50 RTO WO_x cells at different locations. Figure 4 shows programming voltages required for successful SET and successful RESET operations to the 50 cells. A successful SET operation reduces the cell resistance to below 10 kΩ; a successful RESET raises the resistance to higher than 50 kΩ. The SET operation, which changes the cell from HRS to LRS, uses a pulse of the opposite polarity as the RESET operation. The pulse amplitude must be high enough to bring the device resistance to below 10 kΩ. In Fig. 4, the tight distributions for both the RESET voltage and the SET voltage imply that the RTO process is quite uniform. Since W Plug and RTO processes are quite mature in CMOS technology, the process control of the new RTO WO_x RRAM is much easier than that of the previous WO_x devices using plasma oxidation. The voltages for the forming process ($\leq$3.5 V), the RESET operation and SET operation are low (<2 V), the high voltage circuits and the corresponding charge pumping circuits in the conventional Flash memories are not needed. This greatly reduces the process complexity as well as the chip size. The good process control makes the WO_x RTO RRAM very interesting for embedded applications as well.

The new RTO WO_x devices show excellent cycling endurance when a program verify operation is introduced. The program verify operation gives extra programming pulses when a cell does not pass the verification. This ensures that the cycled devices have consistent resistance window over time. A fixed resistance window (from 10 to 50 kΩ) can be maintained very well even after 10^8 cycles (1.4 V, 50 ns for RESET and −1 V, 50 ns for SET), as shown in Fig. 5(a). Reducing the RESET pulse amplitude (from 1.4 to 1 V) can improve the endurance by one order of magnitude to 10^9 cycles at the cost of smaller resistance window (from 50 to 20 kΩ) (1 V, 50 ns for RESET and −1 V, 50 ns for SET), as shown in Fig. 5(b).

In order to examine the high frequency responses of the RTO WO_x RRAM devices, a customized high-speed tester[10] is used. The tester is capable of outputting any pulse width and height with the shortest pulse width down to 2 ns. The impedance is carefully matched in order to minimize the reflecting pulses. Figure 6 shows the transient current vs voltage (*I*–*V*) characteristics for the RESET operation, and Fig. 7 shows the transient characteristics for the SET operation. The RESET pulse width is only 2 ns and the equivalent current density is about 3.4×10^6 A/cm^2. After

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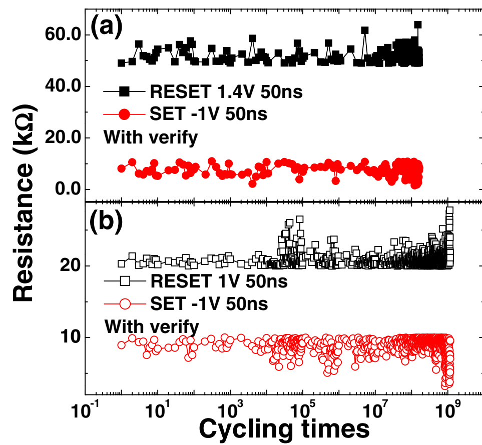

Fig. 5. (Color online) (a) Cycling endurance of a WO_x memory cell. With the program verify, the resistance window between HRS and LRS is well separated even after 10^8 cycles. (b) If the RESET pulse amplitude is reduced, the endurance can be further improved to $>10^9$ cycles while the resistance window is smaller.

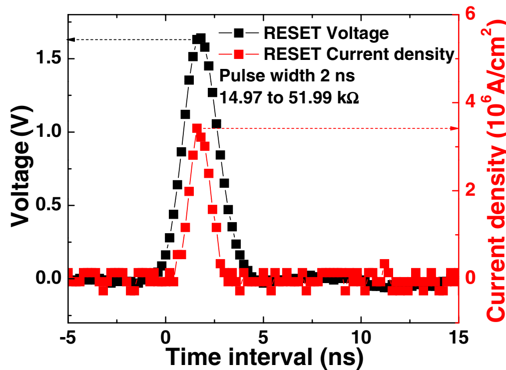

Fig. 6. (Color online) Time resolved voltage and current traces of a typical RESET operation. The RESET pulse width is 2 ns, and the current density is about 3.4 x 10^6 A/cm^2.

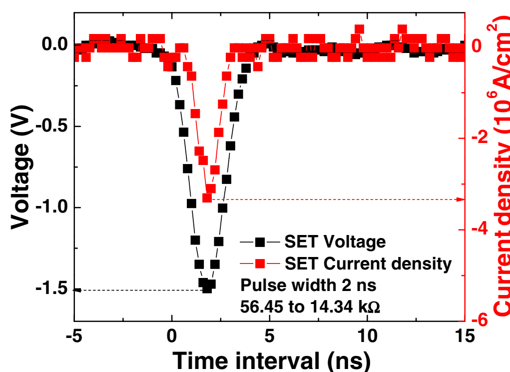

Fig. 7. (Color online) Time resolved voltage and current traces of a typical SET operation. The SET current density is about 3.3 x 10^6 A/cm^2.

the RESET pulse, the device resistance was raised from 14.97 to 51.99 kΩ, which indicates that the pulse is sufficient for a successful RESET operation. The SET operation is completed by another 2 ns pulse with the opposite polarity. The estimated current density is 3.3 × 10^6 A/cm^2. After the SET pulse, the cell resistance decreases from 56.45 to

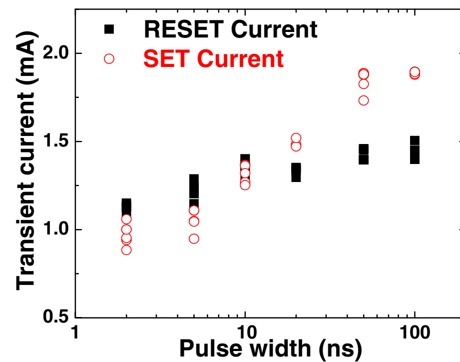

Fig. 8. (Color online) Transient RESET/SET currents with respect to different pulse widths. The test conditions are RESET pulse height is 1.5 V, SET pulse height is −1.2 V. The device cell size is 0.16 µm diameter, the cell area is 0.020 µm^2.

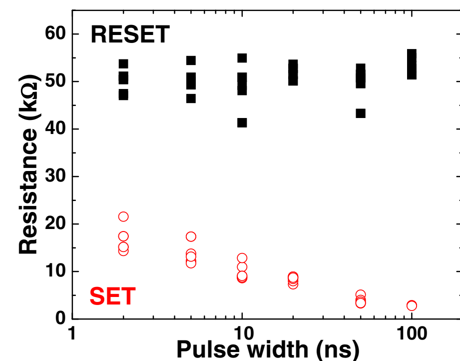

Fig. 9. (Color online) The corresponding resistance readout after RESET/SET operations with various pulse widths. The test conditions are RESET pulse height is 1.5 V, SET pulse height is −1.2 V. The device cell size is 0.16 µm diameter, the cell area is 0.020 µm^2.

14.34 kΩ. The very fast operations suggest that the new RTO WO_x RRAM has the potential for dynamic random access memory (DRAM)-like applications.

The transient currents for the RESET and the SET operations with respect to different pulse widths (ranging from 2 to 100 ns) are shown in Fig. 8. The corresponding resistances after the RESET or the SET operation are shown in Fig. 9. We found that the RESET currents increase slightly as the pulse width increases while the final resistances stay unchanged. On the other hand, the SET current increased by 2× as the SET pulse width increased from 2 to 100 ns. A longer SET pulse gives a lower SET resistance due to more set power through a cell. Comparing the information included in Figs. 3, 8, and 9, we can observe that the pulse voltage is a sufficient parameter to control the RESET resistance (Fig. 3), while the RESET resistance keeps almost the same when the pulse width varies from 2 to 100 ns (Fig. 9). Increasing the SET pulse width can decrease the SET resistance to about 50% and increase the resistance window. Anyway, the current needed is also almost doubled (Fig. 8). From Fig. 3, it is also observed that when the device diameter is scaled down, the resistance window is enhanced, which is beneficial for further scaling.

We have further examined the feasibility of multi-level cell (MLC) operation for the new RTO WO_x RRAM since it shows a larger resistance window than its predecessor,

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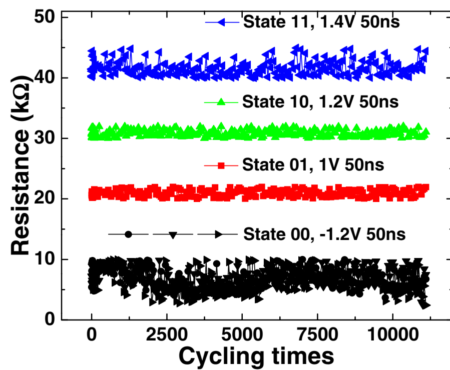

Fig. 10. (Color online) Resistance readout for four different levels in a cycling test. With sophisticated verify mechanism, 10^4 cycles are achievable. The three RESET states (01,10,11) are programmed by positive pulses with different amplitudes, and the SET level (00) is programmed by a negative pulse.

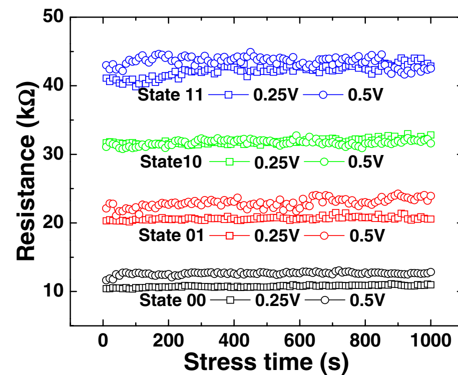

Fig. 11. (Color online) Read disturb test for the four levels. All the states are immune to any resistance drift as long as the read voltage is kept below 0.5 V. The typical read voltage is 0.25 V.

the plasma oxidation WO_x. Two intermediate states (states 10 and 01) are placed between the LRS (10 kΩ) and the HRS (40 kΩ) for 2-bit/cell operation. A more than 7 kΩ resistance window is maintained for any two adjacent states. The LRS is achieved by a −1.2 V, 50 ns SET pulse. The HRS 01, 10, and 11 are obtained by applying 50 ns of 1, 1.2, and 1.4 V pulses, respectively. Sophisticated verify mechanisms are also developed in order to keep the device resistance staying in the pre-defined ranges. With this MLC program verify, more than 10^4 cycles is demonstrated, as shown in Fig. 10.

Finally, we check the resistance stability against continuous read operations. Figure 11 shows that the cell has good immunity to read disturb for all the four states for 1,000 s if the read voltage is kept $\leq$0.5 V. Note that the typical read voltage is only 0.25 V.

4. Conclusions

Tungsten plugs and RTO are mature IC processes. They enable a new and CMOS-compatible WO_x-based RRAM. For single-level cell (SLC) operation, excellent cycling endurance (up to 10^8 times), fast switching speed ($\sim$2 ns), and low voltage (1.4 V) programming are demonstrated. For MLC operation, 2-bit/cell storage with more than 10000 cycling endurance and stable resistance readout over time are demonstrated. This new RTO WO_x RRAM is promising for both high density storage and embedded memory applications.

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