IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

Low-Temperature Polycrystalline Silicon Thin Film Transistor Nonvolatile Memory Using Ni Nanocrystals as Charge-Trapping Centers Fabricated by Hydrogen Plasma Process

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2010 Jpn. J. Appl. Phys. 49 06GG15

(http://iopscience.iop.org/1347-4065/49/6S/06GG15)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 25/04/2014 at 06:20

Please note that terms and conditions apply.

Low-Temperature Polycrystalline Silicon Thin Film Transistor Nonvolatile Memory Using Ni Nanocrystals as Charge-Trapping Centers Fabricated by Hydrogen Plasma Process

Terry Tai-Jui Wang, Pei-Ling Gao, William Cheng-Yu Ma[1], and Cheng-Tzu Kuo[2]*

Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan
[1]*Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan*
[2]*Department of Materials Science and Engineering, MingDao University, Changhua 52345, Taiwan*

Received November 30, 2009; accepted January 18, 2010; published online June 21, 2010

Processes for fabricating a Ni nanocrystal (NC)-assisted low-temperature polycrystalline silicon thin film transistor (LTPS-TFT) nonvolatile memory device of noble stack below 600 °C were successfully developed. The NCs were fabricated in H-plasma atmosphere by heating a nanosized Ni film to realize an appropriate nanoparticle distribution. Results show that NCs with a number density of $\sim 5 \times 10^{11}$ cm^{-2} and a particle diameter of 4 to 12 nm can successfully be fabricated as charge-trapping centers for enhancing the device performance. The results also indicate that the data retentions at the initial time and after 10^4 s for a SiO_2/Ni-NCs/Si_3N_4/SiO_2 gate under the present stack of devices are about 2.2 and ~1.1 V, respectively. © 2010 The Japan Society of Applied Physics

DOI: 10.1143/JJAP.49.06GG15

1. Introduction

Recently, the NAND flash has become more popular for mobile electronic products, and the demand for memory density is multiplied every year. Although the NAND flash is aggressively scaled down, it becomes continuously difficult to follow Moore's law owing to physics limitations. A three-dimensional (3D) multilayer-stack memory was proposed as one of the methods for realizing an ultrahigh-density memory.[1–4] Furthermore, a nonvolatile memory assisted by semiconductor nanocrystals (NCs), such as Si or Ge NCs, has widely been studied to examine the charge trapping ability of NCs.[5–10] One greatest advantage of using NCs is that charges are distributed in more trapping centers, which minimizes charge loss. It results in a thinner tunnel oxide, a lower working voltage, and a higher program/erase (P/E) speed. The use of metallic NCs was also proposed; the metallic NCs were observed to exhibit higher performance characteristics than semiconductor NCs owing to a stronger coupling with the conduction channel, a wider range of available work functions, a higher density of states around the Fermi level for storing more charges, and a smaller energy perturbation due to carrier confinement.[11–17] However, most of those studies were conducted to examine effects of NCs embedded in Si-wafer-based devices on memory performance. To extend the potential applications of NCs in 3D memory structures, one of the important issues is the fabrication of the memory device on a SiO_2 isolation layer instead of a Si wafer, for which a low-temperature process (below 600 °C) is required. In this study, low-temperature processes were developed to fabricate Ni-NCs to be embedded in thin film transistor-nonvolatile memory (TFT-NVM) devices on SiO_2 substrates. Furthermore, nickel was selected as a NC material, considering its high work function (5.15 eV),[18] which yielded a deep energy well, a thin tunnel layer, and a low device operating voltage. Effects of H-plasma treatment on the size and distribution of Ni nanoparticles were reported for catalyst application to synthesize carbon nanotubes.[19] In addition, the H-plasma treatment for fabricating Ni-NCs using a chemical vapor deposition (CVD) system is a popular and favorable process for integration with the formation of low-temperature polycrystalline silicon (poly-Si) TFT devices.

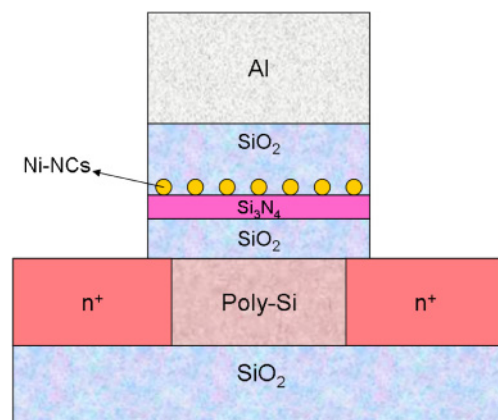

Fig. 1. (Color online) Structure of TFT-flash memory with Ni-NCs. The SiO_2/Si_3N_4/Ni-NCs/SiO_2 gate stack is shown.

2. Experimental Methods

Figure 1 shows the TFT-NVM device structure with the embedded Ni-NCs. The fabrication of the TFT-NVM was started by oxidizing the Si substrate in water vapor at 1000 °C to form 500-nm-thick SiO_2 for simulating the isolation layer of 3D NVM devices. The SiO_2-coated wafer was then deposited at 550 °C using a 100-nm-thick amorphous Si layer by low-pressure chemical vapor deposition (LP-CVD). The process was followed by annealing at 600 °C for 24 h in N_2 atmosphere to crystallize the amorphous Si to form a poly-Si/SiO_2/Si structure stack. The 500-nm-thick field isolation oxide layer was then deposited on the stack by plasma-enhanced CVD (PECVD), and the active source and drain regions were then formed by patterning and etching the field isolation oxide layer. These active regions were implanted with phosphorus (35 keV, 5×10^{15} cm^{-2}) and then activated at 600 °C for 24 h in N_2 atmosphere. The patterning and activation of the stack were followed by SiO_2/Si_3N_4 (7 nm/3 nm) gate stack deposition

*E-mail address: kuoct@mdu.edu.tw

 © 2010 The Japan Society of Applied Physics

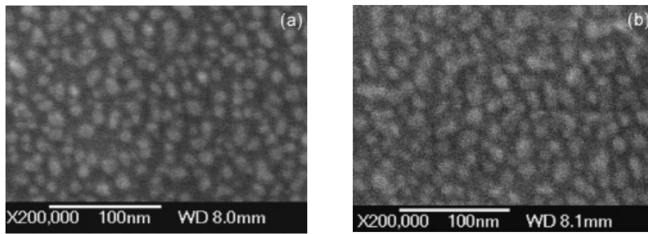

Fig. 2. SEM morphologies of the H-plasma-treated Ni-NCs on Si_3N_4 layer for 3 min treatment time at different microwave powers: (a) 900 and (b) 750 W. The number density of Ni-NCs at 900 W for 3 min (5×10^{11} cm^{-2}) is about one order greater than that at 750 W for 3 min (3.8×10^{10} cm^{-2}), as shown by SEM micrographs in (a) and (b), respectively.

to form a Si_3N_4/SiO_2/poly-Si/SiO_2/Si stack by PECVD with SiH_4, NH_3, and N_2O as reaction gases. For NC formation, an approximately 5 nm wetting layer of pure nickel was deposited on the stack by sputtering and then H-plasma treatment. The distribution and morphology of Ni-NCs were manipulated by varying the process parameters. On top of NCs, a 15-nm-thick SiO_2 blocking dielectric layer was deposited by PECVD, which was followed by O_2 treatment to densify the blocking layer. The TFT stack devices were completed by gate definition with solution etching [(H_3PO_4 : HNO_3 : CH_3COOH : H_2O) = (50 : 2 : 10 : 9)], contact formation, Al electrode patterning, and 400 °C N_2 sintering for 30 min. The gate length and width of the device are ~10 and 100 μm, respectively. Effects of H-plasma treatment conditions on Ni-NC structures were studied. In addition, the effects were characterized and analyzed by scanning electron microscopy (SEM), transmission electron microscopy (TEM), and current–voltage (I–V) measurements.

3. Results and Discussion

Regarding the H-plasma treatment performed to form Ni-NCs, the results show that the dot size and number density of NCs are functions of microwave power (600 to 900 W) and treatment time (1 to 10 min). The dot size and number density result from the competitions among heating ability, etching effect, dot fluidity, and dot agglomeration due to the surface tension effect.[20] Under the present study conditions, the number density of Ni-NCs at 900 W for 3 min (5×10^{11} cm^{-2}) is about one order greater than that at 750 W for 3 min (3.8×10^{10} cm^{-2}), as shown by SEM micrographs in Figs. 2(a) and 2(b), respectively. Effects of H-plasma treatment time on morphologies of Ni-NCs are shown by SEM micrographs in Figs. 3(a)–3(d). Figure 4 shows the corresponding curves of number dot density and average dot diameter versus treatment time for a microwave power of 900 W. This figure also suggests the greatest etching effect, which is the bombardment of NCs out of the surface at the treatment time of 10 min. In other words, the highest number density of NCs is observed at the treatment time of approximately 3 min. In summary, the H-plasma treatment conditions of 900 W for 3 min were chosen for NVM device fabrication.

To examine the device stack, a part of the SiO_2/Si_3N_4/Ni-NCs/SiO_2 stack is shown using the cross-sectional TEM image of the device stack in Fig. 5. It indicates that the layer

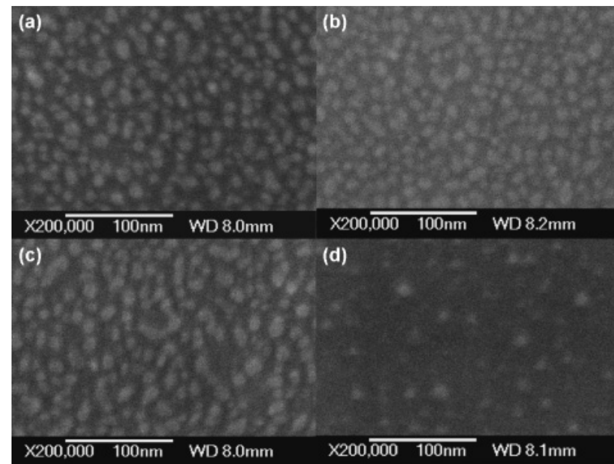

Fig. 3. SEM morphologies of H-plasma-treated Ni-NCs for 900 W microwave power at different treatment times: (a) 1, (b) 3, (c) 5, and (d) 10 min. The figure suggests the greatest etching effect, which is the bombardment of NCs out of the surface at the treatment time of 10 min.

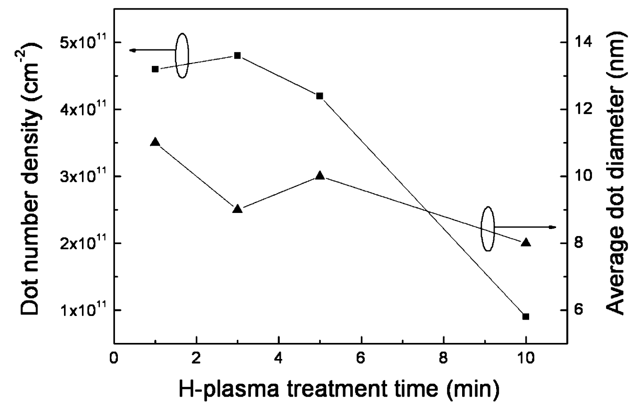

Fig. 4. Curves of dot number density and mean diameter of Ni-NCs versus H-plasma treatment time. The highest number density of NCs is observed at the treatment time of approximately 3 min.

structures in the order from top to bottom are an Al electrode, 20 nm Ni-NCs embedded SiO_2, a 3 nm Si_3N_4 buffer layer, a 7 nm SiO_2 tunneling layer, and a poly-Si channel layer. There are six black dots in Fig. 5 that represent Ni-NCs with sizes ranging from 4 to 9 nm.

The I_D–V_D features with various current densities (maximum is 0.58 μA/μm^2) of the Ni-NC-assisted low-temperature poly-Si thin film transistors (LTPS-TFTs) with gate voltages ranging from 0 to 6 V are depicted in Fig. 6. The features signify that the highest current density in this case is favorable for integrated circuit applications. Figure 7 shows the corresponding four different I_D–V_G curves of these devices with or without Ni-NCs and with gate program-erase biases of 12 V for 1 s and −12 V for 1 s. The V_{TH} shift of the device with Ni-NCs is about 2.2 V in contrast to ~0.1 V for the device without NCs. The V_{TH} shift of 2.2 V is sufficiently high to be sensed as either "1" or "0" by the sensing amplifier. In addition, the on/off current ratio can increase up to 5 orders with an on-current of 10^{-5} A, and the value of the subthreshold swing (SS) can decrease down to ~0.5 V/decade, signifying a rapid response of the device and a low leakage current of the poly-Si channel. The significance

 © 2010 The Japan Society of Applied Physics

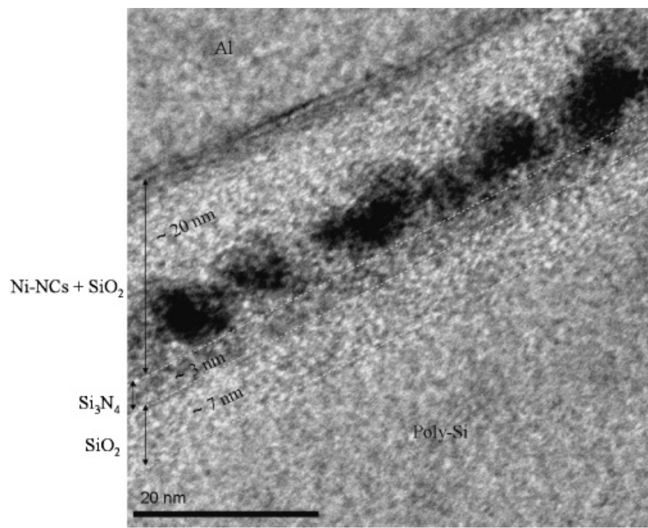

Fig. 5. Typical TEM cross-sectional image of gate stack indicating the following layer structures in the order from top to bottom: Al electrode, 20 nm SiO_2 embedded with Ni-NCs, 3 nm Si_3N_4 buffer layer, 7 nm SiO_2 tunneling layer, and poly-Si channel layer. There are six black dots in this figure that represent Ni-NCs with sizes ranging from 4 to 9 nm.

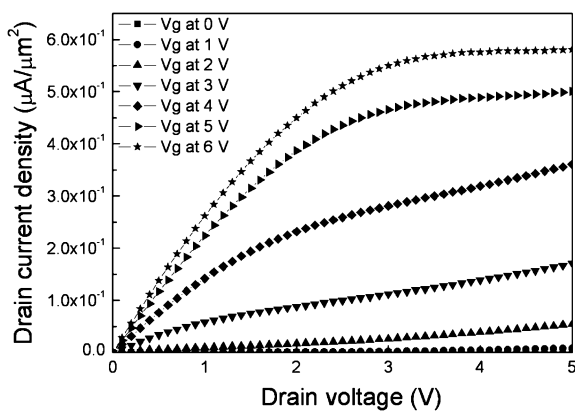

Fig. 6. I_D–V_D curves of Ni-NC TFT-NVM at different gate biases. The highest current density in this case is favorable for integrated circuit applications.

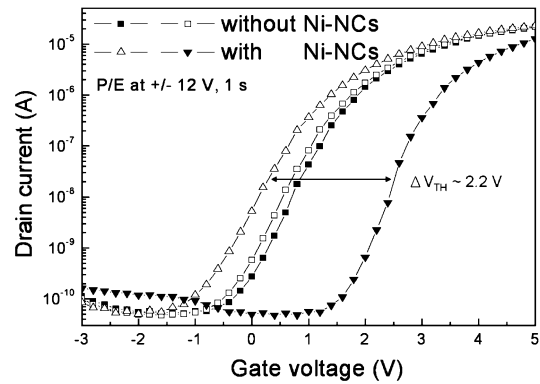

Fig. 7. Four I_D–V_G curves of Ni-NC TFT-NVMs with and without Ni-NCs and with gate program-erase biases of 12 V for 1 s and −12 V for 1 s. The V_{TH} shift of the device with Ni-NCs is about 2.2 V in contrast to ~0.1 V for the device without NCs. The on/off current ratio can increase up to 5 orders with an on-current of 10^{-5} A, and the values of the subthreshold swing (SS) can decrease down to ~0.5 V/decade.

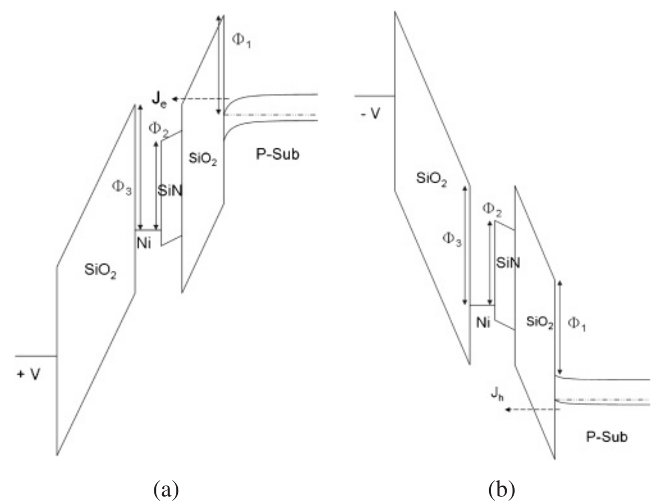

Fig. 8. Band diagrams of device under (a) programming and (b) erasing operations. Using the asymmetric SiO_2/Si_3N_4 tunneling barrier, electrons or holes can be more easily tunneled than only using SiO_2 as the tunneling oxide layer.

of the curves can be understood from the following device functions. When the device is programmed, the electrons are tunneled from the Si substrate through the tunnel oxide layer and trapped in the Ni-NCs. When the device is erased, the holes are tunneled from the Si substrate through the tunnel oxide layer and recombine with the electrons. The function of the top SiO_2 control oxide layer is to prevent the injection of the carriers of the gate electrode into the Ni-NCs by Fowler–Nordheim (FN) tunneling, as shown in Figs. 8(a) and 8(b). However, using the asymmetric SiO_2/Si_3N_4 tunneling barrier, electrons or holes can be more easily tunneled than only using SiO_2 as the tunneling oxide layer. In other words, these devices require a lower operating voltage or a lower power consumption to pump electrons in and out. It can be concluded that the SiO_2/Si_3N_4/Ni-NCs/SiO_2 stack of gate dielectric layers has been demonstrated successfully to manipulate the charging and discharging of electrons in the stack for potential applications in nonvolatile memory devices.

The two curves of retention time versus V_{TH} for TFT-NVMs with Ni-NCs in the device at room temperature are shown in Fig. 9 for two different states. These curves show that the devices with Ni-NCs and the program/erase (P/E) condition of ±12 V for 1 s can maintain a memory window of ~1.1 V for a retention time of 10^4 s. In general, the leakage current of a TFT is a more critical factor in the reverse bias region, known as the Frenkel–Poole (FP) region, in which the trapped electrons can be more easily tunneled out through defects in the tunnel oxide layer by the FP mechanism.[21] In other words, the application of Ni-NCs in the NVM device can improve electron retention through minimizing FP leakage. This may be due to the fact that electrons can be distributed and stored in many NCs, which are insulated to each other to minimize the possibility of simultaneous leakages from all NCs. In addition, the high work function (~5.15 eV) of Ni-NCs yields a deep energy well for storing carriers, enhancing data retention.

 © 2010 The Japan Society of Applied Physics

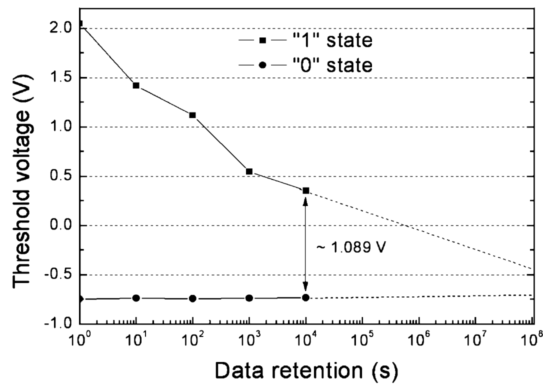

Fig. 9. Data retention curves of Ni-NC-assisted TFT-NVMs for two different data state conditions. The devices with Ni-NCs and the P/E condition of ±12 V for 1 s can maintain a memory window of ∼1.1 V for a retention time of 10^4 s at room temperature.

4. Conclusions

Processes of fabricating Ni-NCs by hydrogen plasma treatment in a CVD system on a Si_3N_4 layer were successfully developed to obtain optimum process parameters for application in LTPS-TFT NVM devices. Results show that an approximately 5-nm-thick Ni film can be used to fabricate NCs with number densities of up to 5×10^{11} cm^{-2} at 900 W for 3 min H-plasma treatment. The corresponding TFT-NVM obtained using Ni-NCs as charge-trapping centers has been successfully demonstrated, indicating the possibility of fabricating a 3D multilayer-stack device below 600 °C for ultrahigh-density nonvolatile memory application. Further improvement of the TFT-NVM can be feasible.

Acknowledgement

The work was supported by the National Science Council, Taiwan, through contract number NSC 98-2221-E-451-001.

1) K. Ichikawa, Y. Uraoka, H. Yano, T. Hatayama, T. Fuyuki, E. Takahashi, T. Hayashi, and K. Ogata: Jpn. J. Appl. Phys. **46** (2007) 661.
2) Z. Jin, S. Jung, N. V. Duy, S. Hwang, K. Jang, K. Lee, J. Lee, P. Hyungjun, J. Kim, H. Son, and J. Yi: Surf. Coat. Technol. **202** (2008) 5637.
3) P. T. Liu, C. S. Huang, and C. W. Chen: Appl. Phys. Lett. **90** (2007) 182115.
4) H. T. Chen, S. I. Hsieh, C. J. Lin, and Y. C. King: IEEE Electron Device Lett. **28** (2007) 499.
5) S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan: Appl. Phys. Lett. **68** (1996) 1377.
6) T. Z. Lu, M. Alexe, R. Scholz, V. Talelaev, and M. Zacharias: Appl. Phys. Lett. **87** (2005) 202110.
7) M. Kanoun, A. Souifi, T. Baron, and F. Mazen: Appl. Phys. Lett. **84** (2004) 5079.
8) Y. Q. Wang, J. H. Chen, W. J. Yoo, Y. C. Yeo, S. J. Kim, R. Gupta, Z. Y. L. Tan, D. L. Kwong, A. Y. Du, and N. Balasubramanian: Appl. Phys. Lett. **84** (2004) 5407.
9) P. Punchaipetch, K. Ichikawa, Y. Uraoka, T. Fuyuki, E. Takahashi, T. Hayashi, and K. Ogata: Jpn. J. Appl. Phys. **45** (2006) 3997.
10) X. B. Lu, P. F. Lee, and J. Y. Dai: Thin Solid Films **513** (2006) 182.
11) F. M. Yang, T. C. Chang, P. T. Liu, U. S. Chen, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou: Appl. Phys. Lett. **90** (2007) 222104.
12) C. C. Wang, J. Y. Wu, Y. K. Chiou, C. H. Chang, and T. B. Wu: Appl. Phys. Lett. **91** (2007) 202110.
13) J. J. Lee, Y. Harada, J. W. Pyun, and D. L. Kwong: Appl. Phys. Lett. **86** (2005) 103505.
14) J. Y. Tseng, C. W. Cheng, S. Y. Wang, T. B. Wu, K. Y. Hsieh, and R. Liu: Appl. Phys. Lett. **85** (2004) 2595.
15) C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, C. W. Hu, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin: Appl. Phys. Lett. **93** (2008) 222101.
16) S. Choi, S. S. Kim, M. Chang, H. Hwang, S. Jeon, and C. Kim: Appl. Phys. Lett. **86** (2005) 123110.
17) J. H. Lee, J. S. Choi, S. Hong, I. Hwang, Y. I. Kim, S. J. Ahn, S. O. Kang, and B. H. Park: Jpn. J. Appl. Phys. **46** (2007) L1246.
18) H. B. Michaelson: J. Appl. Phys. **48** (1977) 4729.
19) C. M. Hsu, C. H. Lin, H. L. Chang, and C. T. Kuo: Thin Solid Films **420** (2002) 225.
20) H. Lee, Y. S. Kang, P. S. Lee, and J. Y. Lee: J. Alloys Compd. **330** (2002) 569.
21) W. J. Tsai, N. K. Zous, C. J. Liu, C. C. Liu, C. H. Chen, T. Wang, S. Pan, C. Y. Lu, and S. H. Gu: IEDM Tech. Dig., 2001, p. 3261.

© 2010 The Japan Society of Applied Physics