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Analysis of Anomalous Capacitance Induced by TAGIDL in p-Channel LTPS TFTs

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In this work, a mechanism of anomalous capacitance in p-channel low temperature polycrystalline silicon thin film transistors (LTPS TFTs) was investigated. In general, the effective capacitance of the LTPS TFTs was only dependent with the overlap area between the gate and source/drain under the off-state. However, the experimental results reveal that the off-state capacitance was increased with decreasing measurement frequency and/or with increasing measurement temperature. By fitting the curve of the drain current vs electric field under off-state region, it was verified that the trap-assisted gate-induced drain leakage (TAGIDL) consists of the Pool–Frenkel emission and thermal field emission. In addition, the charge density calculated from the C_{gsd}-V_g measurement also has the same dependence with electric field. This result demonstrates that the anomalous capacitance is mainly due to the TAGIDL. To suppress the anomalous capacitance, a band-to-band hot electron stress was utilized to reduce the vertical electric field between the gate and the drain. The electric field simulation was also performed by TCAD software.
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Low temperature polycrystalline silicon thin film transistors (LTPS TFTs) have been widely investigated for flat panel applications, such as for active matrix liquid crystal displays and active matrix organic light emitting diode displays[1,2] because the electron mobility of LTPS TFTs is higher than that of conventional amorphous silicon (a-Si) TFTs. Because the maximum process temperature is lower than 600°C, LPTS TFTs can be fabricated on cheap glass. This feature allows the fabrication of a pixel array and peripheral circuits on the same glass substrate. Consequently, this technology becomes more suitable to integrate both the pixel array and peripheral circuits on system-on-panel display,[3,4] and the LTPS TFTs are designed using complementary metal oxide semiconductor inverters. However, in previous papers, the results indicated that large leakage current is an important problem in p-channel LTPS TFTs.[5]

The dominant mechanisms of the leakage current in LTPS TFTs have been widely studied,[6,7] and most of that have been focused on the analyses of current–voltage (*I-V*) transfer characteristics. However, it is rather difficult to investigate the relationship between capacitance–voltage (*C-V*) transfer characteristics and leakage current. Besides, most studies of *C-V* transfer characteristics in LTPS TFTs are mainly reported to monitor the electrical stress induced degradation in the transition region.[8,9] However, the leakage current dependent *C-V* in the off-state region was not investigated carefully. The purpose of this work is to investigate the relationship between the leakage current and *C-V* transfer characteristics in LTPS TFTs. The trap-assisted gate-induced drain leakage (TAGIDL) induced capacitance was observed and verified. In addition, we used an electrical stress to suppress the TAGIDL-induced capacitance and used the simulator TCAD to demonstrate the mechanism.

Experimental

In this work, commercial standard p-channel LTPS TFTs fabricated on a glass substrate with top-gate structures were prepared. First, a 500 nm thick buffer oxide was deposited on the glass. Next, a 50 nm a-Si film was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 380°C on the buffer oxide, followed by dehydrogenation via furnace annealing process at 450°C. Then the a-Si films were crystallized by a 308 nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2. An 80 nm SiO_2 was deposited by PECVD as the gate insulator and 300 nm Mo was deposited as a gate metal by sputtering. After the gate metal definition process, the overlap between the gate and the source/drain regions were defined at 0.75 μm and self-aligned boron implantation with a dose of 2×10^{15} cm^{-2} to form the P^+ regions at source/drain regions. An annealing process was performed to activate the dopant impurities after the source/drain regions implantation. The NH_3 plasma treatment was performed at 300°C to passivate the dangling bonds at the poly-Si/SiO_2 interface and at the grain boundaries. A 500 nm SiN_x layer was deposited as the interlayer dielectric. Finally, the contact holes were patterned by dry etching, and Al metallization was performed. The cross-sectional view of the p-channel LTPS TFT is shown in Fig. 1. The TFTs studied in this work are 16 μm in length and 512 μm in width.

The *I-V* curves and *C-V* curves were measured by an Agilent 4156C semiconductor parameter analyzer and an Agilent 4294A precision LCR meter, respectively. In the *C-V* measurement, the gate-to-source/drain capacitance (C_{gsd}), the gate-to-source capacitance (C_{gs}), and the gate-to-drain capacitance (C_{gd}) with different frequencies were measured.

In the C_{gsd}-V_g measurement, capacitance measurement high was applied to the gate electrode, and both the drain and source electrodes were connected to capacitance measurement low. In addition, the C_{gs}-V_g was measured with a floated drain while C_{gd}-V_g was measured with a floated source.

Results and Discussion

Figure 2 shows the fresh normalized gate-to-source/drain capacitance (C_{gsd}); gate voltage (V_g) transfer characteristics for the p-channel LTPS TFT under different measurement frequencies while temperature was set the 300 K. The normalized capacitance is the ratio of the maximum value of measurement capacitance. Clearly, the C_{gsd}-V_g curves are aligned and independent of different frequencies when the gate bias was swept from −10 to 10 V. However, as the gate bias over than 10 V, the frequency-dependent C_{gsd}-V_g curves were observed. The capacitance value increases both as the gate bias increases and as frequency decreases. As the measurement frequency is 500 Hz, this anomalous capacitance is gradually saturated and reaches a value equivalent to the maximum value of C_{gsd} when V_g was operated at −10 V. In general, when the p-channel

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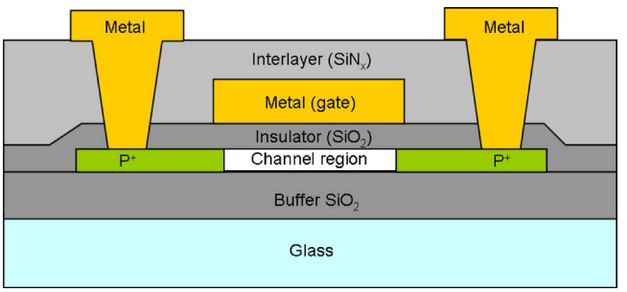

Figure 1. (Color online) Cross-sectional views of p-channel LTPS TFTs.

TFT was operated in an off-state region, the effective capacitance was only dependent with the overlapped region between the gate and the source/drain,[10] which is a frequency-independent constant. In addition, stretching-out *C-V* curves of TFT in the transition region with increasing measurement frequency have also been reported due to the presence of trap states at the gate dielectric/active layer interface in the channel region.[11,12] However, the stretching-out *C-V* curves was not observed in Fig. 2 as the frequency ranged from 500 Hz to 100 kHz. Therefore, the anomalous capacitance was not caused by the interface traps in the channel region.

Figure 3a and b shows the fresh C_{gsd}-V_g transfer characteristics and I_d-V_g transfer characteristics under different measurement temperatures while frequency was set to 500 Hz for the *C-V* measurement and drain bias was fixed at −0.1 V for the *I-V* measurement, respectively. Apparently, the *C-V* curve in the transition region and *I-V* curve in the subthreshold region shifted to the positive direction with increasing temperature. This result indicated that the main conduction mechanism in poly-Si TFTs is the thermionic emission over the grain boundary energy potential barrier V_b, which is a function of the temperature.[13] Besides, in the off-state region from Fig. 3a, the anomalous *C-V* curves showed a strong relationship with temperature. The corresponding voltage, as the anomalous *C-V* occurred, decreased with increasing temperature. As shown in Fig. 3b, the leakage current was increased with both increasing temperature and gate bias in the off-state region. In previous studies, the contribution for the leakage current under the strong electrical field has been reported due to TAGIDL.[14,15] In a high temperature environment or under a high electric field, the TAGIDL can be enhanced by electron hole pair generation via grain boundary traps in the overlap region between the gate and the drain. In general, the mechanisms of the carrier generation are divided into pure field emission, thermionic field emission, and Pool–Frenkel emission.[16] The pure field emission mechanism could be eliminated because the leakage current in our study was strongly dependent on the temperature. Therefore, the Pool–Frenkel effect and thermal field effect are the most likely generation mechanism. The TAGIDL associated with the Pool–Frenkel effect and the thermal field effect is modeled as[17]

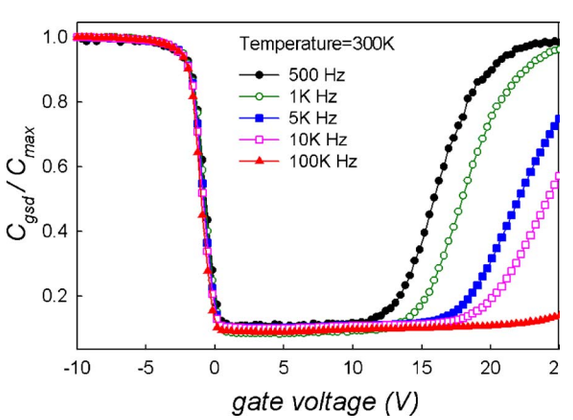

Figure 2. (Color online) C_{gsd}-V_g transfer characteristics of the p-channel LTPS TFT at different frequencies while temperature is 300 K.

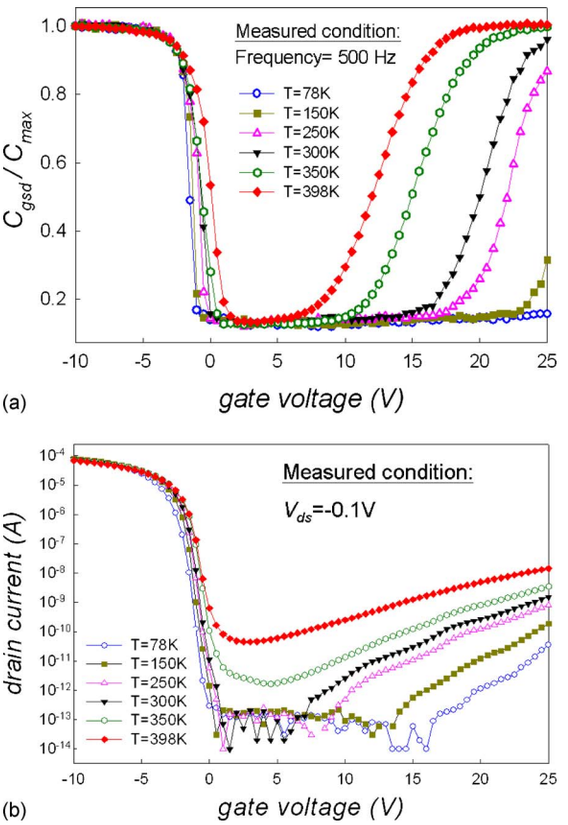

Figure 3. (Color online) (a) C_{gsd}-V_g transfer characteristics of the p-channel LTPS TFT at different temperatures while frequency is 500 Hz, (b) I_d-V_g transfer characteristics at different temperatures while drain voltage is −0.1 V.

$$I_{TAGIDL} = I_o e^{\beta\sqrt{E_m}} \quad [1]$$

where $I_o = qA_j w_D \sigma \upsilon_{th} N_{gb} n_i$, A_j is the depletion area between the gate and source/drain, w_D is the depletion width, σ is the carrier capture cross section (assuming $\sigma_n = \sigma_p = \sigma$), ν_{th} is the carrier thermal velocity, N_{gb} is the grain boundary trap density per unit area distributed throughout the grain, and n_i is intrinsic carrier density. In Eq. 1, β consists of β_{PF} and β_{THE}, which are field enhancement factors arising from the Pool–Frenkel effect and the thermal field effect with expected values of ~0.009 and 0.0011 $cm^{1/2}$ $V^{-1/2}$, respectively, at room temperature.[16]

Considering that the peak electric field E_m at the overlap between the gate and the drain is dominated by the vertical electric field at the interface[18]

$$E_m = \frac{|V_G - V_D - V_{FB}|}{t_{ox}(\varepsilon_{Si}/\varepsilon_{SiO_2})} \quad [2]$$

where ε_{Si} and ε_{SiO_2} are the permittivities of Si and SiO_2, respectively, V_{FB} is the flatband voltage which is defined as the gate voltage that yields the minimum drain current from the transfer characteristic with $V_{ds} = -0.1$ V. The t_{ox} is the thickness of the gate oxide.

Figure 4 shows the plot of ln (TAGIDL) vs $(E_m)^{1/2}$ at V_{ds} of −0.1 V under different temperatures. In all cases, data were fitted with straight lines in the different electric field regions, which were corresponded to the anomalous capacitance in Fig. 3a. It can be seen

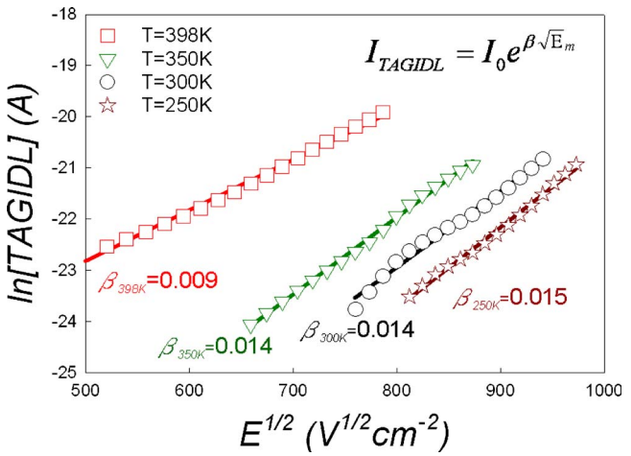

Figure 4. (Color online) Plot of ln (TAGIDL)–$(E_m)^{1/2}$ under different temperatures while drain voltage is −0.1 V.

that value of the β decreases from 0.015 $cm^{1/2}$ $V^{-1/2}$ at 250 K to 0.009 $cm^{1/2}$ $V^{-1/2}$ at 398 K. The result indicated that the main mechanisms of the TAGIDL were the Pool–Frenkel effect and the thermal field effect in this work.

In addition, the charge caused by TAGIDL (Q_{TAGIDL}) can be integrated from the C_{gsd}-V_g measurement in the off-state region, which is based on the reported current equation[19] and given by

$$Q_{TAGIDL} = \int_{V_{g1}}^{V_{g2}} C_{gsd}(V_g)dV_g \quad [3]$$

where the V_{g1} and the V_{g2} in this work are 5 and 25 V, respectively. Figure 5 shows the Q_{TAGIDL}-V_g curves under the different temperatures when the measurement frequency is 500 K Hz. As follows, we analyze the relationship between the Q_{TAGIDL} and the TAGIDL to study the mechanism for the anomalous capacitance, which was extracted by *C-V* and *I-V* measurements, respectively. First, it can be observed from Fig. 3 that the anomalous capacitance is strongly dependent on TAGIDL. As a consequence, the Q_{TAGIDL} associated with E_m was assumed as Eq. 4, which corresponded with Eq. 1

$$Q_{TAGIDL} \approx e^{\beta\sqrt{E_m}} \quad [4]$$

where β is also assumed to consist of β_{PF} and β_{THE}.

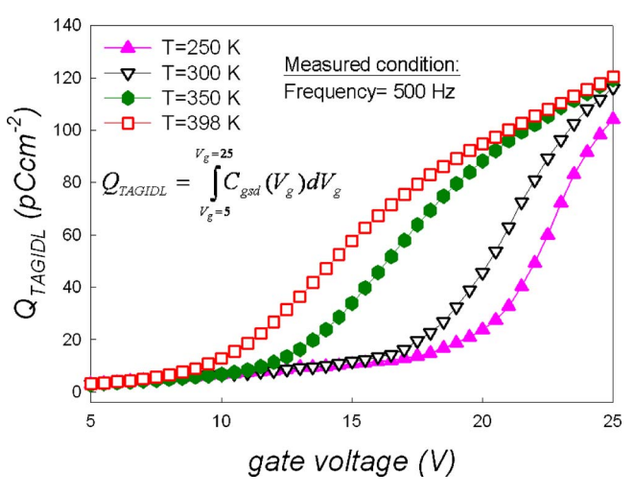

Figure 5. (Color online) Q_{TAGIDL}-$V_{gate\ voltage}$ curves under the different temperatures when the measurement frequency is 500 K Hz.

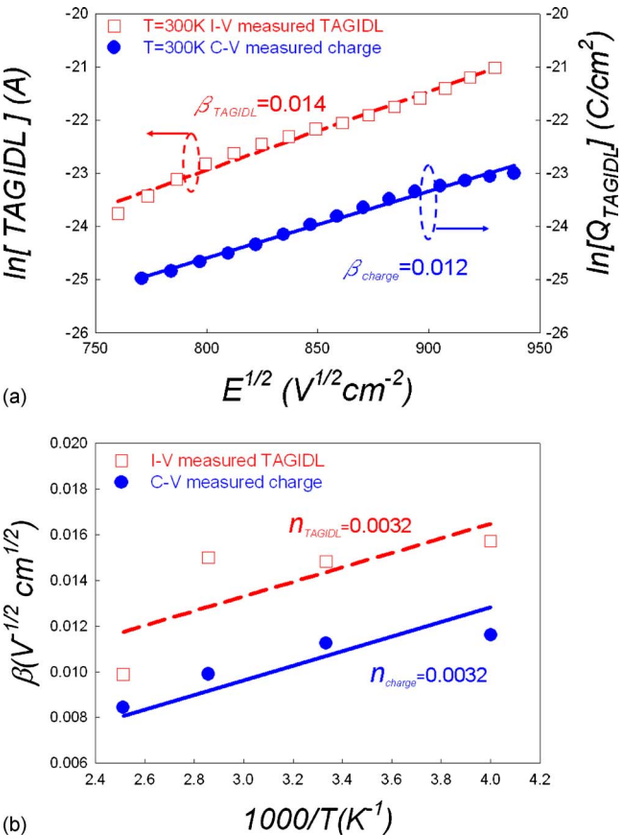

Figure 6. (Color online) (a) Relationship between $(E_m)^{1/2}$, ln (TAGIDL), and ln (Q_{TAGIDL}) when the temperature was 300 K and (b) relationship between the β and the temperatures for TAGIDL and the Q_{TAGIDL}.

Figure 6a shows the relationship between $(E_m)^{1/2}$, ln (TAGIDL), and ln(Q_{TAGIDL}) when the temperature was 300 K. It can be seen that the values of β are similar for the TAGIDL and the Q_{TAGIDL}. Figure 6b shows the corresponding β extracted from the above method at different temperatures, and both the results also exhibit a linear relation with reciprocal temperature and have the same value of *n* (0.0032). Therefore, by these analyses, the principal origination of the carrier generation for the TAGIDL and the Q_{TAGIDL} are identical, which were included in the Pool–Frenkel effect and the thermal field effect.

Figure 7 shows the schematic diagram of a TFT cross section and the energy band diagram along the surface between the drain (P^+) and the gate when the device is operated at the off state. As the gate bias increases, the increase in energy band bending causes a large number of electrons to tunnel to the conduction band. The electrons drifted to the channel region due to the junction electric field between the source/drain and channel region. Additionally, capacitance is directly affected by charge variation. Thus, when the *C-V* is measured at low frequency, the numerous electrons induced by TAGIDL have enough time to flow into the channel region and then cause the charge variation at the poly-Si/SiO_2 interface, which is a reason for the anomalous *C-V* curves in the off-state region.

Our previous study has demonstrated that TAGIDL in n-channel TFTs can be suppressed by band-to-band hot hole (BTBHH) stress.[20] Similarly, band-to-band hot electron (BTBHE) stress has also been used to suppress TAGIDL for p-channel TFTs.[21,22] Figure 8 shows the I_d-V_g curves of p-channel TFTs before and after BTBHE stress with V_{gs} of 20 V and V_{ds} of −20 V for 0.1 s. Because the band-to-band generated electrons were trapped in the gate oxide near the drain junction during the BTBHE stress, the leakage current

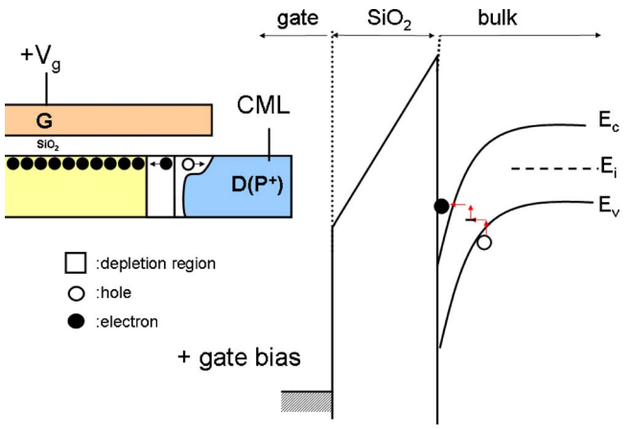

Figure 7. (Color online) Schematic diagram of a TFT cross section and the energy band diagram along the surface between the drain (P^+) and the gate when the device is operated at the off state.

was suppressed due to the reduction of vertical electric field near the trapping area. However, the slight decrease in on-current possibly results from the damage in the interface near drain.

Figure 9a and b shows the normalized C_{gd}-V_g and C_{gs}-V_g curves measurements at initially 500 Hz and after the stresses, respectively. In Fig. 9a, the TAGIDL-induced capacitance was suppressed completely after the BTBHE stress in the C_{gd}-V_g curves. This result can be described by the following series of effects. First, the electrons trapped near the drain due to the BTBHH stress induce two simultaneous effects: a lowering of the vertical electrical field and a reduction of the energy band bending. This reduction of band bending prevents electrons tunneling from the valence band to the conduction band. As a result, TAGIDL-induced capacitance is suppressed. Besides, the minimum capacitance value in the off-state region in the C_{gd}-V_g curves after stress is slightly larger than the value before stress. This result can be explained by the increment in the parasitic capacitance caused by the trap generation at interface near the drain junction.[8,11] Besides, the length of parasitic capacitance in the channel region is 0.2 μm, which is extracted by difference in values of C_{gd} between the initial and the after stress situations. In contrast, the C_{gs}-V_g value was not altered after electrical stress. This is because the electron trapping affects the drain junction only. Consequently, the leakage current due to TAGIDL was not suppressed and it continued to induce the anomalous capacitance effect.

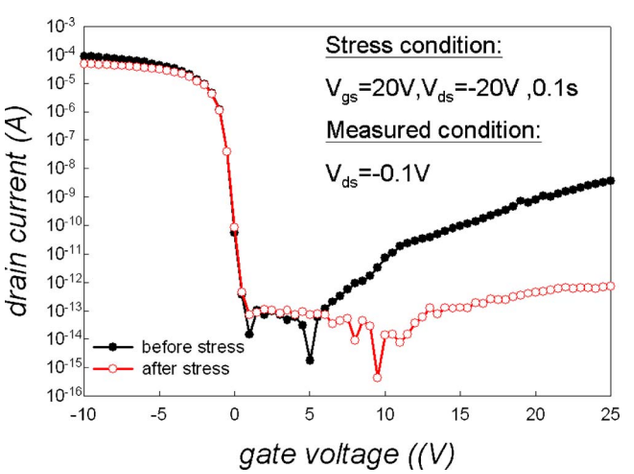

Figure 8. (Color online) I_d-V_g transfer characteristics of the p-channel LTPS TFT both before and after 0.1 s stress.

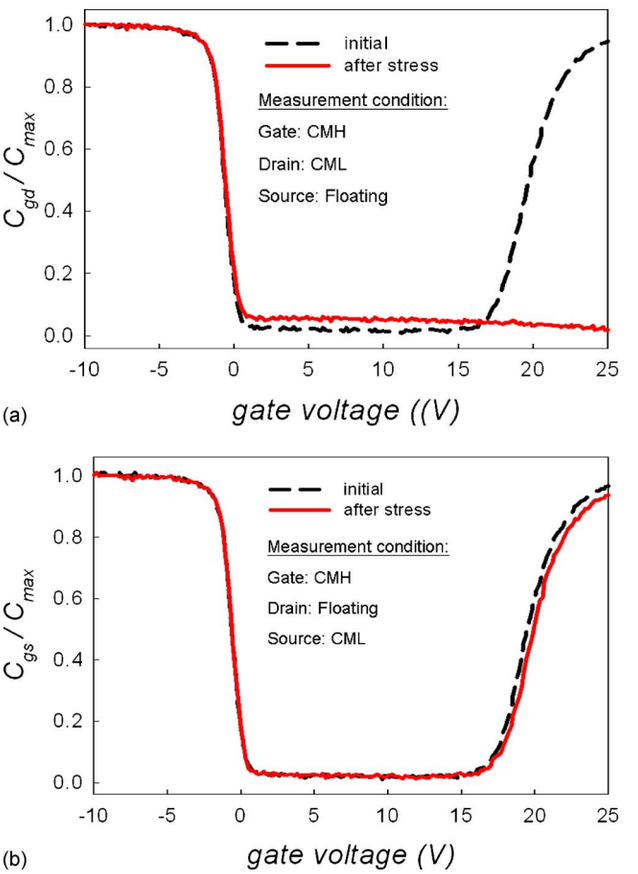

Figure 9. (Color online) *C-V* transfer characteristics of the p-channel LTPS TFT both before and after 0.1 s stress. (a) Gate-to-drain capacitance and (b) gate-to-source capacitance.

In addition, the simulation of an electrical field between the gate and the active layer was performed by the ISE TCAD software. The simulated structure was based on the mentioned device process to set up device information. In this simulation, the doped profiles of source/drain regions were assumed to be Gaussian distribution, and the electrons trapped were assumed to be uniform in the trapped region. The length of trapped region covered the gate/drain overlap region, and the extended length in channel region is 0.2 μm. The trapped electron concentration is assumed o be 4×10^{12} cm^{-2}. Figure 10a and b shows the electric field under the initial situation and electron-trapped situation, respectively. It can be seen that the high

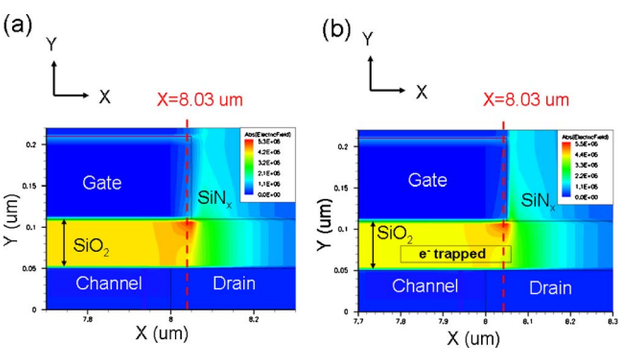

Figure 10. (Color online) Simulation of electrical field from TCAD. (a) Before stress and (b) after stress (electrons trapped).

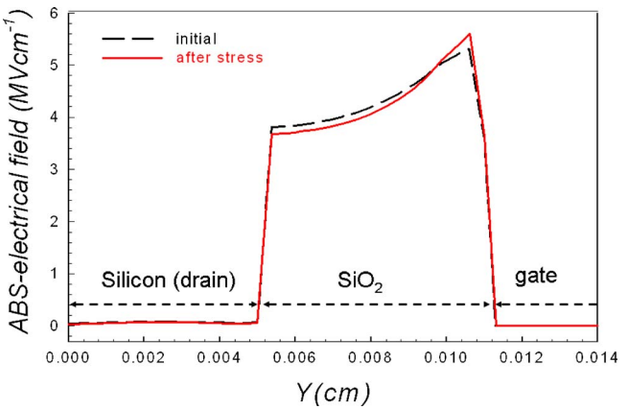

Figure 11. (Color online) Variation in the electrical field against the vertical coordinate (Y) for before stress and after stress conditions when gate voltage was operated at 25 V and lateral coordinate (X) is 8.03 μm.

electrical field occurred in the corner under initial situation and it was liable to induce the TAGIDL. To examine the above statements, the electric field for the initial and electron-trapped conditions at the lateral coordinate (X) of 8.03 μm was monitored. Figure 11 shows the variation in the electrical field against the vertical coordinate (Y) while the gate voltage was 25 V. As shown in Fig. 11, the electrical field between the SiO_2 and silicon after stress was small than in the initial. The simulation result demonstrates that the vertical electric field was indeed reduced by the trapped electrons and this result was consistent with the results in Fig. 8 and 9.

Conclusion

In this work, the mechanism and suppressed method of the anomalous capacitance due to TAGIDL in p-channel LTPS TFTs were investigated. The TAGIDL-induced capacitance is dependent on the temperature and measurement frequencies. The dominant mechanism of the TAGIDL-induced capacitance is verified to consist of the Pool–Frenkel emission and thermal field emission. Moreover, the TAGIDL-induced capacitance is successfully suppressed by BTBHE stress by reducing the vertical electric field between the gate and the drain. The reason of the suppression is consistent with the result of the simulation.

Acknowledgments

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