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The Characteristics of n- and p-Channel Poly-Si Thin-Film Transistors with Fully Ni-Salicided S/D and Gate Structure

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n- and p-channel poly-Si thin-film transistors with fully Ni-self-aligned silicided (fully Ni-salicided) source/drain (S/D) and gate structure (n- and p-channel FUSA-TFTs) have been successfully fabricated on a 40 nm thick channel layer. The conventional poly-Si gate is replaced by the fully Ni-silicided gate, and the parasitic S/D resistance of the FUSA-TFTs is significantly reduced by the fully Ni-silicided S/D structure. The fully Ni-salicidation process is executed at a low temperature of 500°C for a short rapid thermal annealing time. Experimental results show that the FUSA-TFTs give increased on/off current ratio, improved subthreshold characteristics, less threshold voltage roll-off, lower parasitic S/D resistance, higher gate capacitance, and larger field-effect mobility than conventional TFTs. The FUSA-TFTs effectively suppress the floating-body effect and parasitic bipolar junction transistor action. The characteristics of the FUSA-TFTs are suitable for three-dimensional integration applications and high performance driver circuits in the active-matrix liquid crystal displays.
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Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many potential applications including three-dimensional (3D) integration high density flash memories, pixel driving elements in active-matrix organic light emitting diodes and integrated peripheral driving circuits, and addressing elements of active-matrix liquid crystal displays (AMLCDs).[1-4] However, the output characteristics exhibit an anomalous increase in current in the saturation regime, often called the "kink" effect by analogy with silicon-on-insulator (SOI) devices.[5-7] This phenomenon can be attributed to the floating-body effect[8] and avalanche multiplication enhanced by grain boundary traps,[6] particularly in n-channel TFTs. With increasing drain voltage, the added drain current enhances impact ionization and the parasitic bipolar junction transistor (BJT) effect, which leads to a premature breakdown in return.[8] In the floating-body thin-film devices, the improved parasitic BJT effect can be achieved by using deep salicidation and a fully silicided source/drain (S/D) structure.[9,10]

Due to low hole field-effect mobility, p-channel TFTs have a lower on-state current than n-channel TFTs. Nevertheless, p-channel TFTs have advantages, such as a lower off-state leakage current, slighter floating-body and kink effects, a weaker drain impact ionization, and a higher hot carrier reliability. In addition, thin-channel poly-Si TFTs have better device characteristics such as a small leakage current and a suppressed floating-body effect than thick-channel poly-Si TFTs.[11] However, a thin-channel film also leads to increased parasitic S/D resistance. Parasitic S/D resistances become an increasingly serious issue for thin-channel poly-Si TFTs and SOI devices. Several methods such as self-aligned silicide, selective tungsten-clad and metal-replaced junction technology have been proposed to reduce parasitic S/D resistance in thin-channel SOI devices and poly-Si TFTs.[12-15]

Silicided and metal gates have a higher capacitance than poly-Si gates due to the elimination of poly-Si depletion.[16-18] Field-effect mobility and on-state current in such gates can be improved by reducing parasitic S/D resistance and increasing gate capacitance.[14,15] In this paper, n- and p-channel poly-Si thin-film transistors with fully Ni-self-aligned silicided (fully Ni-salicided) S/D and gate structure (n- and p-channel FUSA-TFTs), whose S/D and gate poly-Si layers are completely silicided with Ni, have been successfully fabricated on a 40 nm thick channel layer.[19,20] The low resistance fully Ni-salicided S/D and gate permits a significant recovery of the intrinsic characteristics of thin-channel TFTs. We also find that the floating-body and parasitic BJT effects can be significantly suppressed by FUSA-TFTs.

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Experimental

Figure 1 shows the main fabrication process steps of FUSA-TFTs. First, a 40 nm amorphous silicon (a-Si) layer was deposited by low pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafers. The a-Si layer was then crystallized by solid-phase crystallization at 600°C for 24 h. After the patterning of the active region, a 50 nm tetraethoxysilane (TEOS) gate oxide layer was deposited by LPCVD. Next, a 50 nm a-Si gate layer, along with a 100 nm Si_3N_4 layer as the hard mask, was deposited by LPCVD. Then, the a-Si gate layer was crystallized into poly-Si after the deposition of a Si_3N_4 hard mask layer at 780°C for 1 h.

The a-Si gate layers were divided into in situ n^+ phosphorus-doped or undoped gates in n-channel FUSA-TFTs. The a-Si gate layer was an undoped gate in p-channel FUSA-TFTs. Due to experimental equipment limitations, p-channel FUSA-TFTs with in situ p^+ boron-doped gates were not fabricated in our experiments.

After defining the gate electrode, self-aligned S/D implantation was used to form the n^+/p^+ with P^+/BF_2^+ to dose 5×10^{15} cm^{-2} for n-/p-channel (Fig. 1a). Dopants were activated by rapid thermal annealing (RTA) at 600°C for 120 s for short channel FUSA-TFTs. A 150 nm TEOS oxide was deposited and etched to form the sidewall spacer. The Si_3N_4 hard mask layer was then selectively etched in a hot phosphoric acid bath (Fig. 1b). A Ni film of about 40 nm was deposited by sputtering, and then a fully Ni-salicided process was carried out at 500°C for 60 s by a one-step RTA in the N_2 ambient. The fully Ni-silicided S/D and gate structure was formed by the fully Ni-salicided process (Fig. 1c). In addition, we used thin Ni film (about 15 nm) to form partially salicided n-channel TFTs with in situ doped gates. The V_{th} differences between partially salicided n-channel TFTs and n-channel FUSA-TFTs with in situ doped gates are also studied in this paper.

Conventional devices with self-aligned n^+ S/D and without Ni-salicidation were also fabricated to serve as controls. After the contact and metallization processes, NH_3 plasma treatments were implemented after sintering at 400°C for 30 min. Plasma treatment has long been used in TFT devices. A suitable plasma treatment can improve the electrical characteristics of TFT devices due to the generation of H atoms in NH_3 plasma, which effectively passivates defects in poly-Si TFTs.[21,22] The sintering process has also long been used in the fabrication of semiconductor devices for reducing the contact resistance between the metal and the semiconductor. Sintering was performed in atmospheric pressure N_2 ambient diluted

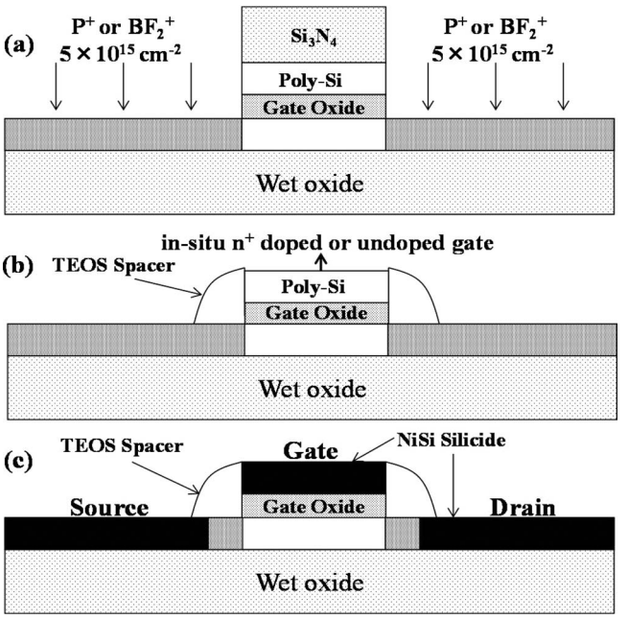


Figure 1. Main process flow of FUSA-TFTs.

with 5% H_2. The H atoms generated during the sintering process passivate the defects in the metal/semiconductor interface.[23]

Results and Discussion

FUSA process.— Cross-sectional transmission electron microscopy (TEM) micrographs of FUSA-TFTs are shown in Fig. 2. The gate and S/D of FUSA-TFTs were fully Ni-salicided. In our study, we used a sufficiently thick Ni film (about 40 nm) to achieve fully Ni-salicided TFTs. According to the volume ratio of Ni-silicidation, a typical 30–40 nm thick Ni film can completely convert the 50 nm thick poly-Si to fully Ni-silicided. To ensure a fully Ni-salicided S/D and gate, we chose a 40 nm thick Ni film and a one-step RTA at 500°C for 60 s. To form fully Ni-salicided TFTs, the duration of RTA must be adequate. The key factor in the process is the balance between the TEOS spacer length and the RTA conditions. When the TEOS spacer length is longer than the lateral diffusion length of the Ni-silicidation, S/D n^+ or p^+ junction can be left to avoid the formation of the Schottky barrier junction. When the Ni-silicided edge is too close to the S/D n^+ or p^+ junction edge, due to an inappropriate high temperature and an overly long RTA process, an abnormally high off-state leakage current (I_{off}) and gate-induced-drain leakage (GIDL)-like current occur.[24,25]

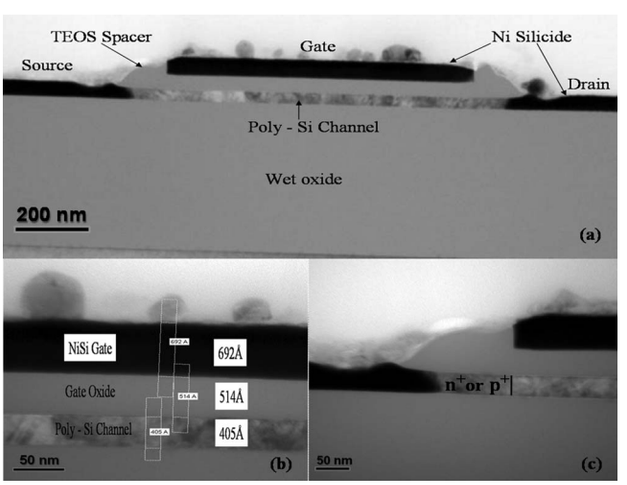


Figure 2. Cross-sectional TEM micrographs of FUSA-TFTs with gate length of 0.8 μm and channel thickness of 40 nm.

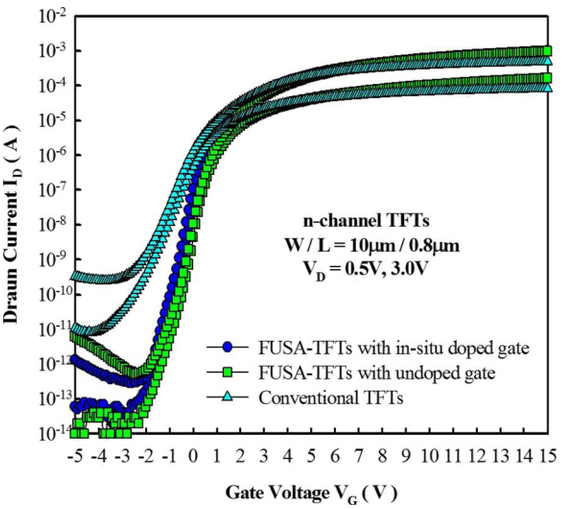


Figure 3. (Color online) Measured transfer characteristics of n-channel conventional and n-channel FUSA-TFTs with W/L = 10/0.8 μm.

n-Channel FUSA-TFTs.— The measured transfer characteristics and field-effect mobility of the n-channel conventional and the n-channel FUSA-TFTs with W/L = 10/0.8 μm are shown in Fig. 3 and 4, respectively. The on-state currents and field-effect mobility in the FUSA-TFTs are higher than those of the conventional TFTs, while the off-state leakage currents of the FUSA-TFTs are lower than those of the conventional TFTs. The on-state currents are significantly degraded by the parasitic S/D resistance in short channel conventional TFTs. The field-effect mobility plotted in Fig. 4 is obtained from the channel conductance at V_D = 0.5 V. For conventional TFTs with a short gate length of 0.8 μm, the field-effect mobility is seriously decreased when gate voltage $V_G > 2.5$ V, but this effect is not found in short channel FUSA-TFTs. The high field-effect mobility of FUSA-TFTs can be maintained with large gate

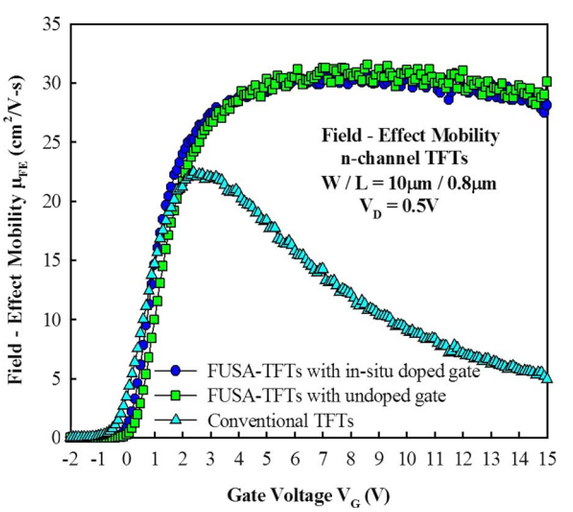


Figure 4. (Color online) Field-effect mobility of n-channel conventional and n-channel FUSA-TFTs with W/L = 10/0.8 μm.

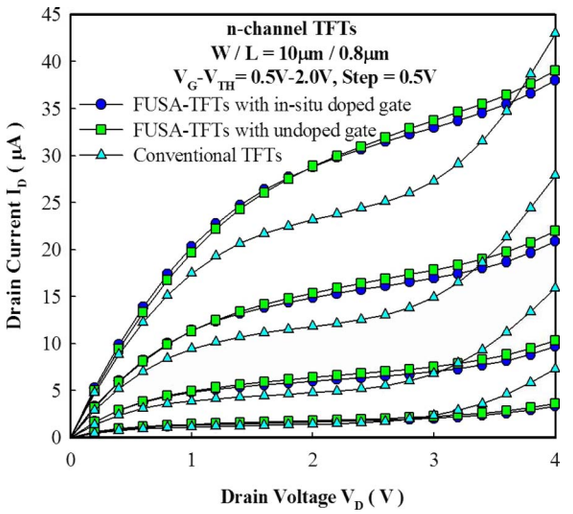


Figure 5. (Color online) Measured output characteristics of n-channel conventional and n-channel FUSA-TFTs with W/L = 10/0.8 μm.

voltages. This improvement is due to the fully Ni-salicided S/D and gate structure, which has a smaller parasitic S/D resistance, higher capacitance, and better scalability than conventional TFTs with poly-Si gates.[15] The superiority of the FUSA-TFTs may also be found in the subthreshold swing (SS). We believe that this is due to the higher gate capacitance in the FUSA-TFTs.

The measured output characteristics of the n-channel conventional and the n-channel FUSA-TFTs with W/L = 10/0.8 μm are shown in Fig. 5. Under a high drain voltage, the strong drain impact ionization causes a profound kink effect and induced parasitic BJT action, which results in decreased drain breakdown voltage due to the floating-body effect in conventional TFTs.[26-29] Silicidation is a well-known method for suppressing the floating-body effect because the silicide layer near the S/D junction works as a sink and an effective lifetime killer for holes.[9,10] Figure 6 illustrates the relationship between the V_{th} shift (ΔV_{th}) and V_D for the n-channel conventional and the n-channel FUSA-TFTs with W/L = 10/0.8 μm. The reference voltage is V_{th} at V_D = 0.5 V. The enhanced ΔV_{th} at high drain voltage is observed in conventional TFTs. The reduced kink

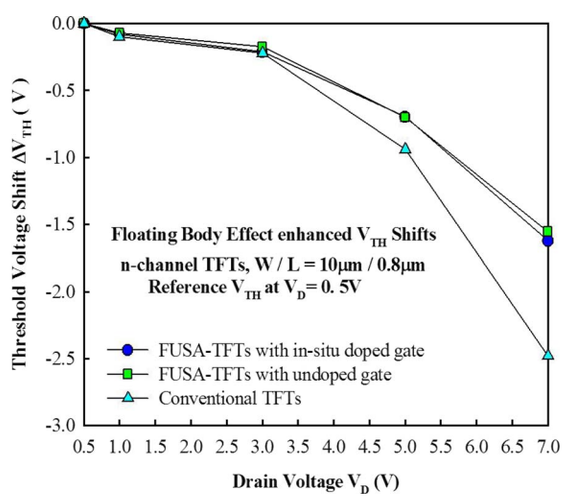


Figure 6. (Color online) Threshold voltage shift (ΔV_{th}) vs drain voltage V_D characteristics for the n-channel conventional and the n-channel FUSA-TFTs with W/L = 10/0.8 μm. The reference voltage is V_{th} at V_D = 0.5 V.

effect, increased drain breakdown voltage, and decreased ΔV_{th} of FUSA-TFTs clearly demonstrate that floating-body and parasitic BJT effects can be significantly suppressed by the fully silicided S/D structure.

To demonstrate that parasitic S/D resistance can be greatly reduced by the fully Ni-salicided process, the parasitic resistance R_P of (a) n-channel FUSA-TFTs with in situ doped gates, (b) n-channel FUSA-TFTs with undoped gates, and (c) n-channel conventional TFTs, in the linear region, is extracted by plotting the measured on-state resistance (R_{on}) vs gate length (L_G), as shown in Fig. 7. The relationship between R_{on} and L across different gate biases may be expressed by several straight lines that extend to merge at a characteristic length L_O representing the accumulation channel in the LDD (and S/D) area and having a residual value of gate-voltage-independent parasitic resistance R_P.[12] The R_P of FUSA-TFTs with an in situ doped gate and an undoped gate is roughly 437 and 372 Ω, respectively. The L_O of FUSA-TFTs with either in situ doped gate or undoped gate is close to 0 μm. The R_P of conventional TFTs is extracted by the same method and is about 5.78 kΩ. Therefore, the on-state currents and field-effect mobility are greatly improved by reducing R_P in the n-channel FUSA-TFTs.

Figure 8 displays the on/off current ratio (I_{on}/I_{off}) of the n-channel conventional and the n-channel FUSA-TFTs with W = 10 μm. The on-state current is defined as the drain current (I_D) at V_G = 10.0 V, V_D = 3.0 V, and the off-state current is defined as the minimum drain current (I_{min}) at V_D = 3.0 V. The I_{on}/I_{off} (10^8–10^9) can be increased by scaling down the gate length in FUSA-TFTs. Because the V_{th} of FUSA-TFTs with in situ doped gates is smaller than the V_{th} of FUSA-TFTs with undoped gates, the I_{on}/I_{off} of FUSA-TFTs with in situ doped gates is larger than the I_{on}/I_{off} of FUSA-TFTs with undoped gates. The I_{on}/I_{off} (10^6–10^7) of conventional TFTs becomes limited as the gate length is scaled down. The enhancement of off-state leakage currents is observed in short channel conventional TFTs. The off-state leakage currents of the conventional TFTs increase as the gate length is scaled down. The enhanced off-state leakage current is due to the amplification of GIDL currents caused by floating-body and parasitic BJT effects in short channel devices.[30] Because the FUSA-TFTs effectively suppress the floating-body effect, the enhancement of GIDL currents can be eliminated in short channel devices.

Figure 9 shows the extracted threshold voltage V_{th} of the n-channel conventional and the n-channel FUSA-TFTs for different gate lengths (defined as $I_D = W/L \times 100$ nA at V_D = 0.5 V). The roll-off of V_{th} is greatly improved in FUSA-TFTs. With this fully Ni-salicided structure, floating-body and parasitic BJT effects can be suppressed, resulting in a stable V_{th} and a lower off-state leakage current in the FUSA-TFTs.[31,32] Figure 9 also shows the V_{th} difference between the FUSA-TFTs with an in situ n^+ doped gate and the FUSA-TFTs with an undoped gate. The V_{th} difference is observed with additional P^+ dopants in the FUSA-TFTs with an in situ n^+ doped gate. The fully Ni-silicided process induced segregation of the impurities from poly-Si to the silicide interface leads to a submonolayer segregation of the dopants, causing a change in the apparent NiSi work function shift.[16,33]

Further, we also used thin Ni film (about 15 nm) to form partially salicided TFTs with in situ doped gates. The partially salicided TFTs were formed by RTA at 550°C for 30 sec. Figure 10 displays the extracted V_{th} roll-off of the n-channel FUSA-TFTs with in situ doped gates and n-channel partially salicided TFTs with in situ doped gates. The n-channel FUSA-TFTs with an in situ doped gate have a more positive V_{th} than the partially salicided TFTs. We also found that short channel (L_G = 1–0.8 μm) partially salicided TFTs display a reverse V_{th} change approximately equal to the V_{th} of the short channel FUSA-TFTs. This result indicates that a shorter RTA time is required to achieve the fully Ni-silicided gate in short channel poly-Si TFTs, compared to long channel poly-Si TFTs. If we use a thinner Ni film to achieve the fully Ni-salicided TFTs, we need a

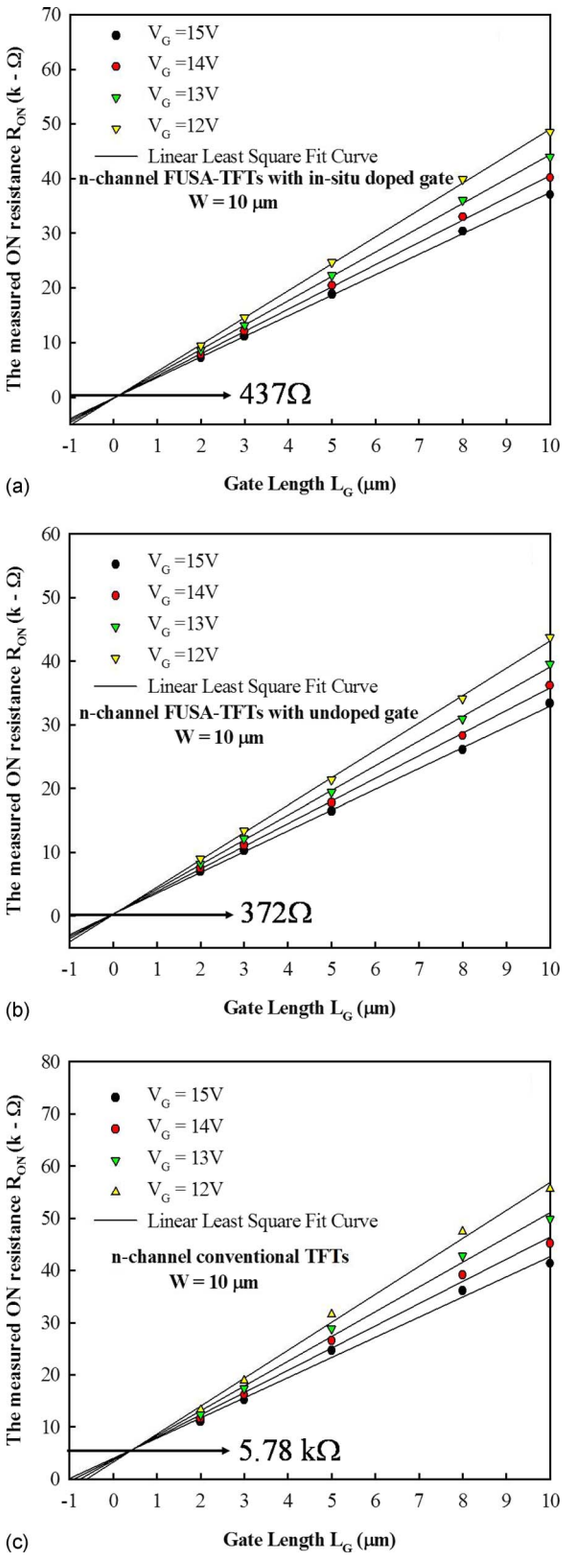


Figure 7. (Color online) The parasitic resistance R_P of (a) n-channel FUSA-TFTs with in situ doped gate, (b) n-channel FUSA-TFTs with undoped gate, and (c) n-channel conventional TFTs, in the linear region, is extracted by plotting the measured on-state resistance (R_{on}) vs gate length (L_G).

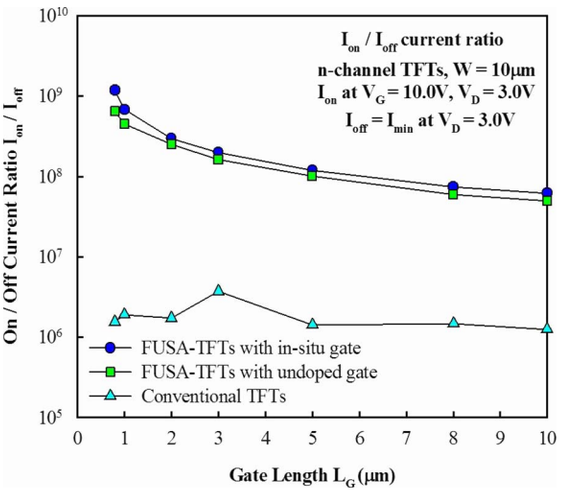


Figure 8. (Color online) On/off current ratio (I_{on}/I_{off}) of n-channel conventional and n-channel FUSA-TFTs with W = 10 μm. On-state current is defined as drain current (I_D) at V_G = 10.0 V, V_D = 3.0 V; off-state current is defined as minimum drain current (I_{min}) at V_D = 3.0 V.

higher RTA temperature or a longer RTA time to ensure that the S/D and gate are fully Ni-salicided across all gate lengths.

p-Channel FUSA-TFTs.— The measured transfer characteristics and field-effect mobility of the p-channel conventional and the p-channel FUSA-TFTs with W/L = 10/0.8 μm are shown in Fig. 11 and 12, respectively. In short channel p-channel TFTs, the on-state currents and field-effect mobility of the FUSA-TFTs are higher than in the conventional TFTs, while the off-state leakage currents of FUSA-TFTs are slightly lower than in the conventional TFTs. The improvement in the electrical characteristics of the p-channel FUSA-TFTs is similar to that seen in the n-channel FUSA-TFTs, except for the improvement in off-state leakage currents. The on-state currents are significantly limited by the parasitic S/D resistance in short channel conventional TFTs. For the conventional TFTs with a short gate length of 0.8 μm, the field-effect mobility is seriously degraded when gate voltage $V_G > -9.0$ V, but this effect is not seen in short channel FUSA-TFTs. The high field-effect mobility of p-channel FUSA-TFTs is due to the fully Ni-salicided S/D and gate

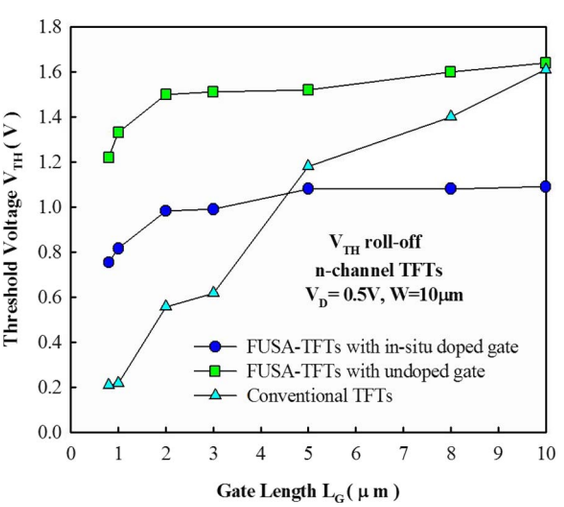


Figure 9. (Color online) Extracted V_{th} roll-off of n-channel conventional and n-channel FUSA-TFTs with different gate lengths (V_{th} is defined as I_D = W/L × 100 nA at V_D = 0.5 V).

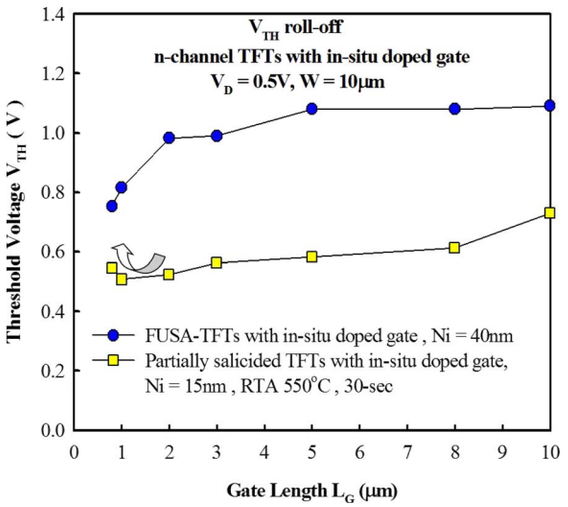


Figure 10. (Color online) Extracted V_{th} roll-off of n-channel FUSA-TFTs with in situ doped gates and n-channel partially salicided TFTs with in situ doped gates. The partially salicided TFTs were formed by RTA at 550°C for 30 s.

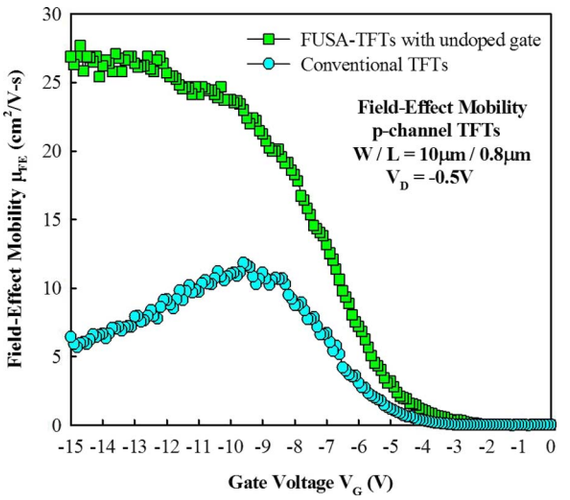


Figure 12. (Color online) Field-effect mobility of p-channel conventional and p-channel FUSA-TFTs with W/L = 10/0.8 μm.

structure, which offers a smaller parasitic S/D resistance, higher capacitance, and better scalability than the conventional TFTs with poly-Si gates.[16] The p-channel FUSA-TFTs also show improved subthreshold characteristics.

The measured output characteristics of the p-channel conventional and the p-channel FUSA-TFTs with W/L = 10/0.8 μm are shown in Fig. 13. Obviously FUSA-TFTs exhibit larger driving currents than conventional TFTs in short channel devices. The high driving currents of the FUSA-TFTs can be attributed to the fully Ni-salicided S/D and gate structure. The short channel FUSA-TFTs have more saturated output characteristics and increased drain breakdown voltage than the conventional TFTs. These findings provide strong evidence that parasitic BJT effects in p-channel TFTs are significantly suppressed by the fully silicided S/D structure.[10]

The parasitic resistance R_P of (a) p-channel FUSA-TFTs with undoped gates and (b) p-channel conventional TFTs, in the linear region, is extracted by plotting the measured on-state resistance (R_{on}) vs gate length (L_G), as shown in Fig. 14. The R_P of FUSA-TFTs with undoped gates is about 387 Ω, while their L_O is close to 0 μm. The R_P of conventional TFTs is about 8.8 kΩ. Therefore, the on-state currents and field-effect mobility are significantly improved by reducing R_P in the p-channel FUSA-TFTs.

Figure 15 displays the on/off current ratio (I_{on}/I_{off}) of the p-channel conventional and the p-channel FUSA-TFTs with W = 10 μm. The on-state current is defined as drain current (I_D) at $V_G = -15.0$ V, $V_D = -3.0$ V, and the off-state current is defined as minimum drain current (I_{min}) at $V_D = -3.0$ V. The I_{on}/I_{off} (10^8–10^9) can be increased when the gate length in FUSA-TFTs is reduced. Unlike n-channel conventional TFTs, the I_{on}/I_{off} (10^7–10^8) of p-channel conventional TFTs increases as gate length is scaled down. The enhancement of off-state leakage currents is not observed in short channel p-channel conventional TFTs due to the weak drain impact ionization and a slight floating-body effect.

Figure 16 displays the extracted V_{th} of the p-channel conventional and the p-channel FUSA-TFTs across different gate lengths (defined as $I_D = W/L \times 10$ nA at $V_D = -0.5$ V). The V_{th} roll-off is greatly improved in the FUSA-TFTs. The threshold voltage absolute values $|V_{th}|$ of FUSA-TFTs are smaller than in conventional TFTs

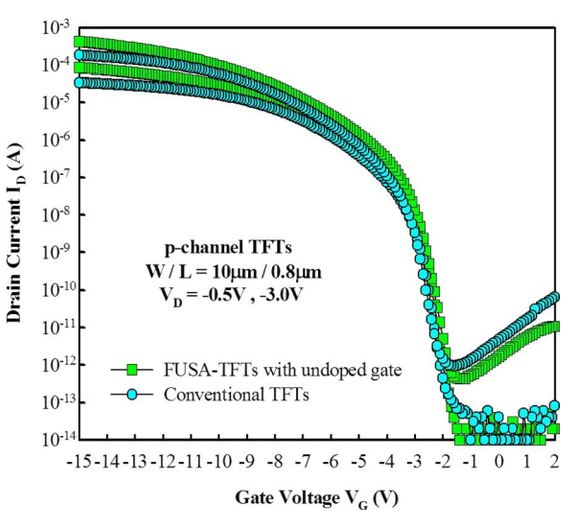


Figure 11. (Color online) Measured transfer characteristics of p-channel conventional and p-channel FUSA-TFTs with W/L = 10/0.8 μm.

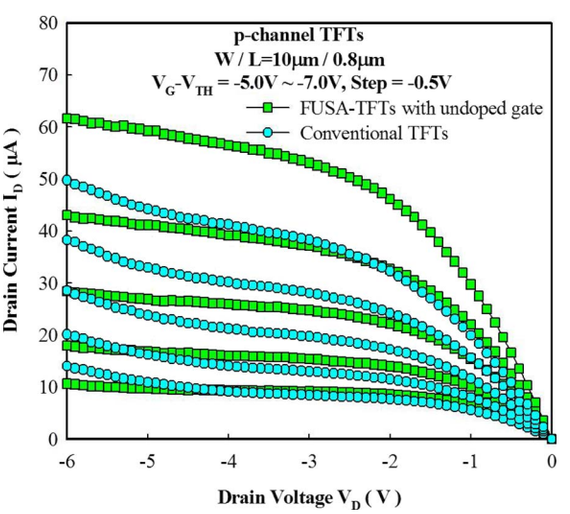
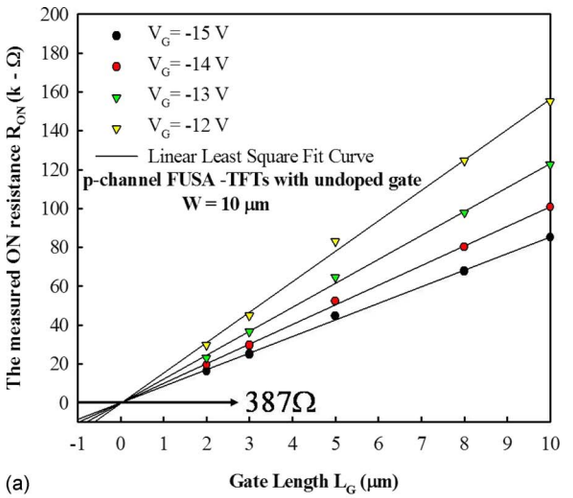


Figure 13. (Color online) Measured output characteristics of p-channel conventional and p-channel FUSA-TFTs with W/L = 10/0.8 μm.



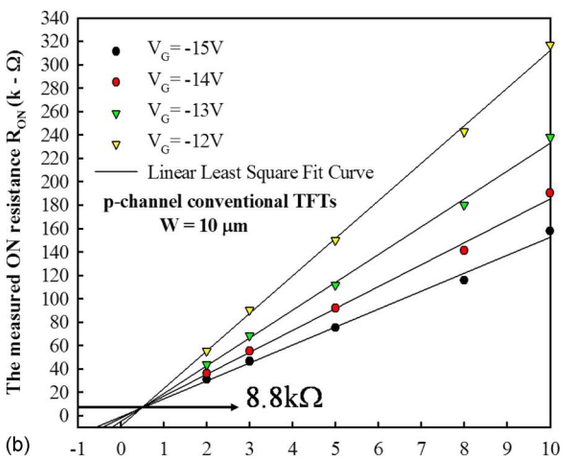


Figure 14. (Color online) The parasitic resistance R_P of (a) p-channel FUSA-TFTs with undoped gates and (b) p-channel conventional TFTs, in the linear region, is extracted by plotting the measured on-state resistance (R_{on}) vs gate length (L_G).

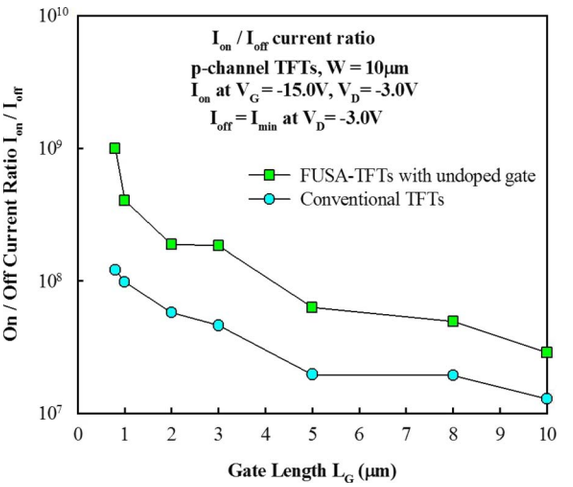


Figure 15. (Color online) On/off current ratio (I_{on}/I_{off}) of p-channel conventional and p-channel FUSA-TFTs with W = 10 μm. On-state current is defined as drain current (I_D) at V_G = −15.0 V, V_D = −3.0 V; off-state current is defined as minimum drain current (I_{min}) at V_D = −3.0 V.

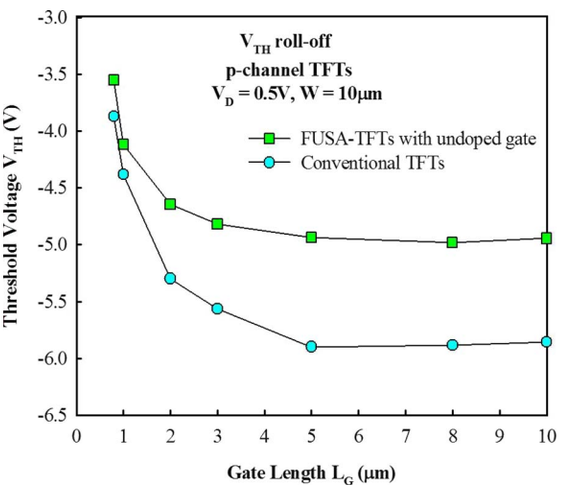


Figure 16. (Color online) Extracted V_{th} roll-off of p-channel conventional and p-channel FUSA-TFTs with different gate lengths (V_{th} is defined as I_D = W/L × 10 nA at V_D = −0.5 V).

due to the improved SS of the FUSA-TFTs. We believe that the stable V_{th} and the improved SS of the p-channel FUSA-TFTs result from the fully Ni-salicided S/D and gate structure.

Conclusions

We have developed n- and p-channel FUSA-TFTs. In n-channel TFTs, the FUSA-TFTs show reduced kink effect, increased drain breakdown voltage, stable V_{th} roll-off, improved SS, lower parasitic S/D resistance, higher field-effect mobility, and increased on/off current ratio compared to conventional TFTs. The p-channel FUSA-TFTs were also fabricated with improved device performance. The parasitic resistance of S/D and gate is greatly reduced, making it possible to recover the intrinsic characteristics of thin-channel TFTs. In this paper, FUSA-TFTs with low thermal budget fully Ni-salicided processes are shown to be a very promising structure with low parasitic S/D resistance and high gate capacitance ability, suitable for 3D integration applications and high-performance driver circuits in the AMLCDs.

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References

1. A. J. Walker, S. Nallamothu, E. H. Chen, M. Mahajani, S. B. Herner, M. Clark, J. M. Cleeves, S. V. Dunton, V. L. Eckert, J. Gu, et al., in *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 29–30 (2003).
2. T. Shimoda, H. Ohshima, S. Miyashita, M. Kimura, T. Ozawa, I. Yudasaka, H. Kobayashi, R. H. Friend, J. H. Burroughes, and C. R. Towns, in *Proceedings of the Asian Symposium on Information Display*, p. 217 (1998).
3. A. G. Lewis, I.-W. Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, *Tech. Dig. - Int. Electron Devices Meet.*, **1990**, 843.
4. H. Oshima and S. Morozumi, *Tech. Dig. - Int. Electron Devices Meet.*, **1989**, 157.
5. M. Koyanagi, H. Kurino, T. Hashimoto, H. Mori, K. Hata, Y. Hiruma, T. Fujimori, I.-W. Wu, and A. G. Lewis, *Tech. Dig. - Int. Electron Devices Meet.*, **1991**, 571.
6. M. Hack and A. G. Lewis, *IEEE Electron Device Lett.*, **12**, 203 (1990).
7. J. P. Colinge, *IEEE Electron Device Lett.*, **9**, 97 (1988).
8. M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, *IEEE Trans. Electron Devices*, **44**, 2234 (1997).
9. F. Deng, R. A. Johnson, W. B. Dubbeldav, G. A. Garcia, P. M. Asbeck, and S. S. Lau, in *Proceedings of the IEEE International SOI Conference*, IEEE, p. 78 (1996).

10. T. Ichimori and N. Hirashita, *IEEE Trans. Electron Devices*, **49**, 2296 (2002).
11. M. Miyasaka, T. Komatsu, W. Itoh, A. Yamaguchi, and H. Ohshima, *Jpn. J. Appl. Phys., Part 1*, **35**, 923 (1996).
12. H. W. Zen, T. C. Chang, P. S. Shih, D. Z. Peng, P. Y. Kuo, T. Y. Huang, C. Y. Chang, and P. T. Lin, *IEEE Electron Device Lett.*, **24**, 509 (2003).
13. K. H. Lee, J. K. Park, and J. Jang, *IEEE Trans. Electron Devices*, **45**, 2548 (1998).
14. D. Zhang and M. Wong, *IEEE Electron Device Lett.*, **27**, 269 (2006).
15. J. Chen, J. P. Colinge, D. Flandre, R. Gillon, J. P. Raskin, and D. Vanhoenacker, *J. Electrochem. Soc.*, **144**, 2437 (1997).
16. J. Kedzierski, D. Boyd, C. Cabral, Jr., P. Ronsheim, S. Zafar, P. M. Kozlowski, J. A. Ott, and M. Ieong, *IEEE Trans. Electron Devices*, **52**, 39 (2005).
17. A. E. J. Lim, R. T. P. Lee, C. H. Tung, S. Tripathy, D. L. Kwong, and Y. C. Yeo, *J. Electrochem. Soc.*, **153**, G337 (2006).
18. M. Qin, V. M. C. Poon, and S. C. H. Ho, *J. Electrochem. Soc.*, **148**, G271 (2001).
19. P. Y. Kuo, T. S. Chao, R. J. Wang, and T. F. Lei, *IEEE Electron Device Lett.*, **27**, 258 (2006).
20. H. C. Wen, J. H. Sim, J. P. Lu, and D. L. Kwong, *Electrochem. Solid-State Lett.*, **7**, G258 (2004).
21. C. W. Lin, M. Z. Yang, C. C. Yeh, L. J. Cheng, T. Y. Huang, H. C. Cheng, H. C. Lin, T. S. Chao, and C. Y. Chang, *Tech. Dig. - Int. Electron Devices Meet.*, **1999**, 305.
22. H. C. You, P. Y. Kuo, F. H. Ko, T. S. Chao, and T. F. Lei, *IEEE Electron Device Lett.*, **27**, 799 (2006).
23. L. C. Hecht, *J. Vac. Sci. Technol.*, **16**, 328 (1979).
24. P. Y. Kuo, T. S. Chao, and T. F. Lei, *IEEE Electron Device Lett.*, **25**, 634 (2004).
25. Y. Zhang, J. Wan, K. L. Wang, and B. Y. Nguyen, *IEEE Electron Device Lett.*, **23**, 419 (2002).
26. S. Yamada, S. Yokoyama, and M. Koyanagi, *Tech. Dig. - Int. Electron Devices Meet.*, **1990**, 859.
27. M. Yoshimi, M. Takahashi, T. Wada, K. Kato, S. Kambayashi, M. Kemmochi, and K. Natori, *IEEE Trans. Electron Devices*, **37**, 2015 (1990).
28. A. G. Lewis, T. Y. Huang, R. H. Bruce, M. Koyanagi, A. Chiang, and I. W. Wu, *Tech. Dig. - Int. Electron Devices Meet.*, **1988**, 264.
29. K. P. Anish Kumar, J. K. O. Sin, C. T. Nguyen, and P. K. Ko, *IEEE Trans. Electron Devices*, **45**, 2514 (1998).
30. J. Chen, F. Assaderaghi, P. K. Ko, and C. Hu, *IEEE Electron Device Lett.*, **13**, 572 (1992).
31. M. Chan, B. Yu, Z. J. Ma, C. T. Nguyen, C. Hu, and P. K. Ko, *IEEE Trans. Electron Devices*, **42**, 1975 (1995).
32. H. F. Wei, J. E. Chung, N. M. Kalkhoran, and F. Namavar, *IEEE Trans. Electron Devices*, **42**, 2096 (1995).
33. Y. Jiang, T. Y. Liow, N. Singh, L. H. Tan, G. Q. Lo, D. Chan, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **2008**, 869.