Journal of The Electrochemical Society, **157** (2) H137-H143 (2010)
0013-4651/2009/157(2)/H137/7/$28.00 © The Electrochemical Society

Improvement of the Thermal Stability of NiSi by Germanium Ion Implantation

Bing-Yue Tsui,[a,z] Chih-Ming Hsieh,[a] Yu-Ren Hung,[a] York Yang,[b] Ryan Shen,[b] Sam Cheng,[b] and Tony Lin[b]

[a]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan*
[b]*Advanced Ion Beam Technology Company, Hsinchu 300 Taiwan*

The thermal stability of nickel monosilicide (NiSi) is one of the important research topics in the area of nano-complementary metal oxide semiconductor. This paper reports the effect of germanium (Ge) ion implantation on the thermal stability of the NiSi/Si structure. High dose Ge ion implantation ($> 5 \times 10^{15}$ cm^{-2}) can improve the thermal stability of the NiSi/Si structure. Ge ion implantation before NiSi formation results in a very smooth NiSi/Si interface due to Ge atom pileup at the NiSi/Si interface. This high concentration Ge layer reduces the interface energy so that the thermal stability can be improved. Both the phase-transformation temperature and agglomeration temperature are improved by 50–100°C. The effects of Ge ion implantation on the NiSi-contacted n^+-p and p^+-n shallow junctions are also examined. Although fast Ni diffusion via the ion implantation induced defects is observed, better thermal stability can still be observed on the n^+-p junction.
© 2009 The Electrochemical Society. [DOI: 10.1149/1.3261852] All rights reserved.

Manuscript submitted June 15, 2009; revised manuscript received September 28, 2009. Published December 7, 2009.

Metal silicides have been used in the Si microelectronics industry for more than 20 years for reducing parasitic resistance and signal propagation delay time.[1-6] Nickel monosilicide (NiSi) is now the desirable contact material because of less Si consumption and low formation temperature.[7-10] The main issue of NiSi is its poor thermal stability, including thin-film agglomeration and high resistivity phase ($NiSi_2$) transformation. Some models based on surface/interface energies, grain boundary grooving, and silicide grain size have been proposed.[11-13] Because the NiSi phase is not in equilibrium with Si at high temperature, the expected reaction of NiSi + Si $\rightarrow$ $NiSi_2$ occurs. Similar to the thin-film agglomeration, the phase transformation is a nucleation-controlled reaction and depends on silicide thickness, dopant impurities, and annealing ramp rate.

Several methods have been proposed to improve the thermal stability of NiSi film on Si substrate; for example, fluorine ion implantation,[14,15] nitrogen ion implantation,[16,17] capping layers,[18,19] palladium (Pd)[20] incorporation, and platinum (Pt)[21-24] incorporation. Among these methods, Pt-incorporated Ni silicide produces the most promising results. One of the drawbacks of the Pt-incorporation method is the higher resistivity due to Pt doping. Recently, carbon incorporation has been reported to improve the thermal stability of NiSi,[25-27] however, the solid-state solubility of C in Si is very low and improper thermal budget after carbon incorporation would produce a large amount of interstitial carbon and result in junction leakage. Because the linewidth and thickness of NiSi scale down continuously, a new technique to improve its thermal stability is required.

In the 1980s, Ge ion implantation was reported as a substrate amorphization technique to eliminate dopant channeling effect.[28-30] Several investigations regarding the effects of the Ge preamorphization implantation (PAI) process on metal-silicide formation have been reported.[31-34] Most of these papers focused on the Ti silicides and Co silicides. High dose Ge PAI can improve the thermal stability of $TiSi_2$, while low dose ($\leqslant 1 \times 10^{15}$ cm^{-2}) Ge PAI does not play any role.[33] The incorporation of Ge results in an increase in the nucleation temperature of $CoSi_2$ from about 600°C to about 800°C.[34] The studies of the effects of Ge incorporation on Ni silicides were recently reported.[25,35-39] Kittl et al. found that the Ge PAI can increase the Ni_2Si growth rate at 250°C.[35] Surdeanu et al. reported that a shallow junction and a good short channel effect on metal-oxide-semiconductor field-effect transistors (MOSFETs) can be obtained with Ge PAI.[36] Both of them did not address thermal stability and shallow junction characteristics. Yun et al. observed that Ge PAI to a dose of 1×10^{14} cm^{-2} results in a smooth NiSi/Si interface and suppresses oxidation on arsenic-doped n^+ Si.[37] However, medium dose Ge PAI did not affect the thermal stability of NiSi. The retardation of the phase transformation from NiSi to $NiSi_2$ was found on the Si_xGe_{1-x} structure, but the NiSi agglomeration and the Ge out-diffusion on Si_xGe_{1-x} substrate are worse than those on Si substrate.[25,38] Kim et al. reported that a thin Si capping layer on $Si_{0.81}Ge_{0.19}$ substrate can improve the NiSi(Ge) agglomeration temperature due to the strain effect.[39] Accurate phase identification was not performed and p-n junction characteristics were not analyzed in their works.

According to the above reports, Ge incorporation to a suitable concentration may benefit the thermal stability of NiSi films, but the effect of Ge incorporation on the NiSi-contacted shallow junction has not been investigated. Moreover, Ge incorporation by high dose ion implantation has not been employed. Recently, the thermal stability improvement of the NiSi/poly-Si polycide structure by Ge ion implantation was reported.[40] It is thus expected that a similar technique can be applied to the NiSi/Si structure. In this work, a thorough study on the thermal stability improvement of the NiSi/Si structure by Ge ion implantation has been carried out. The effects of Ge ion implantation on the electrical characteristics of shallow n^+-p and p^+-n junctions are also examined.

Experimental

Samples were divided into two categories: blanket samples and p-n junction samples. The starting materials were boron-doped (for blanket samples and n^+-p junction samples) and phosphorus-doped (for p^+-n junction samples) 6 in. Si wafers with resistivities of 15–25 and 2–4 Ω cm, respectively. After initial clean, a 20 nm thick screen oxide was thermally grown on blanket samples. Some of the blanket samples were implanted by Ge ions at 20 or 50 keV to a dose of 5×10^{15} or 1×10^{16} cm^{-2}. These samples were classified as the Ge implantation before silicidation (GIBS) samples. The projected ranges (R_p) of Ge implantation at 20 and 50 keV were about 5 and 25 nm, respectively, below the Si surface as simulated by the Monte Carlo method. For the 20 keV samples, the Ge implanted layer would be fully consumed during silicide formation. After removal of the oxide screen layer, a 25 nm thick Ni film was deposited on all of the blanket samples by a high vacuum physical vapor deposition system. A two-step silicidation process was employed to form the NiSi film.[41] The first annealing step was fixed at 300°C for 60 min in vacuum. The GIBS samples were then cut into small pieces and received rapid thermal annealing (RTA) in N_2 ambient at different temperatures for 10 or 30 s. The Ge implantation after silication (GIAS) samples received a second annealing at 600°C for

[z] E-mail: bytsui@mail.nctu.edu.tw

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Table I. Process split conditions of the blanket samples.

Category	Energy (keV)	Dose (cm^{-2})	Annealing temperature (°C)	Annealing time (s)
GIBS	50, 20	5×10^{15}	500–850	10, 30, 60
GIAS	40	1×10^{16}		

30 s followed by Ge ion implantation at 40 keV to a dose of 5×10^{15} or 1×10^{16} cm^{-2}. The R_p was about 17 nm below the NiSi surface, and all of the Ge ions were located in the NiSi layer. The GIAS samples were then cut into small pieces and received RTA in N_2 ambient at different temperatures for different times. Samples without Ge ion implantation were also prepared as control samples. The control samples also received the two-step annealing with the first step at 300°C for 60 min and the second step at temperatures higher than 500°C for 10 or 30 s. Table I lists the process conditions of the blanket GIAS and GIBS samples.

Typical local-oxidation-of-Si isolation was employed to fabricate the p-n junction samples. Only the GIBS method was used to fabricate the p-n junction samples because this method results in better thermal stability than the GIAS method. The Ge dose was 1×10^{16} cm^{-2}. There was no screen oxide before Ge ion implantation, so the implantation energy was reduced to 30 keV to obtain an R_p of about 30 nm below the Si surface. This R_p value is similar to that of Ge implantation at 50 keV through a 20 nm thick screen oxide. To form n^+-p and p^+-n junctions. As and BF_2 ions were implanted at 35 and 20 keV, respectively, to a dose of 5×10^{15} cm^{-2}. A spike annealing at 1025°C was performed to activate the dopants and annihilate the ion implantation induced defects. The silicidation process was identical to that used to fabricate the blanket samples. Table II lists the process conditions of the p-n junction samples.

Surface morphology was inspected by a scanning electron microscope (SEM). Cross-sectional microstructure was inspected by a transmission electron microscope (TEM). Interface roughness was analyzed by an atomic force microscope (AFM). Phases of Ni silicide were identified by X-ray diffraction (XRD). Depth profiles of species were analyzed by a secondary-ion-mass spectroscope (SIMS). The sheet resistance (R_s) of the silicide was measured by a four-point probe system. Current–voltage (I-V) characteristics of junctions were measured by a model Agilent 4156C semiconductor parameter analyzer.

Results and Discussion

Effects of Ge ion implantation on bulk Si.— Figure 1 shows the normalized sheet resistance values of the GIBS samples after annealing at different temperatures for 10 s. The sheet resistance values are normalized with that of the 500°C annealed samples. The samples with annealing temperature lower than 700°C have similar sheet resistance value of around 4–6 Ω/□. Either a higher energy or a higher dose of Ge ion implantation results in better thermal stability. The sheet resistance value of the sample with Ge ion implantation at 20 keV to a dose of 5×10^{15} cm^{-2} increases apparently after annealing at 750°C. By increasing the Ge dose to 1×10^{16} cm^{-2},

Table II. Process split conditions of the p-n junction samples.

Category	Implanted species and energy	Dose (cm^{-2})	Annealing temperature (°C)
p^+-n	Ge 30 keV	Ge 1×10^{16}	500–700
	BF_2 20 keV	BF_2 5×10^{15}	
n^+-p	Ge 30 keV	Ge 1×10^{16}	
	BF_2 20 keV	As 5×10^{15}	

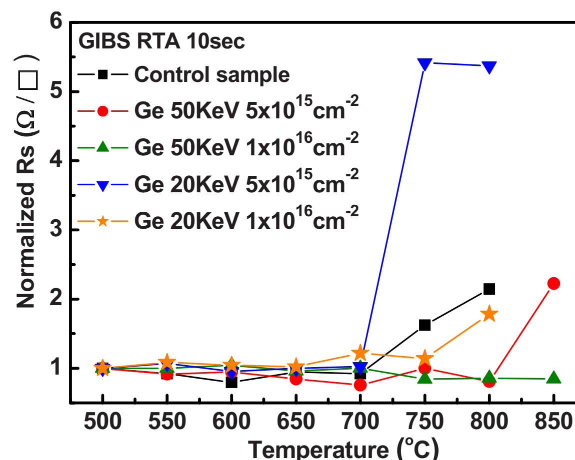


Figure 1. (Color online) Normalized sheet resistance values (R_s) of the GIBS samples after annealing at different temperatures for 10 s. The sheet resistance values are normalized to those of the 500°C annealed samples.

the sustainable temperature can be increased to 750°C. The samples with Ge ion implantation at 50 keV to a dose of 5×10^{15} cm^{-2} exhibit similar thermal stability of 750°C in terms of the sheet resistance value. By increasing the dose to 1×10^{16} cm^{-2}, the sheet resistance value does not degrade even after annealing at 850°C for 10 s. The GIAS samples exhibit the same trend, i.e., higher Ge I/I dose results in better thermal stability. As shown in Fig. 2, when the dose increases from 5×10^{15} to 1×10^{16} cm^{-2}, the sustainable temperature increases from 750 to 800°C. Note that the GIBS samples have better thermal stability than the GIAS samples. These observations imply that Ge ion implantation can improve the thermal stability of the NiSi/Si structure. The mechanism is discussed later.

As the annealing time is increased to 30 s, the GIBS samples still show better thermal stability than the GIAS samples, as shown in Fig. 3. It is also observed that the sustainable temperature degrades upon increasing the annealing time. For example, the sustainable temperature of the GIBS sample with Ge ion implantation at 50 keV to a dose of 1×10^{16} cm^{-2} decreases from 850 to 800°C upon increasing the annealing time from 10 to 30 s. A similar 50°C reduction in the sustainable temperature is observed on the GIAS

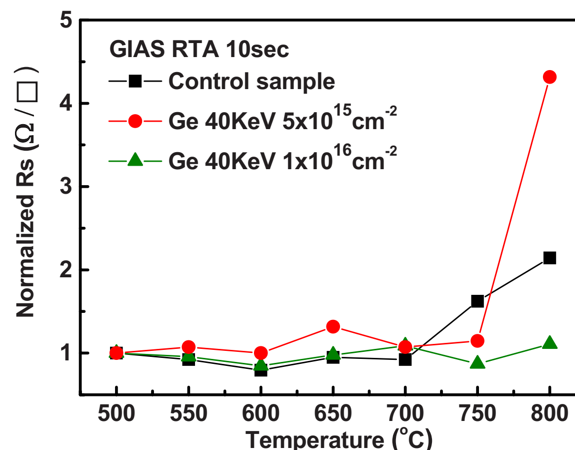


Figure 2. (Color online) Normalized sheet resistance values (R_s) of the GIAS samples after annealing at different temperatures for 10 s. The sheet resistance values are normalized to those of the 500°C annealed samples.

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

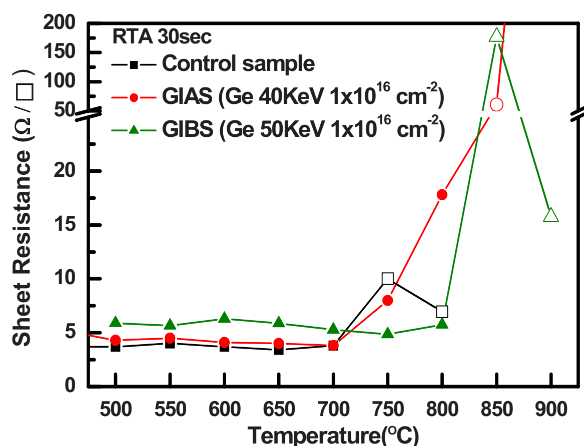


Figure 3. (Color online) Normalized sheet resistance values (R_s) of the GIBS and GIAS samples with Ge ion implantation at 40 and 50 keV, respectively, to a dose of 1×10^{16} cm^{-2}. The annealing time is 30 s. The sheet resistance values are normalized to those of the 500°C annealed samples. Solid symbols represent the NiSi phase and empty symbols represent the $NiSi_2$ phase identified by XRD.

samples. The NiSi phase transforms to the $NiSi_2$ phase at 850°C. The thickness of $NiSi_2$ is almost twice that of the NiSi film so that the sheet resistance decreases.[42]

Two mechanisms are expected to increase the sheet resistance value of the Ni-silicide film. When the agglomeration of silicide film occurs, the silicide film breaks at first and then becomes discontinuous. In this case, the sheet resistance value increases apparently. The silicide phase may transform from NiSi to $NiSi_2$ at high temperature. Although the resistivity of $NiSi_2$ is higher than that of NiSi, the thickness is also increased so that the increase in sheet resistance value is moderate. Therefore, the actual mechanisms of the sheet resistance behavior observed in Fig. 1-3 were clarified by SEM inspection and XRD analysis.

Figure 4 shows the surface morphology of the sample without Ge ion implantation (control sample) and the GIBS samples with Ge ion implantation at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at different temperatures for 30 s. The 750°C annealed GIBS sample still exhibits a very smooth surface. Agglomeration phenomenon is observed on the 800°C annealed GIBS sample. The control sample agglomerates at 700°C. It is clear that Ge ion implantation can

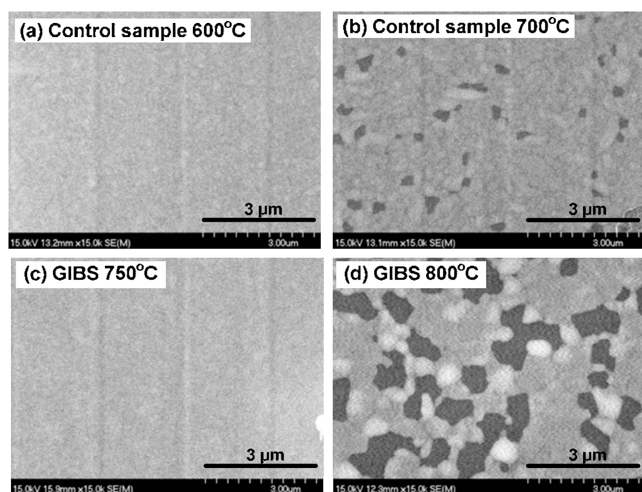


Figure 4. Surface morphology inspected by SEM of the control sample without Ge I/I and the GIBS samples with Ge I/I at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at different temperatures for 30 s.

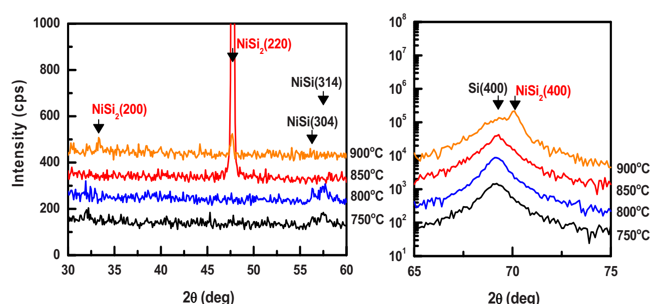


Figure 5. (Color online) XRD spectra of the GIBS samples with Ge ion implantation at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at different temperatures for 30 s.

effectively suppress agglomeration. Figure 5 shows the XRD spectra of the GIBS samples with Ge ion implantation at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at different temperatures for 30 s. The NiSi phase remains stable up to 800°C even if agglomeration has occurred at this temperature. The $NiSi_2$ phase is observed at 850°C. This result indicates that the Ge ion implantation can retard the phase transformation from NiSi to $NiSi_2$, and phase transformation occurs behind agglomeration on the samples with a high dose of Ge ion implantation.

Another advantage of Ge ion implantation on the NiSi/Si structure is the smooth NiSi/Si interface. Figure 6 shows the cross-sectional TEM micrograph of the GIBS sample with Ge I/I at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at 750°C for 30 s. The NiSi/Si interface is quite smooth, which is consistent with the high agglomeration temperature. The thickness of the NiSi film is 45 nm, which translates to a resistivity of 21 μΩ cm. This value is slightly higher than the bulk value but is much lower than the resistivity of $NiSi_xGe_{1-x}$ and Ni(Pt)Si. Figure 7 shows the SIMS depth profile of Ge in GIBS samples with Ge I/I at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at 600°C for 30 s. A large amount of Ge atoms pile up at the NiSi/Si interface. It is suspected that the improved thermal stability and smooth interface are correlated to the high concentration of Ge atoms at the interface.

Table III summarizes the agglomeration temperature and the phase-transformation temperature of the controlled samples, GIBS samples, and GIAS samples with RTA for 30 s. The agglomeration temperatures are determined by SEM inspection and the phase-transformation temperatures are determined by XRD analysis. In the initial stage of agglomeration, the film breaks but is still continuous so that the sheet resistance does not increase obviously. Therefore, the agglomeration temperature determined by the SEM inspection is lower than that determined by the sheet resistance measurement.

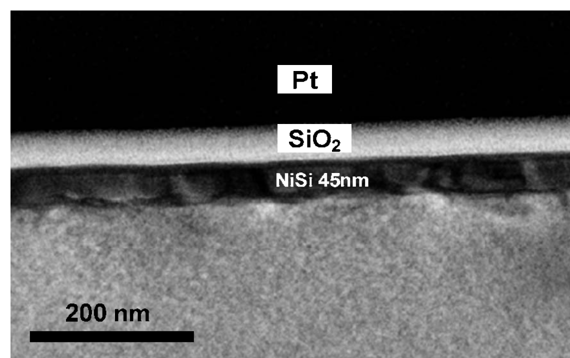


Figure 6. Cross-sectional TEM micrograph of the GIBS sample with Ge ion implantation at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at 750°C for 30 s.

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

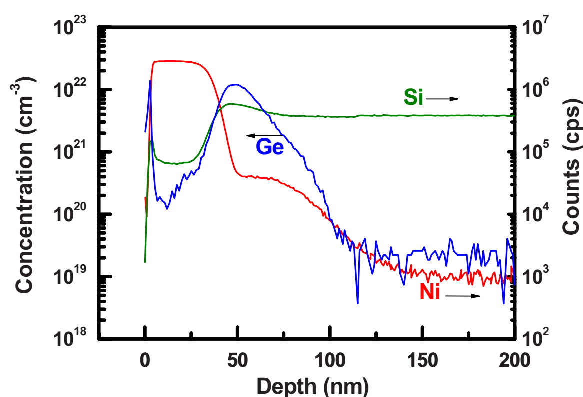
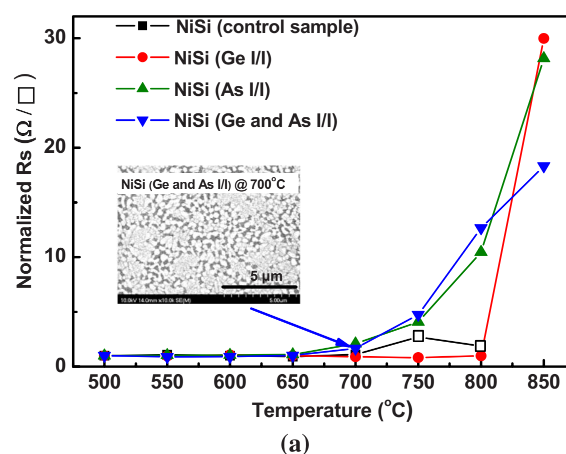


Figure 7. (Color online) SIMS depth profile of Ge atoms of the GIBS samples with Ge I/I at 50 keV to a dose of 1×10^{16} cm^{-2} after annealing at 600°C for 30 s. The depth is measured from the top surface of the NiSi film.



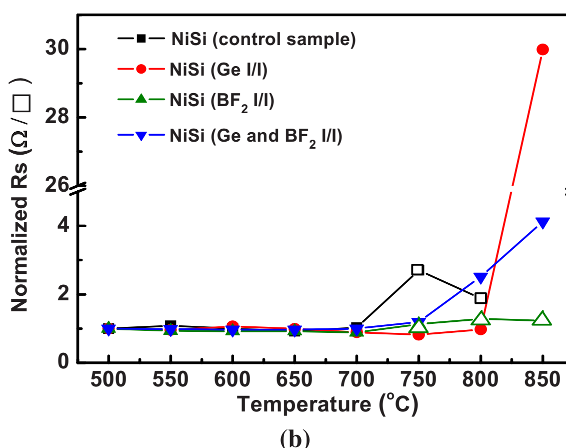


Figure 8. (Color online) Normalized sheet resistance values of the Ni-silicide films on (a) n^+ and (b) p^+ Si layer after annealing at different temperatures for 30 s. The sheet resistance values are normalized to those of the 500°C annealed samples. The inset in (a) indicates that the NiSi film on the Ge implanted n^+-p junction has agglomerated after annealing at 750°C. Solid symbols represent the NiSi phase and empty symbols represent the $NiSi_2$ phase identified by XRD.

The mechanisms of improving agglomeration temperature are discussed in the following. It has been reported that the ion implantation before the silicidation process has two main effects on silicide formation: one is preamorphization of the substrate and the other is the change of surface/interface energy.[11] The Ge ion implantation produces a uniform amorphous layer because ion implantation is a uniform process. The low temperature first step annealing process makes Ni uniformly react with the amorphous Si layer. The NiSi growth rate on an amorphous Si region is higher than that on a crystalline Si region. Once the NiSi front edge reaches the amorphous/crystalline interface, the growth rate is retarded. Therefore, a smooth NiSi/Si interface is obtained. A high concentration of Ge also retards the Ni-silicide growth rate.[43] As Ni silicide grows, Ge atoms are repelled out of the silicide layer and pile up at the silicide/Si interface. The Ge concentration can autoadjust the Ni-silicide growth rate to produce a smooth interface. The piled-up Ge atoms change the NiSi/Si interface energy so that the NiSi agglomeration at high temperature is suppressed. The GIBS samples have better thermal stability than the GIAS samples because the GIBS process incorporates more Ge to the NiSi/Si interface. Similar results can be observed on various silicide/Si structures by F^+ or N_2^+ implantation.[14-17] Higher ion implantation energy and dose result in higher Ge concentration at the NiSi/Si interface, which implies that the sustainable temperature is higher. This is confirmed by our results.

From the classical nucleation theory, the improvement of thermal stability can be explained by the change in mixing entropy which raises the activation energy barrier for nucleation. The formation energy of Ni_2Si (−142.7 kJ/mol) is more negative than that of Ni_2Ge (−37 kJ/mol), and the Ge atoms were segregated to the NiSi grain boundaries during silicide formation.[44] The piled up and segregated Ge atoms act as a barrier to suppress Ni diffusion along grain boundaries. It implies less driving force for silicide islands grooving, which in turn prevents agglomeration. The high resistance to agglomeration is also attributed to the retardation of $NiSi_2$ grain growth. $NiSi_2$ formation was assumed as a nucleation-controlled reaction and ΔG is the Gibbs free energy of the reaction: NiSi + Si → $NiSi_2$. Because the piled up and segregated Ge atoms can retard the reaction, the absolute value of a new ΔG^* decreases and raises the activation free energy for nucleation. Hence, as the agglomeration is suppressed, the phase transformation from NiSi to $NiSi_2$ is also suppressed. Similar results have been reported on the Pt-incorporated NiSi film.[19,21]

The high sheet resistance of the sample with a Ge I/I dose of 5×10^{15} cm^{-2} at 800°C shown in Fig. 3 can be explained now. Although the silicide film of the control sample agglomerates at 700°C as shown in Fig. 4b, its phase transforms from NiSi to $NiSi_2$ at 750°C. The phase transformation increases the film thickness and reduces the silicide/Si interface energy so that the sheet resistance increase is not as severe as that of the samples with a Ge dose of 5×10^{15} cm^{-2}.

Effects of Ge ion implantation on n^+-p and p^+-n junction.— Figure 8a and b shows the normalized sheet resistance value as a function of annealing temperature of the NiSi-contacted n^+-p and p^+-n junctions, respectively. The annealing time is 30 s. The improvement in thermal stability by Ge ion implantation presented in the previous subsection is almost eliminated on the n^+-p junction

Table III. Summary of the thin-film agglomeration temperatures and phase-transformation temperatures of the blanket control samples, GIBS samples, and GIAS samples.

Sample type	Control sample	GIAS	GIBS
Energy (keV)	—	40	50
Dose (cm^{-2})	—	5×10^{15} 1×10^{16}	5×10^{15} 1×10^{16}
Agglomeration temperature	700°C	700°C	800°C
Phase-transformation temperature	750°C	850°C	850°C

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

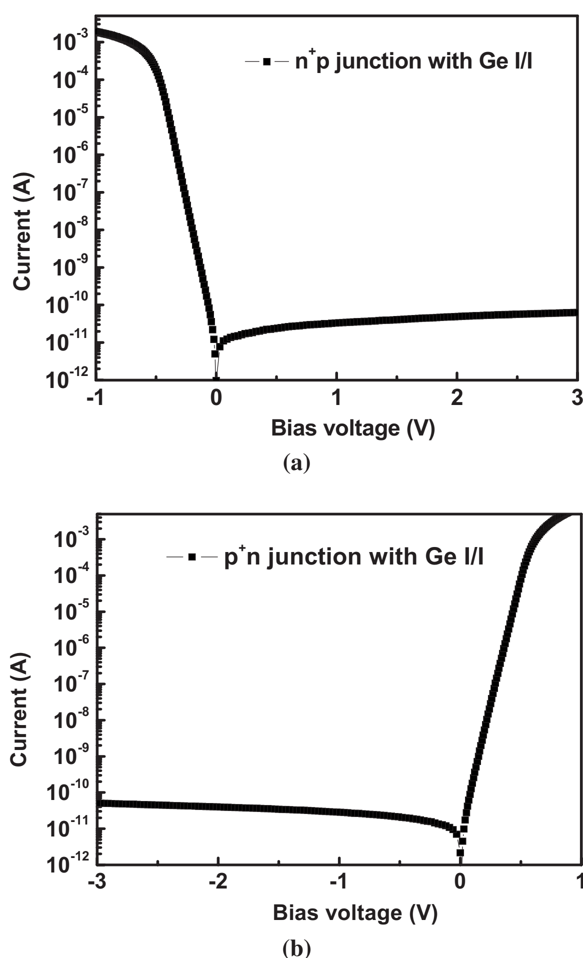


Figure 9. Typical *I-V* characteristics of the (a) n^+-p and (b) p^+-n junctions with Ge ion implantation at 30 keV to a dose of 1×10^{16} cm^{-2} after 600°C annealing for 30 s.

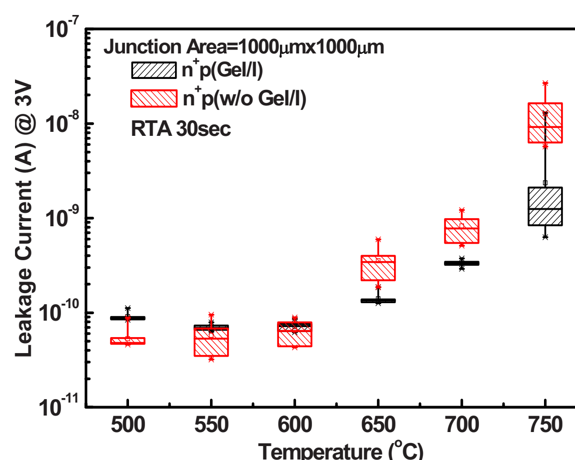


Figure 10. (Color online) Statistics of the reverse leakage current of the n^+-p junctions with and without Ge ion implantation after annealing at different temperatures for 30 s.

samples. Agglomeration phenomenon occurs after annealing at 700°C as shown in the inset of Fig. 8a. However, the XRD analysis indicates that the phase transformation from NiSi to $NiSi_2$ does not occur even at 850°C. It has been proposed that the existence of arsenic atoms at the interface between NiSi film and Si substrate may change the interface energy and then make the agglomeration easily occur in the NiSi films on n^+ Si substrate compared to that in NiSi films on the other substrates.[45] The segregated Ge atoms at the NiSi grain boundaries still suppress the phase transformation from NiSi to $NiSi_2$. On the p^+-n junction samples, the agglomeration temperature can be raised by either F or Ge incorporation.[14,15,40] The phase transformation of the sample without Ge I/I occurs at 750°C (XRD data not shown), which is consistent with the published data.[14] These results indicate that Ge incorporation is better than F incorporation in terms of raising the phase-transformation temperature. The NiSi thickness of the n^+-p junctions with Ge ion implantation after annealing at 600°C for 30 s is about 36 nm, which is slightly thinner than that of the blanket sample due to process deviation. The resistivity of the 500°C annealed n^+-p junction with Ge I/I is 19.8 μΩ cm. To quantify the interface roughness, the NiSi film was removed and the Si surface was scanned by AFM. With Ge I/I, the roughness decreases from 1.50 to 0.85 nm and from 2.23 to 1.61 nm on n^+ and p^+ Si, respectively.

Figure 9a and b shows the typical *I-V* characteristics of the n^+-p and p^+-n junctions with Ge ion implantation after 600°C annealing for 30 s. The forward biased current has an ideality factor of around 1.1 on the n^+-p junctions. This low value implies that most of the ion implantation induced defects near the metallurgic junction have been annihilated. The ideality factors of the p^+-n junctions with or without Ge I/I are all close to 1.2. Therefore, the slightly higher value of the p^+-n junctions compared with that of the n^+-p junctions might be attributed to the quality of the original Si substrates.

Figure 10 shows the reverse-biased junction leakage current statistics of the n^+-p junctions after annealing at different temperatures for 30 s. The p-substrate was grounded and +3 V was applied on the NiSi film. The leakage current remains low as the annealing temperature is lower than 600°C and increases as the annealing temperature increases to 650°C. The leakage current of the junctions without Ge implantation is slightly lower than that of the junctions with Ge ion implantation as the annealing temperature is 500°C. As the annealing temperature increases to higher than 650°C, the junctions with Ge ion implantation exhibit a lower leakage current in comparison with the junctions without Ge ion implantation. Figure 11a and b shows the SIMS depth profiles of the 600°C annealed junctions with and without Ge ion implantation, respectively. The metallurgic n^+-p junction depth is 90 nm beneath the NiSi/Si interface. The depth profile of Ni shows a tail toward the metallurgic junction in Si owing to the Ni dissolution and diffusion along the ion implantation induced defects during silicide formation. The tail in the Ge implanted sample is more apparent than that in the sample without Ge ion implantation due to extra defects generated by Ge ion implantation. The dissolved Ni explains the slightly higher leakage current of the Ge implanted junction after annealing at temperatures lower than and equal to 600°C. Because the phase transformation does not occur up to 850°C, the increase in leakage current with the increase in annealing temperature at temperatures higher than 650°C is obviously affected by the agglomeration of NiSi film.

The statistics of the reverse-biased junction leakage current of the p^+-n junctions after annealing at different temperatures for 30 s is shown in Fig. 12. The leakage current of junctions with and without Ge ion implantation slightly increases as the annealing temperature increases from 500 to 750°C. SIMS analysis, shown in Fig. 13, reveals that the metallurgic junction depth is 120 nm beneath the NiSi/Si interface. The deeper junction and better thermal stability of NiSi on the p^+-n junction in comparison with those on the n^+-p junction explain the better integrity of leakage current. F incorporation could also improve the thermal stability of silicide; therefore, the thermal stability of leakage current from the junctions without Ge ion implantation is similar to that with Ge ion implantation. The phase transformation from NiSi to $NiSi_2$ after 750°C annealing of the junctions with Ge ion implantation retards agglomeration. Because the p^+-n junction depth is not very shallow, phase transformation does not degrade the leakage current performance. According to

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

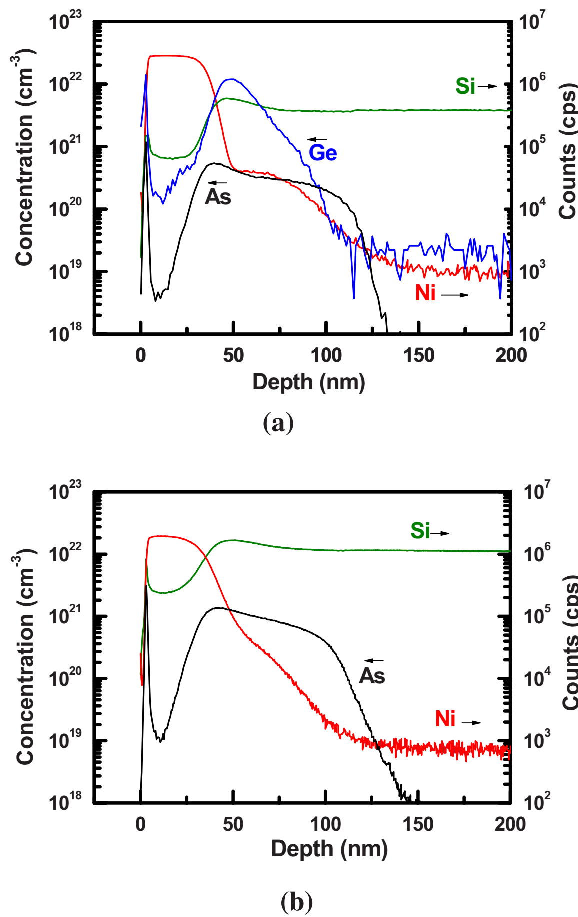


Figure 11. (Color online) SIMS depth profile of the 600°C annealed n^+-p junctions (a) with and (b) without Ge ion implantation. The depth is measured from the top surface of the NiSi film.

the sheet resistance data in Fig. 8b, the NiSi on the Ge ion implanted sample agglomerates at 800°C. Therefore, the junction leakage current increases apparently at 800°C.

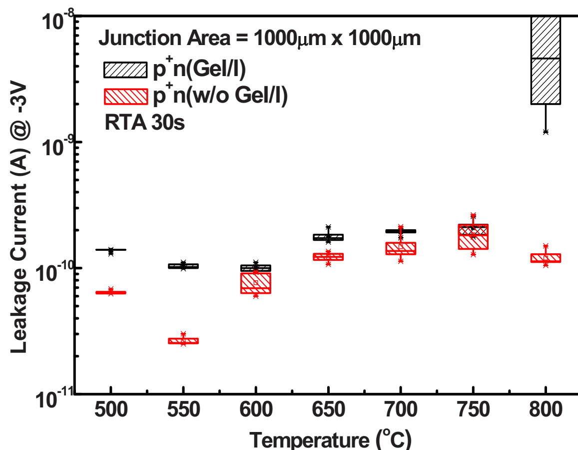


Figure 12. (Color online) Statistics of the reverse leakage current of the p^+-n junctions with and without Ge ion implantation after annealing at different temperatures for 30 s.

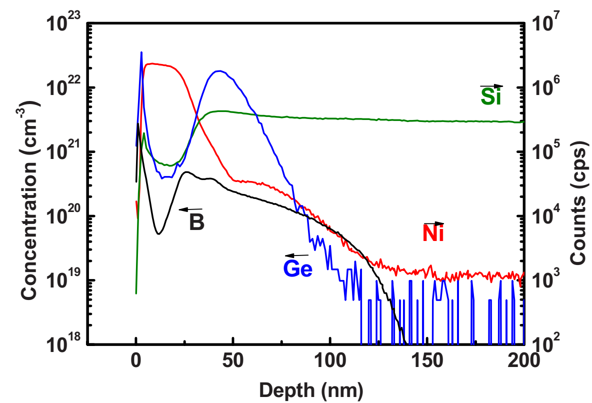


Figure 13. (Color online) SIMS depth profile of the 600°C annealed p^+-n junctions with Ge ion implantation. The depth is measured from the top surface of the NiSi film.

Conclusion

The effect of Ge ion implantation on the thermal stability of the NiSi/Si structure is studied thoroughly. The GIBS process results in a very smooth NiSi/Si interface. The sustainable process temperature of the NiSi/Si structure, considering thin-film agglomeration and phase transformation, can be improved by 50–100°C with high dosage Ge ion implantation at suitable energy. The GIAS process exhibits a similar effect, but the performance is not as good as the GIBS process. These observations are explained by the change in surface energy due to Ge atom pileup at the NiSi/Si interface. Because only a few Ge atoms remain in the NiSi layer, the resistivity of the NiSi film is close to the bulk value.

Applying the GIBS method to n^+-p and p^+-n junctions, although the phase-transformation temperature is raised, the agglomeration temperature of NiSi on n^+-p junction did not improve due to the high concentration of As atoms that induced cluster defects. Electrical measurements indicate that the Ge ion implanted junctions exhibit a slightly higher but acceptable leakage current after medium temperature annealing. This observation is explained by the Ni diffusion and dissolution enhancement due to the Ge ion implantation induced extra defects. If these defects can be annihilated by suitable thermal annealing techniques such as laser annealing, the smooth NiSi/Si interface would have more benefit to ultrashallow junctions. All of these observations suggest the promising nature of Ge ion implantation technique. The highest sustainable process temperature of the thinner NiSi may be lower than that observed in this work. However, the mechanisms identified in this work for the thermal stability improvement could be applied.

Acknowledgment

The authors thank the National Nano Device Laboratory of NARL and the Nano Facility Center of National Chiao-Tung University for supporting the process environment in sample preparation. This work was supported by the National Science Council, Taiwan under contract no. NSC-95-2221-E-009-302-MY3.

National Chiao Tung University assisted in meeting the publication costs of this article.

References

1. K. N. Tu and J. W. Mayer, *Thin Films-Interdiffusion and Reactions*, Chap. 10, John Wiley & Sons, New York (1978).
2. M. A. Nicolet and S. S. Lau, *VLSI Electronics: Microstructure Science*, Vol. 6, Chap. 6, Academic, New York (1983).
3. S. P. Murarka, *Silicides for VLSI Applications*, Academic, New York (1983).
4. G. Ottaviani, K. N. Tu, and J. W. Mayer, *Phys. Rev. B*, **24**, 3354 (1981).
5. T. G. Finstad and M. A. Nicolet, *J. Appl. Phys.*, **50**, 303 (1979).
6. K. Maex, *Mater. Sci. Eng. R.*, **11**, 53 (1993).
7. H. Iwai, T. Ohguro, and S. I. Ohmi, *Microelectron. Eng.*, **60**, 157 (2002).
8. T. Morimoto, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, H. Okano, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, et al., *Tech. Dig. - Int. Electron*

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

Devices Meet., **1991**, 653.

9. Y. Tsuchiya, A. Tobioka, O. Nakatsuka, H. Ikeda, A. Sakai, S. Zaima, and Y. Yasuda, *Jpn. J. Appl. Phys., Part 1*, **41**, 2450 (2002).
10. E. G. Colgan, J. P. Gambino, and Q. Z. Hong, *Mater. Sci. Eng. R.*, **16**, 43 (1996).
11. P. Revesz, L. R. Zheng, L. S. Hung, and J. W. Mayer, *Appl. Phys. Lett.*, **48**, 1591 (1986).
12. T. P. Nolan, R. Sinclair, and R. Beyers, *J. Appl. Phys.*, **71**, 720 (1992).
13. H. Jeon, C. A. Sukow, J. W. Honeycutt, G. A. Rozgonyi, and R. J. Nemanich, *J. Appl. Phys.*, **71**, 4269 (1992).
14. A. S. W. Wong, D. Z. Chi, M. Loomans, D. Ma, M. Y. Lai, W. C. Tjiu, S. J. Chua, C. W. Lim, and J. E. Greene, *Appl. Phys. Lett.*, **81**, 5138 (2002).
15. K. Kashihara, T. Yamaguchi, T. Okudaira, T. Tsutsumi, K. Maekawa, K. Asai, and M. Yoneda, in *Proceedings of The 6th International Workshop on Junction Technology*, p. 176 (2006).
16. T. Ohguro, S. Nakamura, E. Morifuji, M. Ono, T. Yoshitomi, M. Saito, H. S. Momose, and H. Iwai, *Tech. Dig. - Int. Electron Devices Meet.*, **1995**, 453.
17. L. W. Cheng, J. Y. Chen, J. C. Chen, S. L. Cheng, L. J. Chen, and B. Y. Tsui, in *Proceedings of International Conference on Ion Implantation Technology*, Vol. 2, p. 1002 (1998).
18. T. Ohguro, T. Morimoto, Y. Ushiku, and H. Iwai, *Proceedings of International Conference on Solid State Device and Materials*, p. 192 (1993).
19. T. H. Hou, T. F. Lei, and T. S. Chao, *IEEE Electron Device Lett.*, **20**, 572 (1999).
20. Y. J. Kim, S. Y. Oh, J. G. Yun, W. J. Lee, Y. Y. Zhang, Z. Zhong, S. Y. Jung, and H. H. Ji, *IEEE Trans. Nanotechnol.*, **6**, 431 (2007).
21. D. Mangelinck, J. Y. Dai, J. S. Pan, and S. K. Lahiri, *Appl. Phys. Lett.*, **75**, 1736 (1999).
22. D. Z. Chi, D. Mangelinck, S. K. Lahiri, P. S. Lee, and K. L. Pey, *Appl. Phys. Lett.*, **78**, 3256 (2001).
23. P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi, and L. Chan, *IEEE Electron Device Lett.*, **22**, 568 (2001).
24. L. W. Cheng, S. L. Cheng, L. J. Chen, H. C. Chien, H. L. Lee, and F. M. Pan, *J. Vac. Sci. Technol. A*, **18**, 1176 (2000).
25. S. Zaima, O. Nakatsuka, A. Sakai, J. Murota, and Y. Yasuda, *Appl. Surf. Sci.*, **224**, 215 (2004).
26. R. T. P. Lee, L. T. Yang, T. Y. Liow, K. M. Tan, A. E. J. Lim, K. W. Ang, D. M. Y. Lai, K. M. Hoe, G. Q. Lo, G. S. Samudra, et al., *IEEE Electron Device Lett.*, **29**, 89 (2008).
27. S. Lombardo, A. Cacciato, K. K. Larsen, V. Raineri, F. L. Via, V. Privitera, and S. U. Campisano, *J. Appl. Phys.*, **79**, 3464 (1996).
28. A. C. Ajmera, G. A. Rozgonyi, and R. B. Fair, *Appl. Phys. Lett.*, **52**, 813 (1988).
29. M. C. Ozturk, J. J. Wortman, and R. B. Fair, *Appl. Phys. Lett.*, **52**, 963 (1988).
30. M. C. Ozturk, J. J. Wortman, C. M. Osbum, A. Ajmera, G. A. Rozgonyi, E. Frey, W. K. Chu, and C. Lee, *IEEE Trans. Electron Devices*, **35**, 659 (1988).
31. C. Dehm, J. Gyulai, and H. Ryssel, *Appl. Phys. Lett.*, **60**, 1214 (1992).
32. C. T. Huang, T. F. Lei, C. H. Chu, and S. H. Shvu, *IEEE Electron Device Lett.*, **17**, 88 (1996).
33. P. Liu, T. C. Hsiao, and J. C. S. Woo, *IEEE Trans. Electron Devices*, **45**, 1280 (1998).
34. C. Detavernier, R. L. Van Meirhaeghe, F. Cardon, and K. Maex, *Phys. Rev. B*, **62**, 12045 (2000).
35. J. A. Kittl, A. Lauwers, O. Chamirian, M. van Dal, A. Akheyar, M. De Potter, R. Lindsay, and K. Maex, *Microelectron. Eng.*, **70**, 158 (2003).
36. R. Surdeanu, B. J. Pawlak, R. Lindsay, M. van Dal, G. Doornbos, C. J. J. Dachs, Y. V. Ponomarev, J. J. P. Loo, F. N. Cubaynes, K. Henson, et al., *Jpn. J. Appl. Phys., Part 1*, **43**, 1778 (2004).
37. J. G. Yun, S. Y. Oh, H. H. Ji, B. F. Huang, Y. H. Park, J. S. Wang, S. H. Park, T. S. Bae, and H. D. Lee, *Jpn. J. Appl. Phys., Part 1*, **43**, 6998 (2004).
38. T. Jarmar, J. Seger, F. Ericson, andD. Mangelinck, *J. Appl. Phys.*, **92**, 7193 (2002).
39. J. Y. Kim, C. R. Kim, J. Lee, W. W. Park, J. Y. Leem, H. Ryu, W. J. Lee, Y. Y. Zhang, S. Y. Jung , andH. D. Lee, et al., *Jpn. J. Appl. Phys.*, **47**, 7771 (2008).
40. C. M. Hsieh, B. Y. Tsui, Y. R. Hung, Y. Yang, R. Shen, S. Cheng, and T. Lin, *Electrochem. Solid-State Lett.*, **12**, H226 (2009).
41. B. Y. Tsui and C. P. Lin, *IEEE Trans. Electron Devices*, **52**, 2455 (2005).
42. K. Tsutsui, R. Xiang, K. Nagahiro, T. Shiozawa, P. Ahmet, Y. Okuno, M. Matsumoto, M. Kubota, K. Kakushima, and H. Iwai, *Microelectron. Eng.*, **85**, 315 (2008).
43. T. Sadoh, H. Kanno, A. Kenjo, and M. Miyao, *Appl. Surf. Sci.*, **224**, 227 (2004).
44. Y. Tsuchiya, A. Kinoshita, and J. Koga, *IEEE Trans. Electron Devices*, **53**, 3080 (2006).
45. P. Ahmet, T. Shiozawa, K. Nagahiro, T. Nagata, K. Kakushima, K. Tsutsui, T. Chikyow, and H. Iwai, *Microelectron. Eng.*, **85**, 1642 (2008).

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).