三五族化合物半導體晶圓接合之基本研究及應用

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摘　　要

本論文可被區分為兩個主要的部分：一為三五族化合物半導體的接合介面之研究，另一個是化合物半導體晶圓接合在光電元件上的應用。在第一部份探討晶圓接合退火溫度對於砷化鎵接合介面的影響，接著討論接合介面變化與電性的關係。另外，也研究晶圓接合的旋轉角度差異和兩晶片表面角度的差異和電性變化的關係。第二部份是利用晶圓接合的方式轉移異質磊晶種子層成功的執行大晶格不匹配的異質磊晶成長。另一方面，媒介層亦被利用來降低晶圓接合製程溫度，最佳化晶圓接合製程於高亮度發光二極體上的應用。

矽摻雜 n-型(100)並留有原生氧化層的單砷化鎵試片和雙片砷化鎵接合試片在相同的溫度下進行退火(400-850℃)，有系統的觀察接合介面的原生氧化層與電性隨著溫度改變情形。實驗結果指出當晶圓接合溫度為 400℃時，砷化鎵晶片是靠著連續非晶質氧化層接合，將接合溫度升高超過 400℃以上，接合介面的氧化層分佈漸漸變為局部分佈最後消失，接合介面電阻隨溫度升高漸漸的降低，然而，若將溫度繼續升高到 850℃以上，介面氧化層會擴散到 n-型砷化鎵半導體中並發生了反轉效應(n 型轉為半絕緣)，使得其介面電阻急遽升高。在 p-型砷化鎵半導體在相同的溫度下進行接合，但是介面電阻隨著接合溫度升高而降低，結果證明了 n-型砷化鎵受高溫影響產生反轉效應。除此之外，接合角度差異與介面電阻也被研究，執行順相與返相(Anti- and In-phase)兩類的晶圓接合(700℃ 1 小時)，發現反相接合的介面非晶質區存在一薄薄(5nm 以下)的非晶質區，這造成順相接合的介面電阻確實比反相接合低。

磊晶層轉移是晶圓接合技術在光電元件應用上重要的一項，具有直線通道圖形的 50nm 磷化銦鎵磊晶層轉移到磷化鎵基板上當作磷化鋁銦鎵異質磊晶的種子層，磷化銦鎵磊晶轉移層轉移後幾乎沒有缺陷在轉移層中被觀察到，並且，光電性質無太劇烈改變，此外，發現 n-型磷化銦鎵/n-型磷化鎵異質晶圓接合的表面角度差異越大介面電阻就

越大的現象，藉由種子層將上述的四元合金成長在這具有線圖形的基板上，得到了低缺陷密度以及良好光電特性的異質磊晶結構。

晶圓直接接合技術常被用來製作高亮度發光二極體，晶圓接合常需要在高溫下執行，可能會造成發光二極體元件結構的衰退，除此之外，晶圓接合時常會兩晶片之間存在一些不可避免的相對旋轉角，在這實驗，這兩種問題將利用多晶的氧化銦錫薄膜做為媒介層於650℃以下接合磷化銦鎵/砷化鎵和砷化鎵晶片來解決，可發現接合的機制是由於磷化銦鎵上的銦流動到氧化銦錫薄膜上來發生，介面電阻也比起直接接合磷化銦鎵/砷化鎵和砷化鎵晶片來的低，並且隨溫度增加電阻會減少。這媒介層應用在晶圓接合的發光二極體中亦發現，這媒介層存在確實會降低直接晶圓接合元件中的起使電壓並增加操作電流。

Fundamental Studies and Applications of III-V Compound Semiconductor Wafer Bonding

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ABSTRACT

The main topics of this thesis can be divided into two categories: (1) The investigation of boned interfaces of III-V compound semiconductors; (2) Applications of III-V compound semiconductors wafer bonding to optoelectronic devices. In the first category, the effects of annealing temperature on the morphology and the change of electrical property of bonded interfaces were discussed. In addition, the effects of the rotational misalignments and relative surface misorientations between two wafers on electrical resistance of bonded wafers were also studied. In the second category, a seed layer was bonded and transferred to a large lattice mismatched substrate first. Then, the heteroepitaxy layer was grown on the large lattice mismatched substrate successfully by means of the seed layer. Furthermore, to optimum the wafer bonding process of high brightness LEDs (Light emitting diodes), an intermediate layer was used to decrease wafer bonding temperature.

Si doped n-type (100) GaAs wafers which have native oxide were used for systematically investigation of the bonded interface and the electrical characteristics. For estimating the electrical characteristics of bonded wafer, single GaAs wafers and two-layer

bonded stacks were annealed at the same temperature (400-850℃). Experimental results indicated that GaAs bond via an amorphous oxide layer at 400 °C. When temperatures increased above 400 °C, the oxide bonded area declined and finally disappeared. The electrical resistance of bonded interface decreased with the increase of bonded temperature. However, the resistance increased with temperatures exceeding 850 °C. This result caused by the oxygen in-diffusion into n-GaAs and the effect of inversion. P-type GaAs samples were also pressed against each other and annealed under identical thermal conditions. The electrical resistance of bonded interface decreased with the increase of bonded temperature, even the temperatures exceeds 850 °C. Results evidence that the event of inversion of n-GaAs wafers were occurred. Besides, the relationship between various bonding angle and the change of electrical resistance was also studied. Both anti-phase and in-phase structures were bonded at 700 ℃ for 1 hr. It was observed that a thin amorphous layer (about 5 nm) existed at the anti-phase bonded interface. The amorphous layer in the anti-phase bonding structure caused the higher electrical resistance than that was in-phase bonding structure.

Layer transfer technique is one of important applications of wafer bonding to optoelectronic devices. A 50 nm n-$In_{0.5}Ga_{0.5}P$ layer with line patterns was transferred to the n-GaP substrate. This line patterned layer acted as a seed layer for quaternary alloy $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ heteroepitaxy. Almost no defects were observed in the transferred layer and only few changes in the optical property. Moreover, it was discovered that the interface electrical resistance rose while surface misorientations were added. The quaternary alloy which had low defect density and fine optoelectronic property was grown on the line patterned substrate successfully.

Wafer-direct-bonding technique is usually used to the fabrication of high brightness LEDs. However, bonding processes were usually performed at elevated temperatures,

possibly causing degradation in the quality of the LED structure. In addition to this, misorientation between the two bonded wafers may have caused defects between the wafers. In this study, these two problems were solved by bonding the InGaP/GaAs and GaAs wafers with an indium tin oxide (ITO) polycrystalline film at temperatures below 650 ℃. It was found that the bonding occurred mainly through the In transport from the InGaP to ITO, and that the electrical resistance decreased with the bonding temperature. Then, the intermediate layer was used to fabricate high brightness LEDs. Compared with wafer direct bonding technique, the lower threshold voltage and the higher operating current can be gained by using the ITO intermediate layer.