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Ge Epitaxial Growth on GaAs Substrates for Application to Ge-Source/Drain GaAs MOSFETs

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Ge films were epitaxially grown on GaAs(100) substrates and $Ga_{0.88}In_{0.12}As$(100) virtual substrates using an ultrahigh vacuum/chemical vapor deposition system. The incubation time of Ge growth depends on Ga(In)As surfaces that were processed by different wet chemical solutions. Growth behaviors, such as island growth at the initial stages and selective growth into recessed regions of GaAs, were studied by transmission electron microscopy. To test the quality of Ge grown on GaAs, an n^+-Ge/p-GaAs diode was fabricated. We propose that through Ge selective epitaxial growth, Ge can be used as the source–drain of a GaAs metal-oxide-semiconductor field-effect transistor (MOSFET) to overcome some intrinsic limitations of this device.
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For the past few decades, advances in Si complementary metal oxide semiconductor (CMOS) technology have been driven by device scaling, which has increased performance as well as reduced costs and controlled power consumption. However, as devices are scaled below 100 nm, the performance gain attributable to scaling is diminished. Presently, in industry, device performance is improved by mobility enhancement and achieved by applying strain to conventional Si metal-oxide-semiconductor field-effect transistors (MOSFETs) either through process-induced strain[1] or through substrate engineering.[2] However, the mobility benefits that can be achieved by straining Si are limited and are reduced by scaling, and there is a great interest in studying non-Si channel materials that have an even higher mobility enhancement potential. Fortunately, III-Vs promise to increase electron mobility by a factor of 10–30 times, which makes them great candidates for high speed, low power n-channel transistors.[3] However, III-Vs cannot make good p-channels, which are also needed for CMOS, because their hole mobilities are relatively low. Nevertheless, a better integration scheme would utilize III-V for the n-type field-effect transistor and Ge for the p-type field-effect transistor due to the higher hole mobility of Ge. In addition, some III-Vs such as GaAs are almost lattice-matched to Ge. Integration of GaAs and Ge can be achieved by epitaxial growth of either GaAs on Ge or Ge on GaAs. From the viewpoint of epitaxy, the growth of Ge on GaAs is advantageous over the growth of GaAs on Ge because the former lacks the problem of the antiphase boundary phenomenon, which is usually found with GaAs on Ge.[4] The growth of Ge on GaAs was investigated by a few groups using molecular beam epitaxy (MBE) systems in the early days.[5-7] Due to its potential applications mentioned above, Ge growth on GaAs has recently become a subject of interest again.[8,9] In this study, we grew Ge on GaAs substrates using a SiGe ultrahigh vacuum (UHV)/chemical vapor deposition (CVD) system. The GaAs surfaces going through different wet-etching processes can greatly affect the incubation time at the initial stages of Ge growth on GaAs. Finally, a Ge/GaAs diode with good current–voltage (*I-V*) characteristics was fabricated.

Experimental

In this study, GaAs(100) wafers and $Ga_{0.88}In_{0.12}As$ virtual substrates were used as the substrates for Ge growth. The $Ga_{0.88}In_{0.12}As$ virtual substrates used here were grown by an MBE tool on GaAs(100) wafers using a graded buffer layer technique. The $Ga_{1-x}In_xAs$ buffer layer was 0.4 μm thick, and the In composition (x) varied from 0 to 0.12. Their real structures are shown by the cross-sectional transmission electron microscopy (XTEM) image in Fig. 1. It reveals that most dislocations caused by the lattice mismatch between the $Ga_{0.88}In_{0.12}As$ layer and the GaAs substrate are confined inside the graded buffer layer, and the top 0.36 μm $In_{0.12}Ga_{0.88}As$ layer shows a reduced dislocation density, which means that this $In_{0.12}Ga_{0.88}As$ virtual substrate is good enough for Ge growth study. Before the Ge growth, all GaAs substrates including $Ga_{0.88}In_{0.12}As$ virtual substrates were first cleaned in acetone for 1 min and then rinsed in deionized water (DI) for 5 min. Subsequently, dilute HCl solution (HCl:DIW = 1:10) was used to remove the surface native oxides. After that, some GaAs substrates were separated out for etching by a solution of $H_2SO_4:H_2O_2:H_2O$ = 6:2:150. Following this etching step, HCl solution was again used to remove the surface native oxides. Summarily, in this work, three types of surfaces were created for the Ge to be grown on GaAs surfaces with only HCl clean (here called GaAs HCl surface), GaAs surfaces with HCl clean+$H_2SO_4:H_2O_2:H_2O$ etching + HCl clean (here called GaAs H_2SO_4 surface), and $Ga_{0.88}In_{0.12}As$ surfaces with only HCl clean (here called GaInAs HCl surface).

The growth of Ge was carried out using a UHV/CVD system with a base pressure of less than 2×10^{-8} Torr. After GaAs wafers were loaded into the growth chamber, they were first in situ prebaked at 550°C for 10 min. Then, the Ge layer was grown at the same temperature with a constant GeH_4 flow rate of 10 sccm. Throughout the entire growth process, the gas pressure in the growth chamber was kept at 30 mTorr.

For the study of selective epitaxy growth (SEG) of Ge on GaAs, the recessed regions in which the Ge was grown were fabricated on GaAs wafers. The fabrication steps were as follows: (*i*) A 400 nm thick SiO_2 layer was deposited onto a 2 in. GaAs wafer; (*ii*) SiO_2 windows were opened by lithography and HF solution wet etching; and (*iii*) using SiO_2 as a mask, the recessed GaAs regions were formed by etching GaAs using a solution of $H_2SO_4:H_2O_2:H_2O$ = 6:2:150. The detailed etching rates for the different chemical solutions are shown in Fig. 2.

XTEM was used to characterize the variations in thickness of the deposited Ge films. The transmission electron microscopy (TEM) samples were prepared through mechanical polishing and perforation by Ar-ion milling. TEM images were recorded using an FEI Tecnai F20 microscope operated at 200 kV. The structural composition and the chemical bonding configuration of GaAs surfaces, just after being processed by different wet-etching solutions and before Ge UHV/CVD growth, were examined using X-ray photoelectron spectroscopy (XPS) with an Al Kα radiation source (1486.6 eV). We calibrated the peak position and subtracted the background sig-

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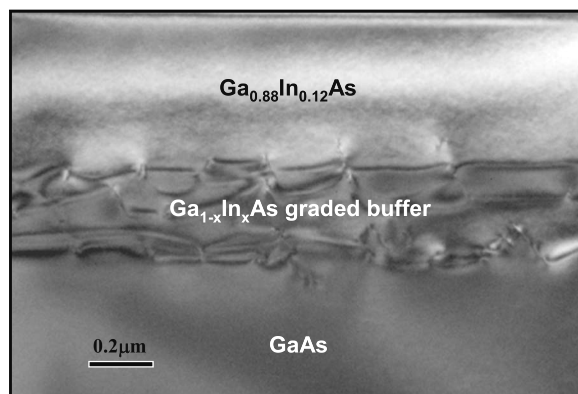

Figure 1. The XTEM image of $Ga_{0.88}In_{0.12}As$ virtual substrates. Most dislocations are confined inside the $Ga_{1-x}In_xAs$-graded buffer layer, and the top 0.3 μm $Ga_{0.88}In_{0.12}As$ has a much reduced threading dislocation density.

nal by considering the positions of substrate peaks in Ga 3d/As 3d spectra and a Shirley-type background. To extract each chemical component from the photoemission spectra, a rigorous fitting process was adopted. After the peak positions were ascertained, they were applied to reconstruct the original spectra and then to extract each respective contribution. During the deconvolution of the spectra, the peak areas were varied while maintaining the full width at half-maximum and the ratio of the Gaussian to Lorentzian distribution constant. Finally, we studied the bonding configuration on these etched GaAs surfaces by combining the analysis of Ga 3d and As 3d core levels. To test the quality of the Ge layer grown on GaAs, an n^+-Ge/p-GaAs heterojunction diode was fabricated. High n-type doping in Ge was formed by phosphorus implantation (1×10^{15} cm^{-2}, 30 keV), which was followed by dopant activation at 600/700°C for 30 s in N_2 ambient with the Ge surface being capped by SiO_2. Al and AuGe/Ni/Au were used as the top and back-side electrical contacts, respectively. The *I-V* characteristic for the n^+-Ge/p-GaAs heterojunction diode was measured using a Keithley 4200 semiconductor analyzer system.

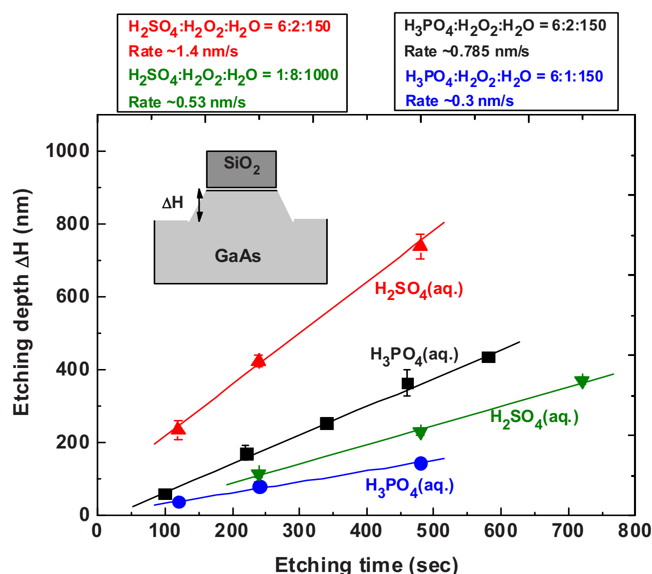

Figure 2. (Color online) GaAs etching depth vs etching time for the different chemical solutions. The inset shows the actual process through which the etching thickness can be easily measured. These data can supply a reference for the recess formation on the GaAs substrate.

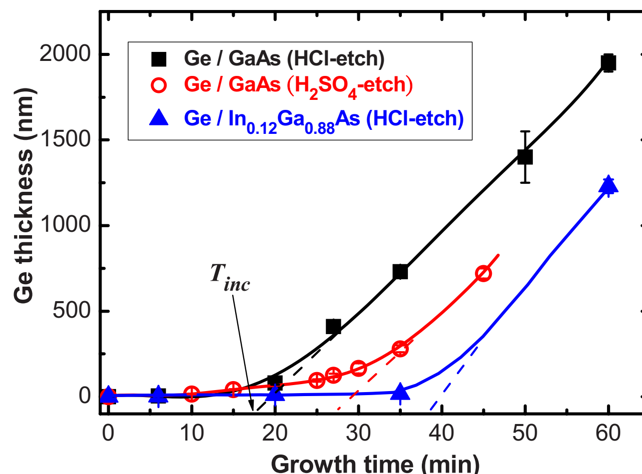

Figure 3. (Color online) Ge growth thickness vs growth time on the different Ga(In)As surfaces. The solid lines are drawn as a guide for the eyes. The incubation times (T_{in}) for Ge grown on GaAs HCl surface, on GaAs H_2SO_4 surface, and on GaInAs HCl surface are 19, 28, and 37 min, respectively.

Results and Discussion

Effects of wet etching of Ga(In)As surfaces on incubation time of Ge growth.— It has been reported[9] that a specific incubation time is required for Ge growth on GaAs. In our study, this incubation time (T_{inc}) was still dependent on the type of etched Ga(In)As surface.

Figure 3 displays the thickness variation in the grown Ge layers vs growth time (T_g) on a GaAs HCl surface, a GaAs H_2SO_4 surface, and a GaInAs HCl surface. For all these surfaces, the Ge growth rate was zero at the beginning, and later, the Ge grew at a very low growth rate. After a critical time, the Ge entered into a steady growth (corresponding to the linear region of plots for Ge thickness vs growth time in Fig. 3). If the incubation time (T_{inc}) is defined as the intersection between the line corresponding to the steady growth and the growth time axis, then from Fig. 3, Ge growth requires a longer T_{inc} (~28 min) on a GaAs H_2SO_4 surface than on a GaAs HCl surface (T_{inc} ~ 19 min), and Ge growth on a $Ga_{0.88}In_{0.12}As$ HCl surface requires the longest T_{inc} (~37 min). Bai et al.[9] reported that the Ge growth on GaAs was initiated via the formation of a Ge–Ga bond because the Ge–Ga bond has a lower formation energy than the Ge–As bond. A rich arsenic (As) coverage on a GaAs surface could block Ge atoms from bonding with Ga atoms and thus impede Ge adatom attachment, leading to the long incubation time. In other words, a GaAs surface with a higher Ga-to-As ratio facilitates Ge nucleation and epitaxy because there are more available Ga sites for Ge adatoms to bond. Next, we demonstrate, by using XPS, that the T_{inc} is truly related to the amount of As on the GaAs. Figure 4a presents the As 3d photoemission spectra for the GaAs HCl surface and the GaAs H_2SO_4 surface. The deconvoluted peaks of the As–As, AsO_x, As_2O_3, and As_2O_5 species appeared in the spectra at binding energies of 0.9, 2, 3.4, and 4.4 eV, respectively, above that of the GaAs substrate. Obviously, the amounts of both As–As and As oxides were higher for the GaAs substrate receiving a H_2SO_4 rinse. In this work, the deconvolution process was also performed on the spectra of Ga 3d core level, and we thus evaluated the signal ratios of all chemical species on the etched GaAs substrates, as summarized in Fig. 4b. The GaAs HCl surface has an As coverage of 11.8%, and the GaAs H_2SO_4 surface has an As coverage of 21.4%. Correspondingly, the growth of Ge on these two surfaces has an incubation time of 19 and 28 min, respectively, indicating that more As coverages on the GaAs surface lead to a longer incubation time for Ge growth. Regarding the growth of Ge on a GaInAs surface, it is speculated that the In–Ge bond, like the As–Ge bond, also has a higher formation energy than the Ga–Ge

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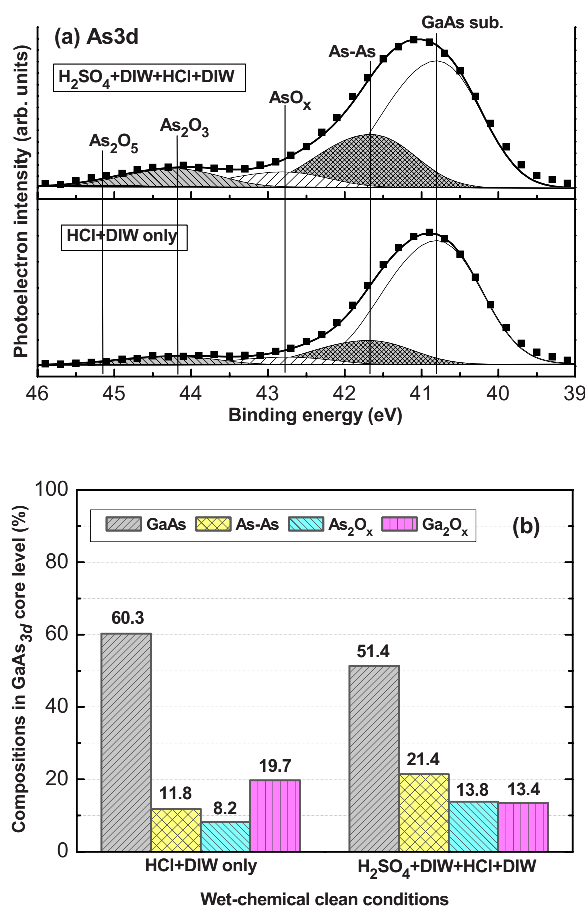

Figure 4. (Color online) (a) The As 3d XPS spectra of the GaAs surfaces subjected to different acid etchants and (b) the analysis of composition ratio on the etched GaAs surfaces revealed by XPS.

bond; thus, In, like As, also tends to impede Ge adatom attachment, so the available Ga sites on the GaInAs surface for Ge adatoms to bond are obviously less than those on GaAs surfaces, resulting in the longest observed incubation time for the growth of Ge on GaInAs.

Ge growth behavior on GaAs.— Figure 5 shows XTEM images of the Ge layer at the initial growth stage. The GaAs substrate here was etched by the chemical solution of H_2SO_4:H_2O_2:H_2O = 6:2:150 before Ge UHV/CVD growth.

At the first stages, the Ge film grew in island mode. With the continuance of growth, the islands started to merge and then formed a blanket film. When the growth time was long enough, the surface of the Ge layer became flat. Figure 5 also reveals that, before forming a blanket film, the Ge islands grew tall at almost the same height and merged with two-dimensional spreading. For the lattice-mismatch material system, such as Ge/Si and GaInAs/GaAs, the initial growth mode of film also start as islands, and island formation is driven by the lattice-mismatch-induced strain.[10] However, for Ge on GaAs, there is no lattice-mismatch strain between Ge and GaAs, and so the mechanism of Ge island formation on GaAs must be different from that of Ge/Si or GaInAs/GaAs. Through detailed studies of the surface morphology of Ge films on GaAs(100) by using low energy electron diffraction and scanning tunneling microscopy, Wang et al.[5] reported that the Ge islands on GaAs(100) are in Stranski–Krastanov mode; the driving force for the formation of this mode is a reduction in the total surface energy by minimizing substrate-induced electronic effects.

Figure 6 shows the TEM image of Ge (T_g = 35 min) selectively grown in the recessed GaAs regions. A good quality Ge epitaxy without dislocation formation was achieved. No Ge was deposited

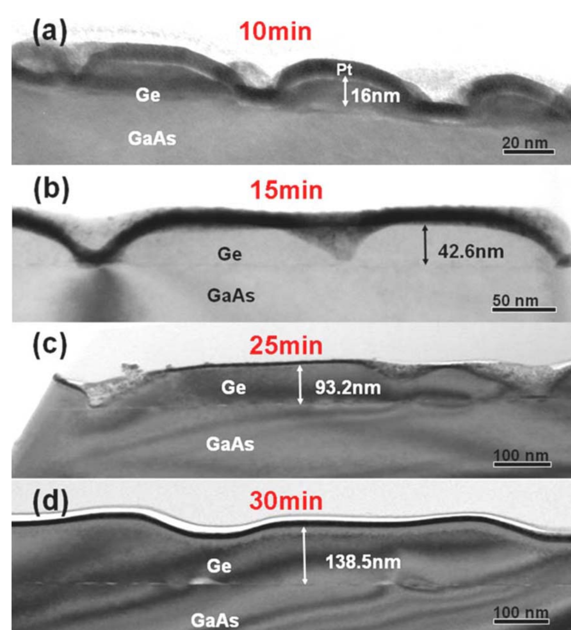

Figure 5. (Color online) The XTEM images of Ge layer on GaAs substrate at different growth times: (a) 10, (b) 15, (c) 25, (d) 30, and (e) 50 min.

onto the SiO_2 region, which indicates a better selective growth of Ge on GaAs than on SiO_2. As mentioned in the introduction section, the III-V materials are being considered as high mobility channels for further high speed and low power metal-oxide-semiconductor device applications. However, so far, the drive current of the III-V MOSFET has not outperformed Si at the sub-100 nm channel length. The root cause is related not only to the dielectric–substrate interface quality but also to the lower density of states and the limited dopant level for III-V.[11] We thus propose that the structure shown in Fig. 6 could potentially tackle these critical issues and hence boost the current drive capability by using Ge as the heterostructural source–drain of a GaAs nMOSFET.

The fabricated n^+-Ge/p-GaAs diode.— Figure 7 shows the diode characteristics of the n^+-Ge/p-GaAs heterojunctions undertaking dopant activation at 600 and 700°C. Compared to the properties of the 700°C annealed diode, the 600°C annealed sample actually

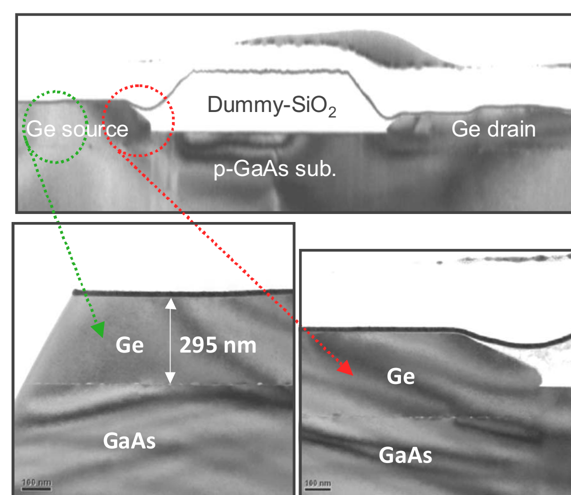

Figure 6. (Color online) The XTEM images of Ge layer selectively grown into the recessed region of GaAs substrate. The Ge layer has an excellent SEG on GaAs compared with that on SiO_2.

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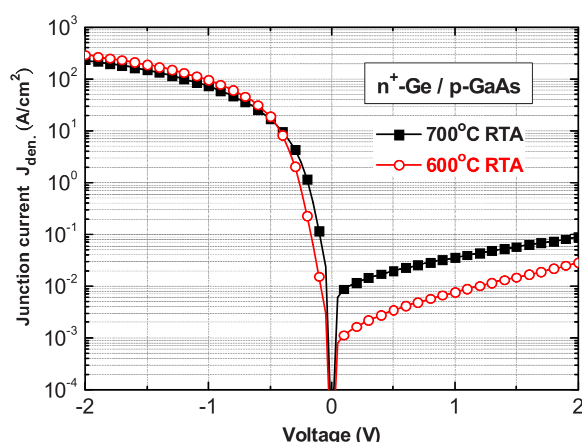

Figure 7. (Color online) The diode characteristics of n+-Ge/p-GaAs heterojunction with dopant activation at 600 and 700°C for 30 s, respectively.

exhibited a higher forward current (J_F) along with a lower reverse leakage current (J_R). The magnitude of the rectifying ratio can be up to 4 orders (in the voltage range of ± 1 V), where the values of J_F and J_R were 9.5×10^1 and 7.7×10^{-3} A/cm^2, respectively. Raising the temperature to 700°C resulted not only in a slight degradation of the J_F to 7.2×10^1 A/cm^2 but also in an increase in the J_R to 3.6×10^{-2} A/cm^2. From the J_R characteristics of both 600 and 700°C annealed samples, we also noticed that the J_R–V_R (reverse voltage) curves slightly deviate from that predicted by the Shockley–Read–Hall theory, where J_R has a square root of V_R dependence, implying the possible onset of the trap-assisted tunneling mechanism in these diodes. Moreover, for the 600°C annealed diode, the ideality factor n_f of 1.17 and the series resistance R_s of 41.4 Ω were extracted from their J_F characteristics, with values of 1.42 and 48.5 Ω for the n_f and R_s of the 700°C activated diode, respectively. The corresponding barrier height Φ_b was estimated to be $0.52(\pm 0.04)$ eV for the 600°C diode, and it decreased slightly to $0.48(\pm 0.04)$ eV for the 700°C diode, where the variation comes from the uncertainty in the Richardson constant A^*. In terms of the above experimental results, the diode characteristics of these n+-Ge/p-GaAs heterojunctions are acceptable, but still, more optimization work is needed.

Conclusions

Ge epitaxial growth on GaAs(100) substrates and $Ga_{0.88}In_{0.12}As$(100) virtual substrates was studied by using a UHV/CVD system. The incubation time of Ge growth depended on the different Ga(In)As surfaces going through different wet chemical processes. One explanation considered the dependence on the number of available Ga sites for the bonding of Ge adatoms on different Ga(In)As surfaces. Fewer Ga sites tended to prolong the incubation time. In this study, Ge was easily grown selectively into GaAs recessed regions with good quality. Based on the grown material, an n+-Ge/p-GaAs diode was fabricated. The diode showed a normal rectifying characteristic, with the rectifying ratio being up to 4 orders of magnitude. These experimental results imply that Ge growth on GaAs can provide an additional way to integrate Ge and GaAs. For example, Ge can possibly be used as the hetero-source/drain of GaAs nMOSFET to further enhance the device performance.

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