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Characterization of Highly Strained nFET Device Performance and Channel Mobility with SMT

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This paper compares and analyzes the strained negative channel field effect transistor (nFET) device performance and the channel mobility behavior obtained by the stress memorization technique (SMT) using two different types of nitride films. These nitride film properties and wafer bowing during SMT fabrication are investigated. The electrical properties of SMT strained nFET devices including current–voltage characteristics, transconductance, carrier mobility, and interface state (D_{it}) are also analyzed. Although SMT nitride strain can enhance electron mobility, it is critical to control the nitride properties and its hydrogen content to minimize electron mobility degradation due to interface-state generation. Thus, a simple view of the essential physics of mobility enhancement in SMT strained nFETs has been provided. Results in this work also provide guidance to further nFET performance enhancement in the ever-more challenging device targets of future technology generations.
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Historically, improvements in the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) have relied on the aggressive reduction of physical geometries as guided by physics-based scaling rules.[1] However, the increase in channel impurity concentration and the raise in vertical field required to control the short channel effect (SCE) actually degrade the carrier mobility and transistor performance. As the industry approaches the physical limitations of the traditional scaling techniques, alternative approaches for improving device performance have become increasingly attractive. Among the most promising of these techniques is the production of high mobility silicon channel structures most commonly accomplished using strained silicon technology. Strained silicon technology has emerged as one of the leading approaches to enhance the performance of today's highly scaled semiconductor devices. This technology has been adopted in production since the 90 nm process node,[2] and apparently this technology will continue through future generations. The strain can be induced either uniaxially or biaxially and strongly depends on integration challenges and the ability to maintain and control enhancement in aggressively scaled devices.

Many strained silicon approaches have thus been developed to enhance carrier mobility.[2-4] Among these emerging approaches, uniaxial strained silicon technologies have become the mainstream for electron and hole mobility improvement especially under high oxide electrical field conditions.[3,4] For instance, a highly tensile nitride capping layer integrated as a contact etch stop layer (CESL) has been greatly utilized in advanced MOSFET fabrication owing to the resulting uniaxially tensile mechanical stress created in the negative channel field effect transistor (nFET) channel and the resulting electron mobility enhancement.[5,6]

Another novel channel strain enhancement technique utilizing nitride dielectric deposition, commonly known as stress memorization technique (SMT), was first proposed by Chen et al.[7] SMT improves nFET performance by depositing a sacrificial tensile nitride stressor on top of the nFET poly gate electrode and source–drain (S/D) after the S/D implantation. The nitride layer covers the nFET regions during subsequent dopant activation annealing and is stripped off after the activation annealing has been completed, resulting in a higher drive current. The presence of the stress from the SMT nitride capping layer during the S/D activation anneal results in plastic deformation, displacing the silicon atoms in the transistor channel from their equilibrium position. The silicon atoms remain in their new positions after the anneal is complete, in effect "memorizing" the tensile stain in the channel, resulting in nFET device improvement. Furthermore, when combined with the strained CESL technique, SMT provides additional strain to the n-channel,[8] creating prospects for using strained silicon technology to achieve the device performance targets of aggressively scaled complementary metal oxide semiconductor design rules.

While a detailed understanding of the SMT process remains the subject of active debate, recent works have suggested that the improved nFET performance results from the inherently memorized tensile stress in the n-channel by the mechanism described above.[7-10] Therefore, to understand and maximize the benefit obtained from the highly strained nitride on the silicon channel, SMT strained nFET device performance including threshold voltage (V_t), transconductance, electron carrier mobility, and the associated interface-state density D_{it}, have been characterized by electrical measurement techniques. Moreover, the wafer bowing measurements are presented, quantifying the evolution of stress throughout the entire SMT fabrication process.

Experiment and Characterization

The devices were fabricated in the National Nano Device Laboratories (NDL) on 6 in. (150 mm) Si wafers using a conventional MOSFET process flow including local oxidation of silicon isolation, gate oxide, spacer, S/D implantation, thermal annealing, and Al metallization processing, as listed in Fig. 1. All the nFET devices characterized in this study had 3 nm thick gate oxide thermally grown in a vertical furnace and a 150 nm thick N^+ poly-Si layer as the gate electrode. After gate dielectric and gate electrode deposition and patterning, desired ion species were implanted through a deposited 100 A plasma-enhanced tetraethyl orthosilicate (TEOS) screen oxide to form the N^+ S/D region. This screen oxide was employed to reduce the N^+ region junction depth.

Before the S/D activation annealing, an SMT process flow for the strained nFET similar to that proposed by Chen et al.[7] was employed. After S/D annealing, a permanent stress was created in the channel region, resulting in strain-enhanced carrier mobility. For the SMT strained nFET nitride capping layer, a ~110 nm tensile nitride film was deposited on the whole device structure including the poly gate and the S/D region. The SMT strain generation obtained from nitride films deposited by two different chemical vapor deposition (CVD) processes are compared in this study. The first type of nitride film was deposited under a high temperature 780°C (hereafter denoted as HT-SiN) Low Pressure Chemical Vapor Deposition (LPCVD) system using a batch-type furnace tool, and thus the HT-SiN nitride film coated both the front and back sides of the wafer. On the other hand, the second nitride film was deposited at a relatively low temperature (hereafter denoted as LT-SiN) 300°C process condition using a single-wafer plasma-enhanced chemical vapor

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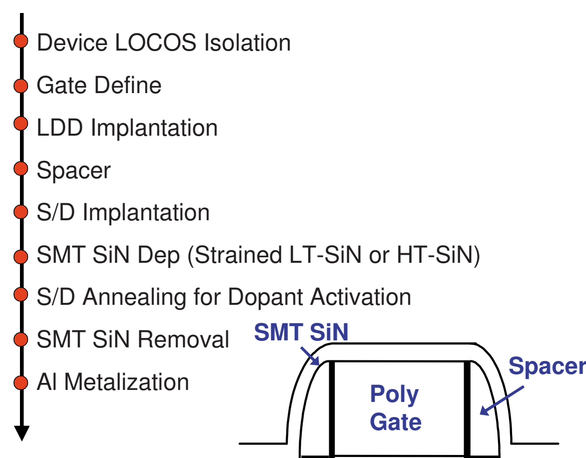

Figure 1. (Color online) SMT process flow. The SMT process deposits a nitride layer over the gate before annealing. The presence of this nitride layer during the subsequent S/D annealing acts to increase tensile strain in the nFET channel. Though this SMT nitride is removed after the annealing, the stress memorized in the channel region remains, and mobility of electrons increases.

deposition (PECVD) system with NH_3, N_2, and SiH_4 as the main reaction gases, thus depositing the LT-SiN nitride film only on the front side of the wafer.

Afterward, to facilitate metallization, the SMT nitride films were removed using a wet chemical etchant H_3PO_4. Passivation was performed by depositing a 300 nm thick TEOS oxide, followed by patterning and etching of contact holes, and finally by metallization. After a completion of the metallization processes, the wafers were annealed at 400°C in a forming gas ambient and the electrical characteristics of the fabricated devices were measured. The nominal device dimension evaluated was a gate length of 0.4 μm and a width of 10 μm. The device characteristics were measured using a semiconductor parameter analyzer (HP 4156A, plus Agilent ICS software). The threshold voltage was determined by the constant drain current method when the drain current equals 10^{-7} W/L(A).[11] The linear and saturation mode threshold voltages, V_{t_lin} and V_{t_sat}, were extracted at drain voltages of 50 mV and 2 V, respectively.

The thicknesses of the LT-SiN and HT-SiN films were measured by a SOPRA ellipsometer. Fourier transformation infrared reflectivity (FTIR) spectra were also measured to provide information concerning the bonding structure of the SMT nitride films. The FTIR spectra were obtained by subtracting the absorbance obtained before deposition from that measured after deposition using a Bio-Rad QS-300 spectrometer.

Wafer curvatures or bowing measurements were performed using a Tencor FLX-2320 thin-film stress metrology instrument, and film stress was subsequently obtained by transforming this wafer curvature using a conversion equation such as Stoney's formula.[12] For highly scaled modern semiconductor devices, such wafer level thin-film residual stress characterization is crucial, and the strain level remaining in the device itself is a major factor in determining the final electrical characteristics, yield, and reliability. This curvature measurement technique was also applied to the patterned electrical wafers to characterize the generated SMT strain.

Results and Discussion

Film properties of LT-SiN and HT-SiN.— Generally speaking, compared to LPCVD films, PECVD materials have a much lower thermal budget, and their film properties can be tuned and controlled over a much wider range by varying appropriate process parameters. In this work, the LT-SiN is formed at 300°C by PECVD with a mixed gas containing SiH_4, NH_3, and N_2, while the HT-SiN is formed at 780°C in an LPCVD furnace with a mixed gas containing SiH_2Cl_2 and NH_3.

Table I. Measured nitride thickness and associated thickness shrinkage rate (%) before and after S/D activation annealing.

Thickness (A)	LT-SiN	HT-SiN
As deposited	1163	1075
After annealing	1028	1044
Thickness shrinkage (%)	11.6	2.9

Table I depicts the LT-SiN and HT-SiN nitride film thicknesses before and after S/D annealing. The typical as-deposited nitride thicknesses (measured on unpatterned monitor wafers) were ~1150 and ~1100 A for LT-SiN and HT-SiN, respectively. However, after annealing, the thicknesses of both nitride films reduced to ~1050 A. The calculated thickness shrinkage rate after annealing for the LT-SiN is ~12% compared to ~3% for that of the HT-SiN.

For strain nitride for CESL application,[5,6] the magnitude of the thin nitride film stress is one of the key properties that can determine the device performance and reliability lifetime. The deposition tool and process parameters largely determine the type and level of nitride stress that develops on the wafer. Because of its simplistic nature, the curvature measurement scheme is traditionally the most widely acknowledged method, and the film stress is determined by converting the measured curvatures using Stoney's equation,[12] as formulated in Eq. 1. A highly stressed film causes wafer deformation, as schematically drawn in Fig. 2

$$\sigma = \frac{E}{6(1-\upsilon)}\frac{t_s^2}{t_f}\left(\frac{1}{R_1}-\frac{1}{R_2}\right) \quad [1]$$

where σ is the film normal stress, E is the elastic modulus of the substrate, t_s is the substrate thickness, t_f is the film thickness, υ is Poisson's ratio of the substrate, and $(1/R_1 - 1/R_2)$ is the local curvature caused by intrinsic stress before and after film deposition.

SMT nitride stress and stress change behavior before and after annealing are measured and shown in Table II. All stress levels are positive, indicating tensile stress. The LT-SiN shows a relatively large increase in tensile stress ~700 MPa (360–1050 MPa), while the HT-SiN shows a much smaller 60 MPa stress increase (1010–1070 MPa).

The representative SiN layer FTIR spectra after CVD deposition and after S/D annealing are shown in Fig. 3. The FTIR analysis results obtained on LT-SiN and HT-SiN films are shown in Fig. 3a and b, respectively. The chemical bonding present in CVD deposited nitrides has been characterized by FTIR according to Lu et al.[13] The dominant spectral feature in each film is at approximately

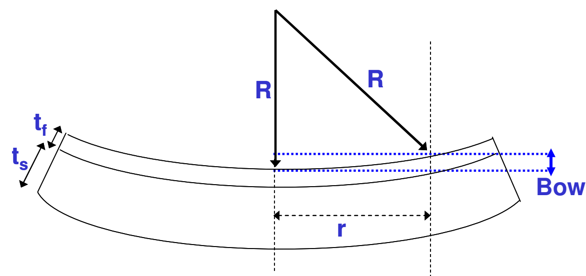

Figure 2. (Color online) Bow is characterized in terms of the curvature of the substrate, which is the height difference between the center and the edge of the wafer resulting from the wafer manufacturing process or the presence of a residually stressed thin film on one side of the wafer. In Fig. 2, the film is under positive (tensile) stress, and the R (radius of curvature) is positive. Therefore, the bow is also positive according to Eq. 2.

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Table II. Measured nitride stress variation before and after S/D activation annealing.

Stress (MPa)	LT-SiN	HT-SiN
As deposited	360	1010
After annealing	1050	1070
Delta stress	690	60

820–850 cm^{-1} and is associated with the Si–N asymmetric bond-stretching mode. The remaining features in these spectra are due to vibrations involving hydrogen atom motion: (*i*) a N–H bond-stretching mode at ~3350 cm^{-1}, (*ii*) a N–H bond-bending mode at ~1150 cm^{-1}, and (*iii*) a Si–H bond-stretching mode at ~2150 cm^{-1}, respectively.

The as-deposited LT-SiN spectrum of Fig. 3a shows substantially stronger Si–H and N–H bonds compared with the as-deposited HT-SiN spectrum of Fig. 3b. This results from the higher deposition temperature of the LPCVD process. Hydrogen atom is more mobile and active and less likely to remain in a stable Si–H or N–H bond.

The FTIR spectra for nitrides with LT-SiN and HT-SiN after S/D annealing are also shown in Fig. 3a and b, respectively. We observe that the intensities of the Si–H and N–H bond peaks become negligible after annealing, suggesting hydrogen removal during the S/D activation anneal.

The change is much more dramatic in LT-SiN because of the large amount of hydrogen initially incorporated during the deposition of the PECVD film. The magnitude of the reduction in hydrogen content is directly responsible for the irreversible increase in the tensile stress of the film due to the volume reduction, as reported by Hughey and Cook.[14-16] As observed in Fig. 3a, the FTIR spectra show a reduction of the N–H and Si–H bond peaks, which agrees with this scenario. This phenomenon is typical of the LT-SiN formed by PECVD and is well correlated with the LT-SiN film's massive stress change toward a tensile equilibrium state after hydrogen removal, as shown in Table II. Apparently, the smaller stress change observed in Table II for the HT-SiN layer is mainly due to less initial hydrogen concentration during nitride layer deposition and less hydrogen bonding change, as indicated by the FTIR spectra in Fig. 3b.

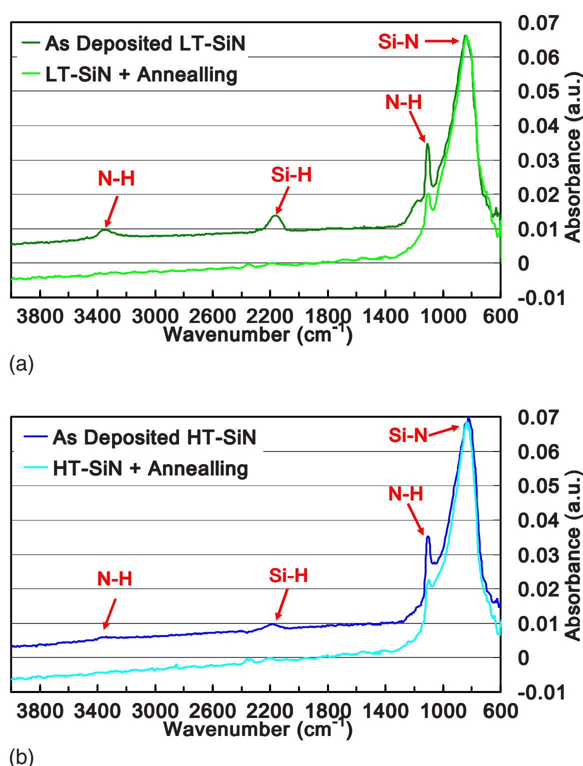

Figure 3. (Color online) (a) LT-SiN film FTIR analysis results before and after S/D activation annealing. FTIR spectra indicated features associated with[13] (*i*) the Si–N asymmetric bond-stretching vibration at 820–850 cm^{-1} and (*ii*) the bond-bending vibration of the N–H group at ~1150 cm^{-1}, (*iii*) the bond-stretching vibration of the Si–H group at ~2150 cm^{-1}, and (*iv*) the bond-stretching vibration of the N–H group at ~3350 cm^{-1}. (b) HT-SiN film FTIR analysis results before and after S/D activation annealing. HT-SiN sample contains much less Si–H and N–H bonds than those of LT-SiN samples in (a).

Device wafer bow measurement.— Wafer bowing refers to the curvature of the wafer substrate, i.e., the height difference between the center and the edge of the wafer. A graphical description of wafer bow is shown in Fig. 2 and formulated in Eq. 2

$$\text{Bow} = (|R| - \sqrt{R^2 - r^2})\text{sign}(R) \quad [2]$$

where R is the radius of curvature and r is the scan distance.

When applying strain silicon technology to increase carrier mobility, wafer bow is a key metrology item for chipmakers as they transition to production on 300 or 450 mm wafer sizes because larger wafers can bow, or bend, more than twice as much as the 150 mm wafers used here on the deposition of a given film. The larger global wafer bow accumulates larger stress on the wafer and increases the device's susceptibility to film cracking, delamination, and electrical performance degradation, which would all negatively impact transistor structural integrity and can result in serious circuit yield loss.

Wafer bow can be modulated by the presence of a stressed thin film deposited on the wafer. Therefore, wafer bow is a quantitative index for the bending (curvature) of a wafer during the device fabrication processes. For instance, wafer bow due to electroplated copper films with different copper seed layers has been studied.[17] Furthermore, previous observations by Yu et al.[18] have also revealed a correlation between the wafer bow height and defect injection into strained epitaxial SiGe upon activation laser and rapid thermal annealing (RTA) annealing. This study further indicates that the final wafer curvature was determined by the initial shape of the wafer plus the deformation caused by the subsequent fabrication processes.

To successfully apply SMT technology, it is essential to utilize wafer bow measurement to understand the SMT strain behavior and to minimize the SMT strain induced defect creation and/or strain relaxation after annealing when large SMT strain is present. Because any wafer has some initial curvature and surface irregularities are caused by several front–end processing steps occurring before SMT, a curvature measurement was performed before the deposition of the SMT capping nitride film. Further curvature measurements were performed after each of the subsequent SMT process steps such as nitride film deposition, RTA for S/D annealing, and nitride strip. These data were compared to the initial curvature. Figure 4 plots the increased wafer bow at each SMT process step and demonstrates that wafer curvature represents the SMT strain generated in the fabricated silicon device. The LT-SiN SMT film stress causes significantly higher levels of curvature in device wafers after SMT deposition and the subsequent S/D activation annealing. It indicates that wafers processed with SMT using LT-SiN are significantly warped compared to those processed with HT-SiN. This is likely because HT-SiN is processed with a double-sided coating furnace batch system, so the stress from the HT-SiN films on the front and back sides of the wafer cancel each other out to produce much less macroscopic wafer bending. This does not imply that there is no SMT strain generated by HT-SiN. However, with SMT processing using LT-SiN, the wafer bow is increased further after S/D activation annealing due to the large increase in film stress reported in Table II.

Recrystallization of amorphized silicon upon thermal annealing leads to strain and stress generation in the silicon material itself.[19-22]

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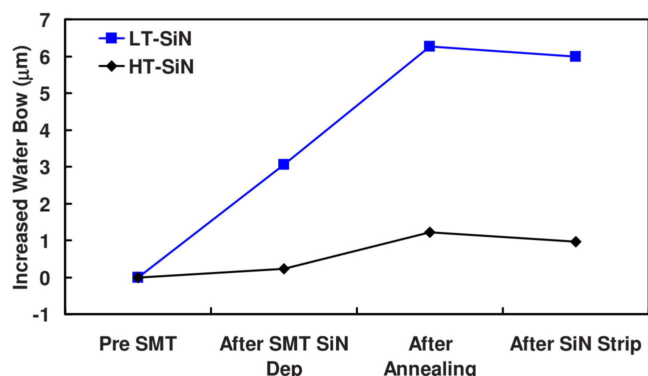

Figure 4. (Color online) Increased device wafer bow height measured on patterned wafers at different SMT stages to evaluate the SMT strain behavior.

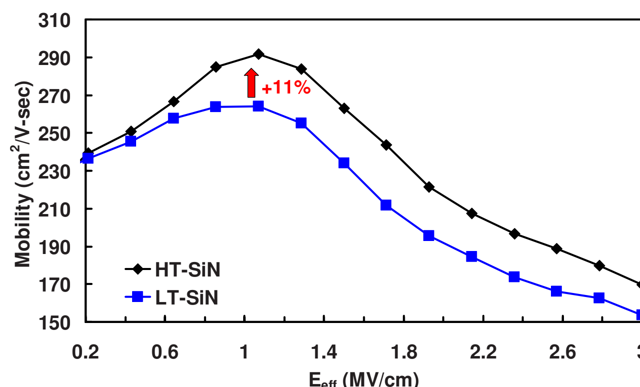

Figure 6. (Color online) Measured 10 × 0.4 μm nFET mobility at V_d = 50 mV. There is an ~11% improvement in the peak value of electron mobility with the adoption of HT-SiN as the SMT capping layer.

Because the transistor's poly-silicon gate and the S/D region were all amorphorized after high dosage S/D implantation, this increased tensile wafer curvature after annealing is likely to result from the SMT capping nitride film stress change and the strain exerted by the recrystallization of the amorphized S/D regions upon S/D activation annealing. Nevertheless, wafer warpage continues to exist even after the SMT nitride is subsequently removed, both for wafers processed with SMT by LT-SiN and for those with HT-SiN. This can be viewed as the generation of the SMT strain, which remains present in the wafer after completing the SMT process. Moreover, as the electron mobility in the channel can be increased by tensile strain in the in-plane longitudinal direction and by compressive strain in the out-of-plane vertical direction according to the piezoresistance model,[2,4,23] this "memorized" SMT strain in the poly-Si gate and S/D region can thus enhance the electron mobility and the nFET drive current.[7-10]

nFET device mobility and SCE characterization.— In addition to the enhanced wafer curvature exerted by the memorized strain, as shown in Fig. 4, electrical characterization was preformed to study the impact of SMT on nFET device (W/L = 10/0.4 μm) transconductance and mobility. Figure 5 plots the linear transconductance G_{m_lin} improvement resulting from the HT-SiN SMT process. Compared to LT-SiN process, a maximum G_{m_lin} enhancement of around 13% under a drain voltage of 50 mV is obtained. The nFET field-effect electron mobility, measured at a drain voltage of 50 mV by the conventional split capacitance–voltage (C-V) method,[24] is shown in Fig. 6. The maximum field-effect electron mobilities are 292 and 264 cm^2/V s, respectively, in these two samples. Similar to the findings in Fig. 5, the field effective mobility of the device with the HT-SiN SMT is also over 10% higher than the one of the device integrating LT-SiN. In Fig. 5 and 6, there is an obvious transconductance and carrier mobility improvement when HT-SiN is used as an SMT layer. These results clearly suggest that the HT-SiN SMT process induces a higher permanent stress in the channel region, and the electron mobility is thus enhanced after completing S/D annealing. Thus, it can also be concluded from this work that the "optimized" SMT process can further enhance nFET carrier mobility and device performance, as previously reported.[7,9,10] The retained transconductance G_{m_lin} and mobility improvement, even after the removal of the stressor film, can be attributed to a stress "memorization" effect.

The linear and saturation threshold voltages (V_{t_lin} and V_{t_sat}) are plotted as a function of channel length in Fig. 7. Regarding SCE control, neither HT-SiN nor LT-SiN films demonstrate a significant nFET V_t roll-off from a long channel (L = 10 μm) down to a short channel (L = 0.4 μm), which indicates that processing with the capped SMT nitride improves nFET SCE performance by retarding n-type dopant diffusion upon subsequent activation annealing.[8] Moreover, drain induced barrier lowering (DIBL) can be calculated from Eq. 3 as the threshold voltage difference between linear and saturation modes, divided by the difference in the applied drain voltage

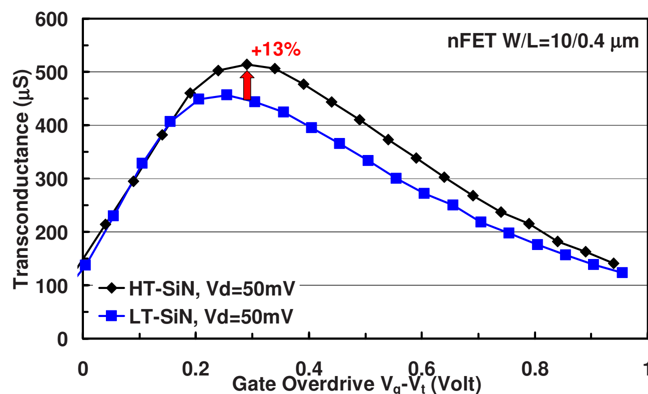

Figure 5. (Color online) Measured 10 × 0.4 μm nFET G_{m_lin} at V_d = 50 mV. There is an ~13% improvement in the peak value of G_{m_lin} with the adoption of HT-SiN as the SMT capping layer.

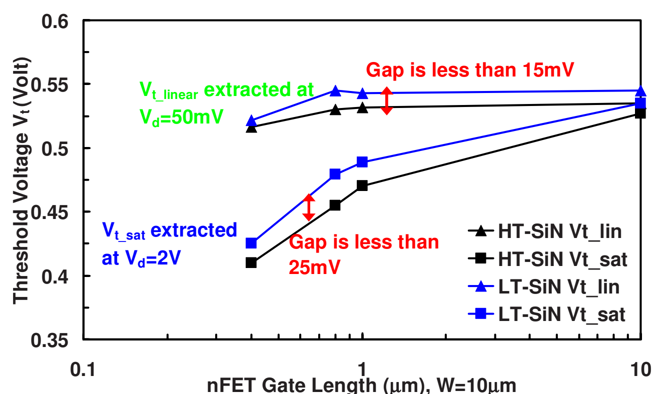

Figure 7. (Color online) Measured W = 10 μm nFET V_t as a function of channel length; LT-SiN as SMT capping layer improves nFET SCE with less V_t roll-off.

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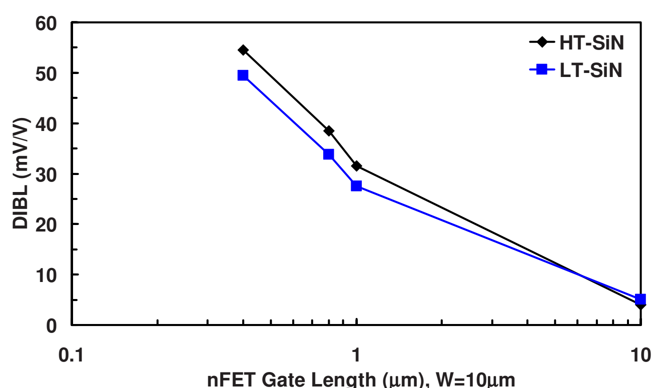

Figure 8. (Color online) Calculated $W = 10\ \mu m$ nFET DIBL. Slightly improved DIBL at reduced gate length nFET devices can be observed with LT-SiN as the SMT capping layer.

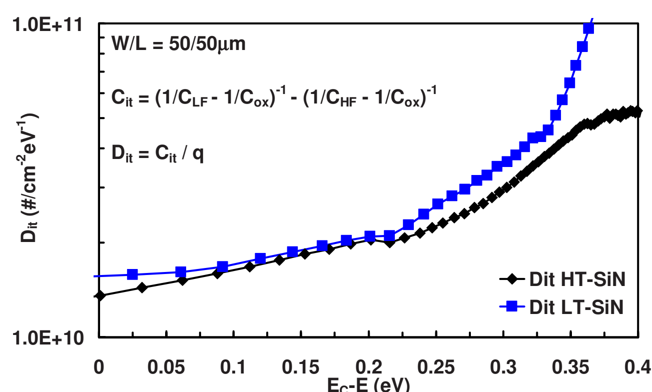

Figure 9. (Color online) Measured interface-state density (D_{it}) characteristics as a function of trap energy near the conduction band edge using 50 μm square MOS capacitors by high–low C-V technique.[27] The interfacial quality is degraded with the adoption of LT-SiN as the SMT capping layer when trap energy range ($E_C - E$) is greater than 0.25 eV, where E_C is the energy of the conduction band edge and E is the interface-state energy.

$$\text{DIBL} = \Delta V_t/\Delta V_{ds} = 1000^{*}(Vt_{\text{lin}} - Vt_{\text{sat}})/(2 - 0.05)\ (\text{mV/V}) \quad [3]$$

The calculated DIBL is plotted as a function of channel length in Fig. 8. DIBL reflects the influence of the drain voltage on the carrier potential in the channel.[25] The slightly increased DIBL by HT-SiN observed in Fig. 8 can be attributed to increased dopant diffusion encroaching from the S/D extension during the deposition of HT-SiN due to its higher deposition temperature. Therefore, to lower the DIBL and improve the SCE performance, a lowered thermal budget process is always preferred to suppress dopant diffusion.

A large shift in the threshold voltage V_t can often indicate a change in the device's dopant distribution profile or the generation of bulk traps or interface states[11] due to unoptimized stressor processing techniques, which can adversely impact device performance without strain engineering benefits. However, from the threshold voltage data in Fig. 7, the linear threshold voltage (V_{t_lin}) difference between wafers processed by the HT-SiN and LT-SiN SMT processes is less than 15 mV, and the saturation threshold voltage (V_{t_sat}) difference is also less than 25 m V. Such small V_{t_lin} and V_{t_sat} differences between HT-SiN and LT-SiN SMT processes suggest that the enhanced thermal budget by the furnace deposition system does not significantly deteriorate S/D dopant distribution in the transistor itself.

Interface-state D_{it} characterization by high–low C-V measurement.— As predicted by Matthiessen's rule in Eq. 4,[26] there are several key factors that contribute to the carrier transport mobility variation. The interface state is a major factor influencing inversion channel electron mobility, in which the maximum mobility depends on the interface-state density

$$\frac{1}{\mu_{\text{effective}}} = \frac{1}{\mu_{\text{lattice}}} + \frac{1}{\mu_{\text{impurity}}} + \frac{1}{\mu_{\text{Dit}}} + \frac{1}{\mu_{\text{surface_roughness}}} \quad [4]$$

Therefore, the high–low C-V technique[27] is utilized to characterize the density of interface traps D_{it}. The measured D_{it} results in Fig. 9 indicate that the interface quality deteriorated with LT-SiN when the trap energy range ($E_C - E$) is greater than 0.25 eV, where E_C is the energy of the conduction band edge and E is the interface-state energy. At the same time, the LT-SiN and HT-SiN SMT processes have comparable T_{ox} values, extracted from C-V analyses, and similar threshold voltage values, as previously shown in Fig. 7. As the MOSFET parameters are related through interface states and oxide traps near the interface, the increased interface trap D_{it} generated at the oxide/silicon substrate interface under inversion mode, as shown in Fig. 9, can lead to the reduced transconductance in Fig. 5 and the lowered electron mobility in Fig. 6. Therefore, to further improve the nFET device performance, the SMT process should be optimized with respect to these parameters.

Relevance of SiN film properties on electrical measurement results.— As shown in Fig. 9, when the double-sided HT-SiN was utilized as the SMT capping layer, it reduced the density of interface states. Hence, both the nFET transconductance in Fig. 5 and the electron mobility in Fig. 6 were improved. Thus, interfacial quality degradation must be considered with the adoption of advanced nitride films in pursuing performance gain for SMT technology.

Intrinsic stress results from the microstructure created in thin films when the atoms of these thin films are deposited on the substrate via various kinds of deposition tool and processes. Thus, the thin film's formation process environment, deposition rate, and impurities determine the sign and magnitude of the residual stress in the silicon substrate and, more specifically, in the silicon devices fabricated. As the LT-SiN is formed by a PECVD technique at a low temperature, it incorporates a higher hydrogen concentration compared to HT-SiN.[13,14] The resulting LT-SiN nitride layer has substantially higher Si–H and N–H bonding concentrations compared with an HT-SiN nitride layer formed at a high temperature, resulting in a larger stress increase after annealing.[14] Moreover, the higher temperature condition in a furnace system used to fabricate HT-SiN can help to passivate the dangling bonds at the interface. Thus, a lower D_{it} level can be achieved by HT-SiN compared to that formed by LT-SiN.

From the physical property point of view, the HT-SiN nitride is thermally stable because the layer is formed with less hydrogen bonding, as evidenced in Fig. 3b, exhibits little thermal stress variation, as shown in Table II, and shows lower thickness shrinkage upon annealing, as shown in Table I. At the same time, HT-SiN is deposited on both the front and back sides of the wafer, and thus the stress changes from the two sides of the wafer cancel each other out. Therefore, wafer bowing can also be suppressed, with less curvature induced after S/D RTA, as shown in Fig. 4. Such unique physical properties prevent the cracking phenomena and reduce the stress applied to the underlying layer, and less gate edge damage during the SMT formation process can be expected, as illustrated in Fig. 10.

Moreover, from the chemical property point of view, the formation of N–H bonds is more desirable than that of Si–H bonds as less hydrogen atoms evolved from the higher temperature nitride upon thermal annealing. This is because the bonding strength of N–H (4.7 eV) is larger than that of Si–H (3.9 eV),[28] and Si–H is more likely to release hydrogen after bond breakage compared to a N–H bond. In this respect, Yamamura et al. also confirmed that their novel strained CESL SiN, with a reduced amount of unstable Si–H bonds and incorporating more stable N–H bonds, is able to improve gate oxide interface quality and NBTI performance.[29]

It has been reported that excess released hydrogen can lead to

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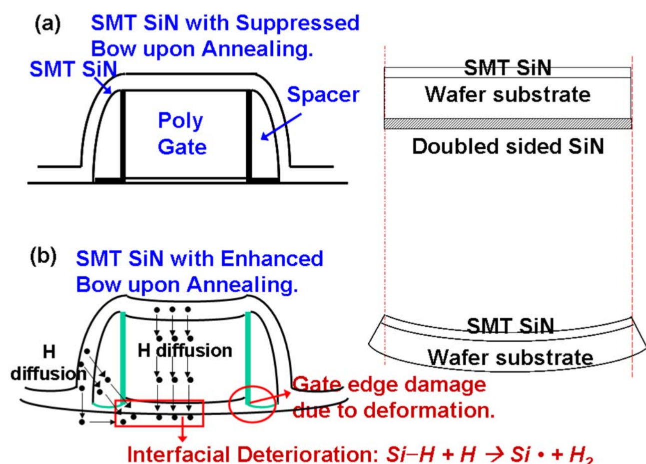

Figure 10. (Color online) (a) Top and (b) bottom. Schematic illustration of wafer bending inducing gate edge damage and interfacial quality deterioration due to high stress change in the SMT capping nitride in (b).

Si/SiO_2 interface quality degradation D_{it}.[30-33] Hydrogen plays a crucial role in the fabrication of high quality Si/SiO_2 interfaces in MOSFET electronic devices in that the interface-state buildup at the device's substrate/oxide interface is highly related to the transport of atomic hydrogen during its fabrication, and suppression of hydrogen transport aids in improving the electrical integrity of devices.[30,31] Because hydrogen is always present in the oxides of these transistors, the interface is unavoidably exposed to the hydrogen depassivation process. As hydrogen atoms impinge on the $Si(111)/SiO_2$ interface to depassivate the Si–H bond, the dangling Si bond and resulting interface traps can thus be formed via the chemical reaction in Eq. 5 shown below[32,33]

$$Si - H + H \rightarrow Si \bullet + H_2 \quad [5]$$

For the SMT application here, the hydrogen concentration evolved from the SMT nitride can also influence the interface quality. Because the HT-SiN film incorporates less hydrogen and creates fewer Si–H bonds, it is much more compositionally stable. Less hydrogen is released upon annealing, as shown by the FTIR spectra in Fig. 3b, and less interfacial degradation is obtained (Fig. 9). The mechanism responsible for this improvement is illustrated schematically in Fig. 10a. On the contrary, LT-SiN involves large quantities of hydrogen, which will be released upon annealing, as confirmed by the FTIR in Fig. 3a. Because the gate oxide quality at the gate edge has already been weakened by the mechanical stress exerted by the wafer bow due to the LT-SiN film's stress increase upon thermal annealing, as illustrated in Fig. 10b, the interface is especially vulnerable to hydrogen attack with hydrogen diffusion paths though the poly gate, spacer, and S/D region (Fig. 10b), resulting in a higher D_{it} level (Fig. 9).

Conclusion

In this paper, the SMT strain silicon technique has been experimentally studied for two different nitride films with respect to film stress, wafer curvature, nFET device performance, transconductance, and mobility. Moreover, the influence of interface states on the characteristics of nFET devices and the associated electron mobility behavior with these two different kinds of capping nitrides have also been quantitatively analyzed.

In this study, nFET V_t and DIBL have a similar level when using HT-SiN or LT-SiN for SMT application. Nevertheless, nFET devices with higher device performance, carrier mobility, and lowered interface-state density can be fabricated by the HT-SiN as the SMT capping nitride. The lowered D_{it} level achieved by HT-SiN as the SMT capping nitride is likely because (*i*) HT-SiN has less hydrogen in nitride itself, (*ii*) HT-SiN is more thermally stable with low thickness shrinkage and its stress is stable upon S/D annealing, and thus (*iii*) less wafer curvature is induced to suppress gate edge damage.

It is generally but not always true that a higher stress film deposited onto the transistor can produce a high mobility channel, nor is it always guaranteed that an improved device performance can be obtained with such a higher film stress when adopting strain silicon technology. This is because that excess force may lead to stress relaxation, permanent wafer deformation, or transistor structural damage. Furthermore, interface-state degradation must be balanced with the adoption of advanced nitride films for SMT in pursuing further nFET performance gain.

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