Journal of The Electrochemical Society, **157** (2) J29-J33 (2010)
0013-4651/2009/157(2)/J29/5/$28.00 © The Electrochemical Society

Degradation of Low Temperature Polycrystalline Silicon Thin Film Transistors under Negative Bias Temperature Instability Stress with Illumination Effect

Chia-Sheng Lin,[a] Ying-Chung Chen,[a] Ting-Chang Chang,[b,c,d,*,z] Hung-Wei Li,[e] Wei-Che Hsu,[b] Shih-Ching Chen,[b] Ya-Hsiang Tai,[f] Fu-Yen Jian,[c] Te-Chih Chen,[b] Kuan-Jen Tu,[b] Hsing-Hua Wu,[f,g] and Yi-Chan Chen[g]

[a]*Department of Electrical Engineering,* [b]*Department of Physics,* [c]*Institute of Electro-Optical Engineering, and* [d]*Center for Nanoscience and Nanotechnology, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[e]*Department of Photonics and Institute of Electro-Optical Engineering, and* [f]*Department of Photonics and Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan*
[g]*Photovoltaics Technology Center, Industrial Technology Research Institute, Chutung, Hsinchu, Taiwan*

This work investigates negative bias temperature instability (NBTI) in low temperature polycrystalline silicon thin film transistors (LTPS TFTs) in a darkened and in an illuminated environment of different light intensities. Experimental results reveal that the generations of interface state density (N_{it}) are identical under various illuminated intensity NBTI stresses. Nevertheless, the degradation of the grain boundary trap (N_{trap}) under illumination was more significant than that for the darkened environment, with degradation increasing as illumination intensity increases. This phenomenon is mainly caused by the extra number of holes generated during the illuminated NBTI stress. The increased N_{trap} degradation leads to an increase in the darkened environment leakage current. This indicates that more traps are generated in the drain junction region than from carrier tunneling via the trap, resulting in leakage current. Conversely, an increase in N_{trap} degradation results in a decrease in the photoleakage current. This indicates that the number of recombination centers increases in the poly-Si bulk, affecting photosensitivity in LTPS TFTs.
© 2009 The Electrochemical Society. [DOI: 10.1149/1.3265456] All rights reserved.

Manuscript submitted March 26, 2009; revised manuscript received October 26, 2009. Published December 17, 2009.

Low temperature polycrystalline silicon thin film transistors (LTPS TFTs) have been widely investigated for flat-panel applications, such as for active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diodes.[1-3] Compared to amorphous silicon (a-Si) TFTs, LTPS TFTs have a higher electron mobility and driving current. Consequently, the LTPS TFTs can integrate both the pixel array and peripheral circuits on the same glass substrate to realize a system-on-panel (SOP) display.[4,5] Because driving circuits for LTPS TFTs are designed using the complementary metal oxide semiconductor inverter structure, the reliability of the p-channel LTPS TFTs [understood by such measurements as negative bias temperature instability (NBTI)] has been an important problem and has been widely investigated and discussed. Previous studies, however, have investigated NBTI only in darkened environments[6-8] although LTPS TFTs are usually operated in illuminated environments on AMLCDs or SOP displays. Therefore, NBTI under illumination is an important issue for predicting LTPS TFT degradation. Both the illumination effect in LTPS TFTs [9,10] as well as the reliability of a-Si TFTs under illumination have previously been studied.[11] However, NBTI degradation in p-channel LTPS TFTs under illumination has not been adequately clarified.

This work studies the NBTI effect of p-channel LTPS TFTs under various illumination intensities and temperatures. By analyzing the interface state density (N_{it}) and the grain boundary trap density (N_{trap}) after NBTI stresses, the results indicated that only the generation of N_{trap} after illuminated NBTI stress is more pronounced due to the excess light-induced holes. The darkened leakage and the photoleakage currents after different NBTI stresses were also investigated.

Experimental

The p-channel LTPS TFTs were fabricated on a glass substrate with top-gate structures. First, a 500 nm thick buffer oxide was deposited on the glass. Next, a 50 nm a-Si film was deposited by plasma enhanced chemical vapor deposition (PECVD) on the buffer oxide. Then, an a-Si–H film was crystallized by excimer laser annealing at room temperature. The average grain size was 2 μm. An 80 nm gate oxide was deposited by PECVD, and 300 nm Mo was deposited as a gate metal by sputtering. After the source and drain region formations, NH_3 plasma treatment was utilized at 300°C to passivate the dangling bonds at the poly-Si/SiO_2 interface and at the grain boundaries. Finally, a 500 nm SiO_2 layer was deposited and identified as the interlayer dielectric layer. The TFTs studied in this work were 6 μm long and 10 μm wide.

During the stress operation, the device was stressed with a gate voltage of −25 V+ threshold voltage (V_{th}) for 1000 s under the darkened and the illuminated environments, while the source and drain were both grounded. This stress operation was run at 70, 100, 125, and 150°C. The light was from the halogen lamp illumination introduced through the objective of a microscope and focused onto the device. The reflected light also reached the active layer via the Al thin film deposited atop the Si wafer that carries the device. For illuminated NBTI stresses, the photo intensities were set at 190 and 400 lx. During the measurement subsequent to the stress condition, all measurements were performed under darkened conditions with a gate voltage swing from 5 to −10 V, with the drain voltage set to −0.1 and −10 V. The threshold voltage was extracted from the tangent slope of the normalized drain current (linear region) vs the gate voltage in the linear scale at the transconductance maximum ($G_{m,max}$).

Results and Discussion

Figure 1a and b shows the I_d-V_g transfer characteristics when the device operates in the linear region for the LTPS TFT at the initial condition and (a) after NBTI stress under darkened conditions and (b) after NBTI stress under 400 lx illumination intensity. The normalized I_D is defined as $I_D/(W/L)$. It is clear from these figures that the subthreshold swing, the transconductance, and the on-current have degraded for both the darkened and illuminated NBTI stress conditions. V_{th} shifts to the negative direction under both NBTI stresses. The threshold voltage (V_{th}) shift of the TFT is caused by charge trapping or defect creation in the gate oxide. Such V_{th} shift caused by charge trapping requires a high electric field across the gate oxide (above 6 MV/cm).[6] In this experiment, the electric field across the gate dielectric (about 3 MV/cm) is not high enough to cause hole injection. These experimental results are similar to pre-

* Electrochemical Society Active Member.
[z] E-mail: tcchang@mail.phys.nsysu.edu.tw

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

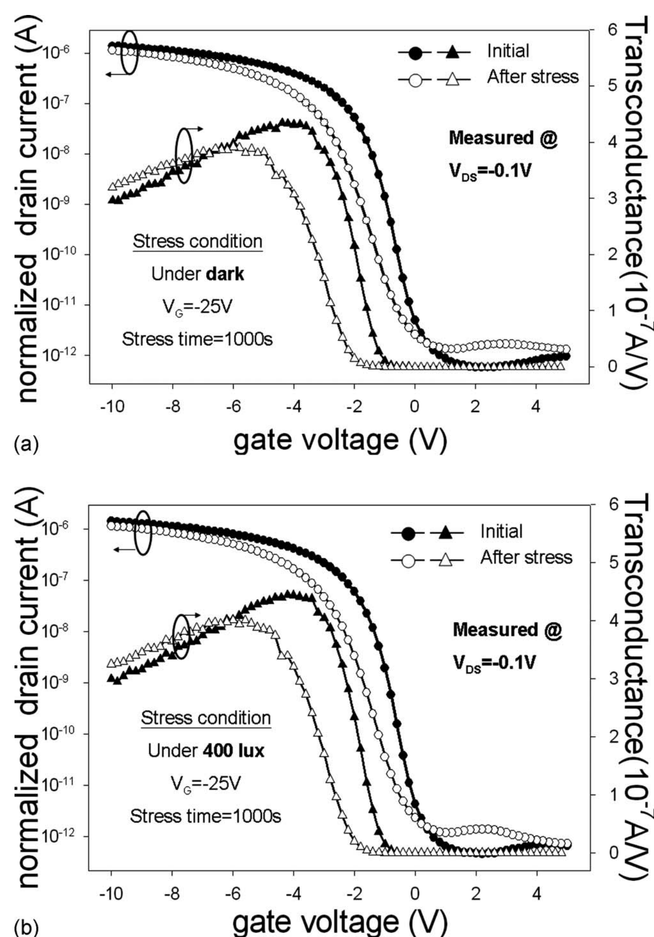

Figure 1. I_d-V_g transfer characteristics in the linear region of the LTPS TFT at 125°C under initial NBTI stress and after (a) darkened and (b) 400 lx NBTI stresses.

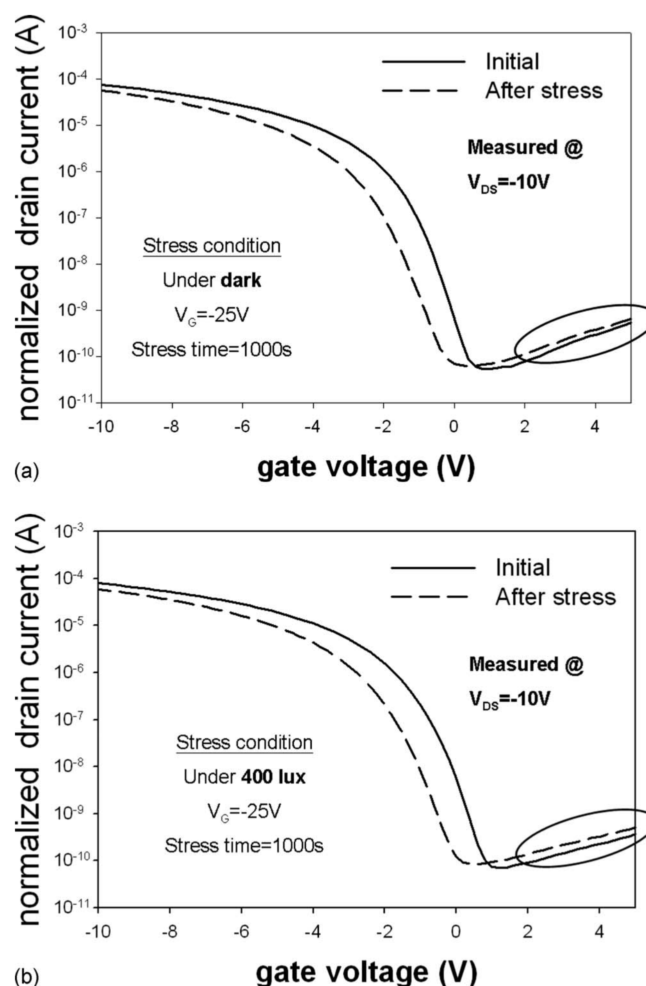

Figure 2. I_d-V_g transfer characteristics in the saturation region of the LTPS TFT at 125°C under initial NBTI stress and after (a) darkened and (b) 400 lx NBTI stresses.

vious studies for LTPS TFTs.[6,7] This indicates that interface states and grain boundary traps were generated during NBTI stress.

Figure 2a and b shows the I_d-V_g transfer characteristics when the device is operated in the saturation region for the LTPS TFT at an initial condition and (a) after darkened NBTI stress and (b) after illuminated NBTI stress at 400 lx intensity. The circled area indicates a clear increase in the leakage current after both the darkened and illuminated NBTI stresses. The variations in leakage current are about 19 and 38% under darkened and 400 lx NBTI, respectively, measured at $V_{gs} = 5$ V and $V_{ds} = -10$ V. In polysilicon (poly-Si) TFTs, the leakage current is principally caused by trap-assisted tunneling at the drain junction.[12] The experimental results indicate that increased leakage current after both darkened and illuminated stresses is due to the degradation of the grain boundary traps.

Figure 3 shows the negative shift of the threshold voltage ($-\Delta V_{th}$) with stress time under the darkened and 400 lx illuminated intensity NBTI stresses. $-\Delta V_{th}$ increases with an increase in stress time, which displays power law dependence. The exponent factor n can be extracted by the power law relationship, $\Delta V_{th} = At^n$,[13] where n is 0.36 both under the darkened and the 400 lx NBTI stresses. These results indicate that the diffusion-controlled electrochemical reaction is the principal degradation mechanism for both the darkened and the 400 lx NBTI stresses.[14]

Figure 4 shows the variation in V_{th} during repeated stress/recovery periods under darkened and illuminated environments at 125°C. The gate voltage was switched from −25 to 0 V, and the source/drain were also grounded in the recovery periods. As can clearly be seen in both stresses, the threshold voltage shifts were reduced as the gate voltage was switched to 0 V. This result can be explained by the passivation of the interface traps by the absorption of hydrogen at dangling bond sites. When the channel inversion

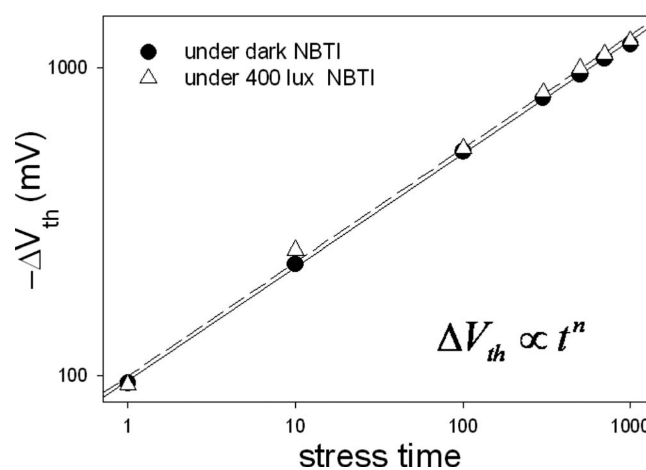

Figure 3. Relationship between negative threshold voltage shift and stress time.

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

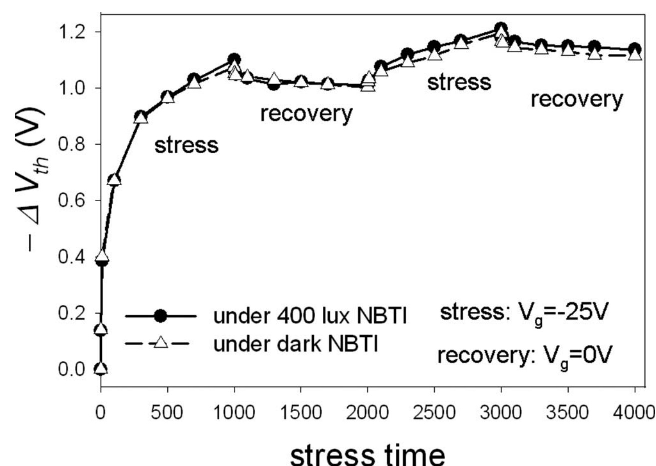

Figure 4. Variation in V_{th} during repeated stress/recovery periods under darkened and illuminated stresses.

layer disappeared, the hydrogen species moved back to the interface between SiO_2 and poly-Si and further passivated the Si dangling bonds, decreasing the V_{th} shift.[15,16]

Because the differences between the darkened and illuminated NBTI stresses are not readily apparent in Fig. 1 and 2, the generation of the interface state density (N_{it}) and the grain boundary traps (N_{trap}) for both stress conditions can be analyzed to better understand the influence of illumination. In general, N_{it} can be extracted from the subthreshold swing by ignoring the depletion capacitance in the active layer according to the following equation.[17] The N_{it} trap increase occurs not only at the SiO_2/poly-Si interface, but also in the grain boundary in the weak inversion region. The subthreshold swing is defined as one-half of the gate voltage required to increase the threshold drain current by 2 orders of magnitude (from 10^{-11} to 10^{-9} A)

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right) \qquad [1]$$

Because the degradation and NBTI stress are strongly related to stress temperature, both the darkened and 400 lx illumination intensity stress temperatures were varied in a range from 75 to 150°C. The correlation between the increase in N_{it} and the stress temperature is illustrated in Fig. 5, where the N_{it} increase is defined as

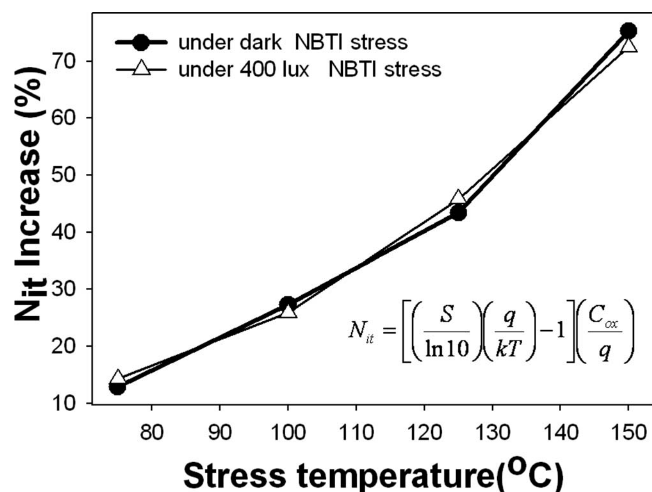

Figure 5. Relationship between N_{it} increase and different stress temperatures.

$[(N_{it_stress} - N_{it_initial})/N_{it_initial}] \times 100\%$. Clearly, the increase in N_{it} after NBTI exhibits no difference between the darkened and 400 lx illuminated intensity environments, which suggests that it is not strongly dependent on the extra holes generated under illumination.

N_{trap} can be estimated by the Levinson and Proano method,[4,17] shown in the inset in Fig. 6. N_{trap} is a concentration of traps located at the grain boundaries when the energy band bends from flatband (FB) to inversion and the concentration includes N_{it}. Figure 6 shows the generation of the grain boundary trap states (N_{trap}) at various stress temperatures under both NBTI stresses. The generation of N_{trap} is defined as $[(N_{trap_stress} - N_{trap_initial})/N_{trap_initial}] \times 100\%$. The inset shows the plots of $\ln [I_{ds}/(V_{gs} - V_{FB})]$ vs $1/(V_{gs} - V_{FB})^2$ curves, where the FB voltage is defined as the gate voltage that yields the minimum drain–current from the transfer characteristic with $V_{ds} = -0.1$ V. The N_{trap} can be determined from the square root of the slope

$$N_{trap} = \left(\frac{C_{ox}}{q}\right)\sqrt{|\text{slope}|} \qquad [2]$$

As can be seen in the figure, the N_{trap} increase under 400 lx illuminated intensity NBTI stress is more pronounced than that for the darkened NBTI stress. This is because more grain boundary trap states are created by the extra hole during the illumination stress.

Figure 7 shows the relationships between the N_{it} increase and the $-V_{th}$ shift under different illumination intensities for an NBTI stress

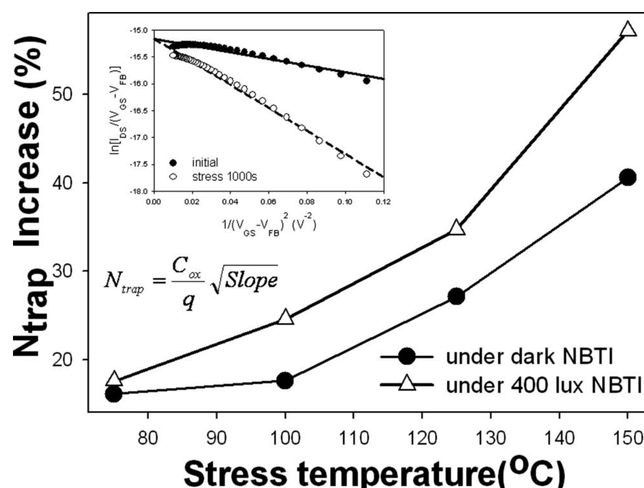

Figure 6. Relationship between N_{trap} increase and different stress temperatures.

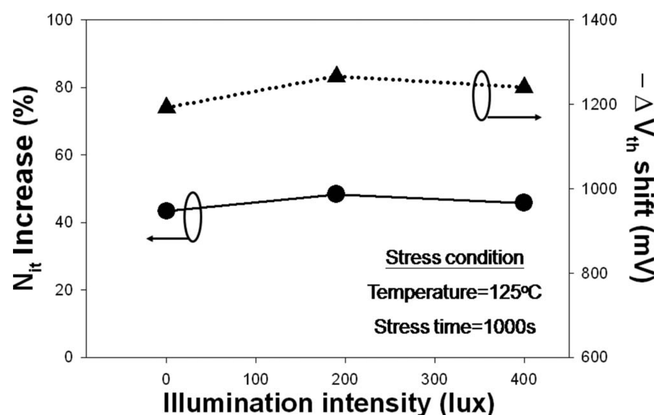

Figure 7. Relationship between N_{it} increase, negative threshold voltage shift, and illumination intensity.

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

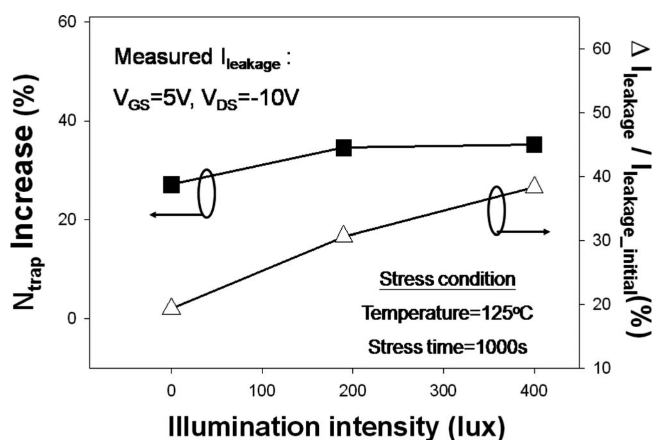

Figure 8. Relationship between N_{trap} increase, change in leakage current, and illumination intensity.

of 1000 s at 125°C. It is clear that the N_{it} increase is not a function of the illumination intensity. We know from Eq. 1 that the definition of the N_{it} increase includes both the traps at the SiO_2/poly-Si interface and those at the weak inversion region. In poly-Si TFTs, to achieve V_{th}, the traps must be filled at both the SiO_2/poly-Si interface and at the partial poly-Si bulk. Therefore, the V_{th} shift is dominated by the N_{it} increase.

Figure 8 shows the relationship between the N_{trap} increase, the change in leakage current, and the illumination intensity for the NBTI stress of 1000 s at 125°C. The leakage current was measured at $V_{gs} = 5$ V and $V_{ds} = -10$ V in the off region under the dark environment. It can be seen that the leakage current and N_{trap} increased with increasing illumination intensity. The N_{trap} increase is related to the number of photoinduced carriers during illumination. Further, the increase in N_{trap} causes the leakage current to increase due to trap-assisted tunneling in the drain depletion region.

Figure 9a shows the schematic diagram of the device during the darkened NBTI stress. As the negative gate bias is applied, the inversion hole at the poly-Si/SiO_2 interface reacts with Si–H, resulting in the H dissociation and the generation of dangling bonds from the Si atoms. Furthermore, the dissociated H species can diffuse into the gate oxide and react with the oxygen of SiO_2 to form many OH groups bonded to Si atoms and Si dangling bonds.[18] Finally, the Si dangling bonds become the positive fixed oxide charges in the gate oxide and cause the V_{th} shift. The Si dangling bonds generated at the poly-Si/SiO_2 interface also degrade the subthreshold swing and on-current. Figure 9b shows the schematic diagram of the device during the illuminated NBTI stress, with the inset showing the power spectrum of the light source. Similar to the darkened stress condition, there is a formation of inversion holes between the poly-Si and the gate oxide; this is reflected in nearly identical values for N_{it}. Such N_{it} increase is related to the hole concentration at the Si–SiO_2 interface under the same electric field and stress temperature. The order of the hole current when the device is operated in the turn-on condition (i.e., $V_{gs} = -25$ V) is about 10^{-6} A/cm^2 in both the darkened and illuminated environments. However, the order of light-induced leakage current is only about 10^{-11} A/cm^2 (observed in the off-state region). This result implies that inversion hole concentration at the interface is much higher than light-induced hole concentration. Thus, the N_{it} increase is not sensitive to the extra holes from the illumination. The light-induced electron–hole pairs are also generated in the poly-Si bulk, a fact reflected in the difference between N_{trap}. In poly-Si TFTs, however, there are many grain boundaries in the channel regions, and the passivated Si–H bonds in grain boundaries degrade under NBTI stress. During illuminated NBTI stress, the light-induced holes react with the Si–H bonds in the grain boundaries, causing a more significant N_{trap} increase and leakage

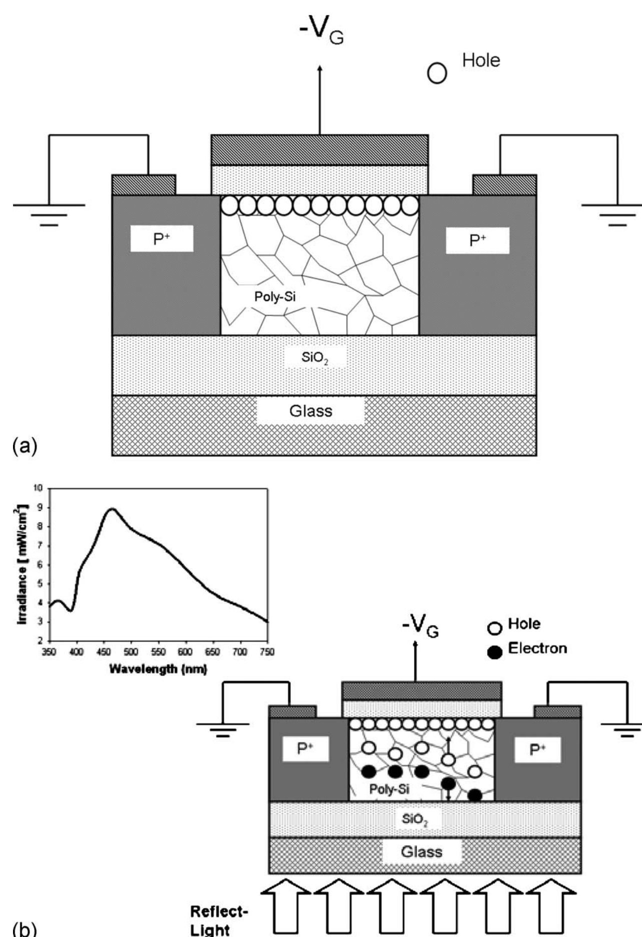

Figure 9. Schematic diagrams of LTPS TFT cross section with inversion and light-induced charges under (a) darkened and (b) illuminated NBTI stresses.

current degradation. Moreover, the difference in the N_{trap} increase between the darkened and the illuminated NBTI is more distinct at higher temperatures.

The N_{trap} increase is related to the photocurrent when the device is operated at the off-state region. Figure 10 shows the I_d-V_g transfer

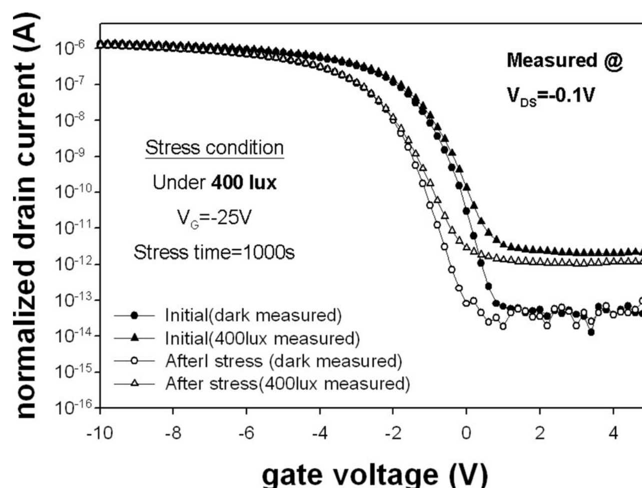

Figure 10. I_d-V_g transfer characteristics in the linear region of the initial and stressed LTPS TFTs measured in dark and 400 lx illumination environments at 30°C.

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

characteristic of TFTs with the −0.1 V drain voltage under all four conditions: initially unstressed, measured in both dark and 400 lx illumination environments and after 400 lx NBTI stress, and measured in both dark and 400 lx illumination environments. The leakage current in the TFT in the dark was about 10^{-14} A as the gate bias was swept from 5 to 0 V. Within the same range of the gate bias, the leakage current under the 400 lx was as high as 2 orders of magnitude, about 10^{-12} A. However, it can be clearly observed that the photoleakage current after an illumination stress was lower than that for the initial one. This is because the increase in N_{trap} actually functions to increase the number and availability of recombination sites.[19]

Conclusion

In this work, the NBTI in p-type poly-Si TFTs under darkened and illuminated conditions was investigated. Degradation occurred in the threshold voltage, subthreshold swing, and on-current for both NBTI stresses. For both darkened and illuminated stresses, the N_{it} increase and threshold voltage shifts are similar due to the inversion hole-induced H dissociation at the interface. Nevertheless, during the radiant illumination NBTI stress, the generation of extra holes in the poly-Si bulk causes the degradation of N_{trap} to be greater than that during the darkened NBTI stress. Further, the N_{trap} degradation serves to increase the leakage current and to reduce the photoleakage current.

Acknowledgments

The work was supported by the National Science Council under contract no. NSC-97-3114-M-110-001 and no. 97-2112-M-110-009-MY3. The authors thank Chi Mei Optoelectronics (CMO) for their technical support.

National Sun Yat-Sen University assisted in meeting the publication costs of this article.

References

1. H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, *Tech. Dig. - Int. Electron Devices Meet.*, **1991**, 563.
2. W. B. Tam and T. Shimoda, *SID Int. Symp. Digest Tech. Papers*, **2004**, 1406.
3. Y. Matsueda, R. Kakkad, Y. S. Park, H. H. Yoon, W. P. Lee, J. B. Koo, and H. K. Chung, *SID Int. Symp. Digest Tech. Papers*, **2004**, 1116.
4. K. Yoneda, R. Yokoyama, and T. Yamada, in *Proceedings of the International Symposium on VLSI Circuits*, p. 85 (2001).
5. H. Tokioka, M. Agari, M. Inoue, T. Yamamoto, H. Murai, and H. Nagata, in *Proceedings of SID*, Society for Information Display, p. 280 (2001).
6. C.-Y. Chen, J.-W. Lee, S.-D. Wang, M.-S. Shieh, P.-H. Lee, W.-C. Chen, H.-Y. Lin, K.-L. Yeh, and T.-F. Lei, *IEEE Trans. Electron Devices*, **53**, 2993 (2006).
7. S. Maeda, S. Maegawa, T. Ipposhi, H. Nishimura, T. Ichiki, J. Mitsuhashi, M. Ashida, T. Muragishi, Y. Lnoue, and T. Nishimura, *J. Appl. Phys.*, **76**, 15 (1994).
8. J.-C. Liao, Y.-K. Fang, C.-H. Kao, and C.-Y. Cheng, *IEEE Electron Device Lett.*, **29**, 477 (2008).
9. K. Suzuki, F. Takeuchi, Y. Ebiko, M. Chida, and N. Sasaki, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 785.
10. J. R. Ayres, S. D. Brotherton, I. R. Clarence, and P. J. Dobson, *IEE Proc.: Circuits Devices Syst.*, **141**, 27 (1994).
11. C.-Y. Huang, T.-H. Teng, C.-J. Yang, C.-H. Tseng, and H.-C. Cheng, *Jpn. J. Appl. Phys., Part 2*, **40**, L316 (2001).
12. P. Migliorato, C. Reita, and G. Tallarida, *Solid-State Electron.*, **38**, 2075 (1995).
13. A. T. Krishnan, V. Reddy, and S. Krishnan, *Tech. Dig. - Int. Electron Devices Meet.*, **2001**, 865.
14. S. Ogawa and N. Shiono, *Phys. Rev. B*, **51**, 4218 (1995).
15. C. T. Sah, J. Y. C. Sun, and J. J. T. Tzou, *J. Appl. Phys.*, **54**, 5864 (1983).
16. M. A. Alam, *Tech. Dig. - Int. Electron Devices Meet.*, **2003**, 345.
17. C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitriou, and N. Economou, *IEEE Trans. Electron Devices*, **39**, 598 (1992).
18. E. Proano, R. S. Misage, and D. G. Ast, *IEEE Trans. Electron Devices*, **36**, 1915 (1989).
19. Y.-H. Tai, Y.-F. Kuo, and Y.-H. Lee, *IEEE Electron Device Lett.*, **29**, 1322 (2008).

Downloaded on 2014-04-24 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).