低介電常數材料之研究及其在深次微米金屬半導體積體電路之製程整合之研究

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摘要

隨著積體電路製作技術的大幅成長, 元件線寬持續縮減至深次微米, 具有高速' 高元件' 積集度低功率消耗及低成本之 ULSI 積體電路得以大量生產製造. 伴隨著元件尺寸縮減後, 後段金屬導線亦需跟隨著微型化且單一層導線已不敷使用, 必須建構多層內導線才得以全部連結, 除增加製造程序的複雜度外, 與元件微型化不同的是, 金屬導線傳輸的速度會隨尺寸之縮短而更遲緩, 衍生所謂電阻-電容時間延遲(RC delay time); 在內連線結構中, 使用低介電常數是一可行且克服此一問題的方法之一.

本論文主要探討以化學氣相沉積所生成之低介電質材料之性質及在製程整合之研究. 主要探討的低介電質材料包括: Fluorosilicate glass (FSG), Carbon-doped organo-silicate glass(OSG) 及 organo-fluorosilicate glass (OFSG); 此外, 當積體電路製程轉移至銅製程時, 需要有銅阻抗層以防止銅擴散至低介電材質; 然而由於銅阻抗層的介電常數極高且銅易氧化影響阻抗層的附著性, 因此, 低介電常數之銅阻抗層及製

程整合之控制在本論文中也加以研究.

低介電質薄膜 FSG 在製程整合最大挑戰為氟在鍍膜熱穩定性的問題. 實驗得知, 覆蓋一層富矽氧化層 (Silicon-rich oxide; SRO) 可有效的防止氟的擴散而造成製程上的問題. 同時;我們亦發現提高鍍膜的沉積溫度, 利用氮氣電漿 (PE-N_2) 對 FSG 薄膜表面處理及發展兩種不同沉積方式的 FSG 薄膜當作金屬介電絕緣層, 亦可增加製程整合之穩定性.

為有效降低內導線中之電容值, 化學氣相沉積之 Carbon-doped organo-silicate glass 介電質薄膜被導入成為新的介電絕緣層. 如何得到較低之介電常數及較高之機械性質為製程整合最大的課題. 此外, 在半導體製程中, 熱處理為不可避免的步驟, 因此高熱阻抗也為低介電材料必要之條件. 吾人發現不同的反應條件可改變沉積膜之結構, 以得到較佳的低介電材料性質;使用 Ar 氣體在沉積環境中當載氣時, 能有效提升鍍膜之電性及機械強度. 此外, 吾人亦利用 Diethoxymethylsiliane (DEMS) 來取代目前所用之反應前驅物 Trimethylsilane (3MS); 實驗結果顯示,在薄膜的性質及實際的製程整合結構中, DEMS-based 的低介電質沉積膜有較優良之電性性質,機械強度及熱穩定性,以及在製程整合中之優越性.此外,在此篇論文中也針對 DEMS-based 的低介電質沉積膜的性質,結構及最適化之沉積條件作一詳盡之探討.

由於上述所提之低介電質薄膜各有其優劣點, 因此吾人亦發展出一種新的介電質薄膜 organo-fluorosilicate glass. 係在 Carbon-doped organo silicate galss 沉積過程中加入含氟原子之氣體, 此氟原子可取代不穩定的有機團及改變介電質薄膜的化學結構, 因而提高了材料之機械性質, 穩定性及附著能力.

在銅嵌大馬士革結構中, 銅易氧化及擴散至低介電絕緣層中, 造成可靠度的問題, 因此, 銅阻抗層的性質及沉積前的前處理為製程整合最須考慮的要素. 實驗得知, 利用氨氣電漿 (NH_3) 前處理可有效還原銅氧化物, 最適化之前處理時間可得較佳之電性性質, 增加銅導體與鄰接鍍膜之附著性, 以及避免可靠度的失效. 此外, 為避免整體電容值的升高, 低介電材質的銅阻抗層也被提出來取代傳統之氮化矽 (SiN; k=7) 薄膜. 實驗結果顯示, 以3MS為前驅物所產生之碳氮化矽 (SiCN) 及碳氧化矽 (SiCO) 薄膜可有效降低介電常數至3-5, 此直數值與沉積溫度有關; 然而, 低溫所沉積的這兩種鍍膜有化學及熱穩定的問題, 因此, 沉積溫度需高於350^{o}C才能滿足為銅阻抗層之需求.

Study of Low-Dielectric-Constant Materials on Process Integration of beyond sub-micro MOS Integrated Circuits

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Abstract

As the device dimensions continue to shrink, interconnect delay becomes a limiting factor for increasing circuit device speed. Since interconnect delay is the product of the resistance in metal interconnect and the capacitance between the metal lines, the minimization of the parasitic capacitance and the resistance in interconnect is required. Incorporation of low-dielectric-constant materials in multilevel interconnect can effectively reduce parasitic capacitance, thus decreasing the transmission delay.

In this study, several kinds of low-dielectric-constant materials are investigated, including Fluorine-Silicate-Glass (FSG), carbon-doped organo-silicate glass using trimethylsilane (3MS) and Diethoxymethylsilane (DEMS) as precursors. Moreover, the effects of the low-dielectric-constant materials on the integration issue are studied to evaluate the compatibility of low-*k* materials on semiconductor process.

On the other hand, copper (Cu) barrier film is an indispensable layer in Cu dual-damascene fabrication. This layer can increase the effective interconnect capacitance because its dielectric constant can be as high as 7.0 (SiN film). Meanwhile, to prevent Cu from oxidation, which induces reliability fail, the plasma Cu oxide (Cu_xO) reduction is

performed before Cu barrier film deposition. As a result, this integration process control and varying low-dielectric barrier films evaluation were investigated in this work as well.

The SIMS data shows that using a cap layer can enhance the thermal stability of FSG and silicon-rich oxide (SRO) is superior to PE-OX in blocking the F diffusion at high temperature and moisture environment. A double interlayer of high-density plasma FSG and SRO have been developed to control fluorine instability for sub-0.18 μm device. On the other hand, the interconnect conditions need further study for robust integration. A higher FSG deposition temperature, PE-N_2 plasma treatment on FSG layer, and a stack of HDP-FSG and PE-FSG layer interconnect is proposed to prevent FSG bubble, Al delamination, and interconnect crack. HDP-FSG can fill the gap as small as 0.23 μm gap, which indicates that FSG can be used for the 0.18 μm processes. Moreover, FSG film with a higher deposition temperature can further fill the 0.21 μm gap, which use FSG in process less than 0.18 μm device. In 600Å USG/8000Å FSG/2,000Å SRO cap layered structure, HDP-FSG shows 7.45 to 7.7% line-to-line capacitance reduction and has similar via resistance to that of USG film.

Lower dielectric constant as well as higher mechanical strength of plasma enhanced chemical vapor deposition (PE-CVD) low-*k* films is required for circuit speed and package. Low-*k* films deposited by PE-CVD using 3MS and oxygen (O_2) precursors in Ar carrier gas exhibited the strongly improvement in deposition rate, non-uniformity, leakage current and hardness due to decreasing micro-porous. However, a bit scarification on dielectric constant of the deposited low-*k* films occurred. On the other hand, The DEMS-based low-*k* films had a lower dielectric constant, higher hardness and higher chemical and thermal stability than those of the 3MS-based films. From the

results of blanket films and four-level interconnect test devices, the DEMS-based films were found to have superior electrical performance than that of the 3MS-based films. Above results clearly reveal that the DEMS-based films are the promising low-*k* materials in the next technology generation.

Additionally, higher heat resistance is necessary to prevent degradation during the interconnect fabrication process. The films deposited from the DEMS precursor at higher temperatures show a lower amount of carbon component and a preference for monomethylated Si atoms relative to lower deposition temperatures and the higher cross-linking bonding due to CH_n bridging network, resulting in higher hardness strength and thermally stability. The electrical performance films from DEMS deposited at different temperatures in ILD test structures was provided similar results as blanket films, showing good electrical performance.

The composition, bonding configuration, optical, mechanical, electrical properties and thermal stability of SiCOH films using DEMS and O_2 as a precursor by PE-CVD method have been investigated in this work. The refractive index of SiCOH increases with increasing deposition temperature yet decreases with increasing oxygen addition to the deposition recipe. The addition of oxygen dramatically enhanced the plasma deposition rate of DEMS. The as-deposited films also show lower the dielectric constant and decreased mechanical hardness and modulus. The effect of which is reduced at higher temperatures. The results can be accounted for by the changes in composition and bonding configuration, as determined from FT-IR and elemental analyses. The low dielectric constant organo-silica-glass (OSG) films deposited by DEMS and O_2 is shown to be the most reliable: the dielectric constant are stable even after a heating test at 700^{o}C

and a pressure cooler test for 168 h, and superior to other PE-CVD low-*k* films deposited by other precursors. However, O_2 plasma ashing process lead to the dielectric degradation in deposited low-*k* films during photo-resist removal processing. The nitrogen plasma treatment is proposed to prevent the damage from oxygen attack on the low-*k* films deposited by DEMS.

A new low-*k* interlayer dielectric material, organofluorosilicate glass (OFSG), has been developed and characterized. The addition of silicon tetrafluoride to a trimethylsilane-based organosilicate glass deposition process provides chemical and structural changes to the deposited film that result in improved mechanical strength at comparable dielectric constants to their non-fluorinated analogs. The presence of SiF_4 in the plasma affects the replacement of more labile organic species with 2-3 atomic percent inorganic fluorine, providing enhanced material stability. The chemical and structural changes also result in enhanced adhesive strength and reduced residual stress and stress hysteresis. The resistance of OSG and OFSG films against heat and moisture stress test was investigated. Compared with OSG films, the OFSG films were shown to be having superior thermal stability and electrical properties. The enhanced degradation of the dielectric constant of OFSG films during moisture stress tests was attributed to the hydrolytic instability of Si-F bonds. Consequently, similar to fluorosilicate glass, moisture resistance of the OFSG film will require attention during integration of this material.

While various low-*k* (*k* ~3.0) materials have been extensively developed as the inter-layer dielectrics (ILDs), high dielectric constant (*k* ~7.0) silicon nitride (SiN) is still the primary candidate for the Cu capping barrier and etching stop layer required in the Cu

dual damascene structure. To further reduce the effective dielectric constant of the Cu interconnects system. In addition, Cu can be easily be oxidized when exposed to commonly used processing environments at low temperatures (<200^{o}C), and such oxidation could negatively impact component performance and reliability. Therefore, Cu oxide (Cu_xO) should be completely removed by reduction reaction through hydrogen-based plasma treatment to ensure superior conductivity of the Cu interconnects and to enhance the adhesion of SiN to the post Cu-CMP surface. NH_3 and H_2 plasma pre-treatments have been investigated as a method of removing the oxide from the Cu surface, to improve the adhesion of the PE-CVD barrier layer to post Cu-CMP surfaces. H_2 plasma treatment showed an excellent Cu_xO removal rate and had less impact on the low-dielectric ILD layer. A higher leakage current between Cu lines was the main drawback for this pre-treatment. Insufficient exposure to the NH_3 plasma pre-treatment leads to an increased occurrence probability of delamination at the Cu/SiN interface. Optimization of the NH_3 treatment time resulted in the reduction of the adhesion failures and a lower metal leakage current. In addition, excessive thermal time (pre-heating and treatment time) induces the Cu-hump problem, resulting in a reliability failure. A longer waiting time (>18 h) leads to delamination at the SiN/Cu surface, even after performing the NH_3 treatment. The post Cu-CMP clean seemed to effectively solve this issue, but increased the process complexity. Therefore, optimization of the process time prior to the Cu barrier layer deposition process is crucial for ensuring the performance of the Cu interconnects.

SiN and 3MS-based silicon carbide (SiCN and SiCO) films deposited by PE-CVD method have been comprehensively investigated by varying deposition temperature. The

important requirements for the Cu barrier layer were adequately considered in terms of these three films. Among these barrier films, PE-SiN films with varying deposition temperature (200-450^{o}C) still were the excellent option as Cu barrier layer film due to the possession of high barrier properties and integration capacitance. In addition, SiN film with low hydrogen content has a superior etch selectivity and a better electrical performance. However, the lethality of this film is higher dielectric constant, as high as 7.0.in the 200-450^{o}C deposition temperature. Therefore, much effort need to done to lower permittivity for the reduction of the parasitic capacitance. On the other hand, a 3MS-based barrier film, including SiCN and SiCO films, can reduce the dielectric constant to 3~5, depends on the deposition temperature. Although the film with lower deposition temperature can further reduce the dielectric constant, it suffers from the predicament of the thermal and chemical stability. As a result, the deposition temperature of the film must above 350^{o}C to improve its properties to have a good fit as Cu barrier layer.

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Contents

Chapter 1

Introduction

As interconnect feature size continues to decrease, the propagation delay (RC), crosstalk noise and power dissipation of the interconnects become limiting factors in ultra-large scale integration (ULSI) device performance [1]. Since RC delay is a product of the resistance in the metal interconnect (R) and the capacitance between the metal line (C), incorporating copper wiring and low dielectric constant (low-*k*) dielectric to replace the conventional AlCu/SiO_2 into interconnect technology can effectively reduce the RC delay [2].

Many low-*k* materials have been applied in ULSI metallization. The best low-*k* materials perform reliably upon integration with the manufacturing process, exhibiting high thermal stability to 425^{o}C, mechanical stability and compatibility with etching, stripping, cleaning and polishing processes [3].

The early winner of low dielectric constant materials, fluorosilicate glass (FSG), is currently being scaled into volume production. Especially, high-density plasma CVD (HDP-CVD) FSG attracts more attention since it can provide high aspect ratio gap-filling ability. However, like other FSG films deposited by other method or precursors, the suffering primary challenge of FSG films is fluorine stability [4,5].

Another concern of FSG low-*k* films is that the *k* value is not sufficient low (*k*=3.5-3.8), leading the reduction of the capacitance limited. To solve the above issue to meet the ITRS roadmap, several organic and inorganic materials had been proposed.

Organic materials have more integration issues than inorganic materials, such as thermal stability, poor adhesion, and low resistance to O_2 plasma. On the other hand, inorganic dielectric materials have better thermal and mechanical stability and film adhesion during process integration though they have still higher dielectric constant. Accordingly, films have organic and inorganic components are very promising as low-*k* dielectric materials with stable properties. The promising candidate materials with dielectric constant equal to 2.8-3.2 will likely to be organic carbon doped silicates (OSG). These materials contain Si-CH_3 groups as well as Si-O groups. Carbon's lower polarizability, in Si-CH_3 bonding helps to reduce the dielectric constant. Additionally, the presence of space-occupying alkyl groups in this film produces "free volumes" in the film, which also can reduce the dielectric constant [6,7].

To reduce the resistance and improve electromigration of the interconnects, Cu has the attracting material due to its lower electrical bulk resistivity of 1.6 and higher electromigration resistance compared to aluminum alloys. However, the use of the Cu will cause some integration challenges, such as poor adhesion to dielectric materials (SiO_2, polyimide), easily oxidized at 200^{o}C, and chemical corrosion. Therefore, the implementation of barrier layer between Cu and low-*k* film as Cu diffusion barrier and etching stop layer is required. Silicon nitride (SiN) is a primary candidate for the Cu barrier and etching stop layer required in the Cu damascene structure. However, a high dielectric constant of SiN films (*k*=7-8) was the key limiting factor of ULSI circuit performance. A number of low-*k* silicon carbide (SiC) films deposited by PE-CVD using organosilicate gases have been reported regarding the thermal stability and Cu-diffusion restrained [8].

Another concern is the Cu can be easily oxidized when exposed to commonly used processing environments at low temperatures (<200^{o}C), and such oxidation could negatively impact component performance and reliability [9]. Hydrogen-based plasma, such as NH_3 and H_2, was reported to generate H species to remove the Cu oxide formed on the Cu surface by oxidation-reaction reaction.

The work in this thesis was divided into eight chapters to discuss the low-*k* films and their integration issues in ULSI. The contents in each chapter are given as follow:

Chapter 1: Introduction of the motivation and organization of this thesis.

Chapter 2: Literature Review. General background of the low dielectric constant for the application in multilevel interconnect architecture is introduced.

Chapter 3: The experimental method and procedure, along with analysis technology are introduced.

Chapter 4: The characteristics of fluorine-doped silicate glass (FSG) are investigated. In addition, the integration of FSG into ULSI is also under discussion. An optimized FSG scheme for ULSI application is also proposed in this chapter.

Chapter 5: The characteristics of carbon-doped silicate glass (SiCOH) are investigated. Several carbon precursors under different process conditions are conducted. Furthermore, integration issues such as thermal stability, moisture resistance, and O_2 ashing effect are also studied.

Chapter 6: In this chapter, we developed the organofluorosilicate glass (OFSG) films of the composition Si:O:C:H:F, where essentially all fluorine is bonded to silicon, were deposited via plasma enhanced chemical vapor deposition (PE-CVD). The films with combination with advantages of FSG and SiCOH films are provided. This material provides superior electrical and mechanical properties, improved thermal and oxidative stability, and improved adhesive strength relative to non-fluorinated organosilicate glass (OSG) analogs produced from similar processes.

Chapter 7: Comparisons of different Cu-barrier layers are studied in this chapter. Additionally, optimized process of Cu-barrier films deposition was also discussed. Moreover, plasma treatment prior to Cu-barrier layer deposition, such as NH_3 and H_2 plasma treatment, are also compared to remove the Cu oxide.

Chapter 8: Summary of the contribution of this thesis and the plan of further work.

Chapter 2

Literature Review

2-1 Advanced interconnect scheme

As interconnect feature size continues to decrease below 200 nm, a variety of problems immerges such as the propagation delay (RC), crosstalk noise, and power dissipation by increasing chip power. The use of copper (Cu) should solve resistivity and electromigration issues but reliability concern with respect to an efficient diffusion barrier. Low-*k* dielectrics allowing capacitance reduction have low thermal conductivity and mechanical strength thus poor heat dissipation and package capability. Integration of Cu and low-*k* materials in damascene architecture are intensively under study worldwide [10].

The dimension of scaling of back-end interconnection results in the fact not only does the line-width and spacing between metal interconnects are made smaller, but also the length of the interconnect lines will increase. According to Figure 2-1, assuming the minimum metal pitch equals twice the metal width and the dielectric thickness is the same as that of the metal line in between. In a simple first-order model, RC time delay can be approximated as the Eqs.(2-3)

$$R = \rho (L_m/WH) \quad (2\text{-}1)$$

$$C = 2(C_L+C_v) = 2\varepsilon (L_mH/W + L_mW/H) \quad (2\text{-}2)$$

$$RC = 2\rho\varepsilon \left(L_m^2/W^2 + L_m^2/H^2 \right) \quad (2\text{-}3)$$

Where ρ is the resistivity of interconnect, L_m is the interconnect length, W is the interconnect width, ε is the permittivity of the dielectric, and H is the thickness of the metal.

Therefore, while the critical dimensions continue to shrink, the size reduction of space widths (W) and the length increase of interconnect line (L_m) will lead to a significant increase of the parasitic capacitance (C) and the metal line resistance (R). For this reason, a large portion of the total circuit propagation delay (RC delay) is dependant upon the characteristics of interconnects than on the scaling of active devices. In addition, since reducing cross-section of the interconnects area also causes higher conduction current density and leads to electromigration, changing the geometric structure of interconnection is not desirable to reduce interconnection delay. Thus, in order to reduce interconnect delay; using new materials for low resistivity (ρ) and low permittivity (ε) is in high demand to replace aluminum (Al) and silicon dioxide (SiO_2) of the conventional interconnection [11].

Recently, Cu has been introduced as the interconnect metal, replacing the conventional Al, to decrease the resistance due to its high conductivity [12,13], and low-dielectric-constant materials are proposed to reduce the parasitical capacitor for the interconnect application [14-16]. As compared with traditional Al/SiO_2 interconnects, the reduction in time delays with the Cu/low-*k* approach is shown in Figure 2-2. Moreover, the power dissipation can be calculated according to Eq. (2-4)

$$P \alpha 2\pi f V^2 C \quad (2\text{-}4)$$

Where *f* is the frequency of operation, V is the applied voltage, C is the capacitance. It is clearly shown that the power dissipation can be reduced by introducing low-*k* materials in the interconnect structure. As a result, the low-*k* material can lower line-to-line capacitance for reduction of signal propagation delay, reduce cross-talk noise in interconnects, and alleviate dissipation as well [17,18].

2-2 Gap-fill, Single and Dual Damascene Architecture

In traditional AlCu process, the AlCu was first etched using etch gas ($CF_4/O_2/N_2$). When metallization process migrate to Cu damascene or remain with Al processes, low-*k* requirements will differ (Figure 2-3). For example, high-aspect-ratio gap filling is crucial in the traditional scenario. Liner materials, deposited using PE-CVD or HDP-CVD, can be used to provide a moisture barrier, improve step coverage or enhance adhesion. In a Cu damascene structure, dielectric gap fill is no longer an issue, but the deposited dielectric is sufficiently thicker than ILD used in subtractive processes. Liner oxides may be required, and capping layers, which increase the mechanical stability of the dielectric during Cu CMP, typically are used. Silicon nitride or silicon carbide films are used frequently for dielectric etching stop and Cu barrier layer. The low-*k* dielectric must be compatible with tantalum (Ta), TaN and TiN barrier films [19, 20].

2-3 Low Dielectric Constant Materials

The Semiconductor Industry Association 2001 roadmap states that in the near term,

Fluorine-doped oxide and variety of low-*k* spin on dielectric are being qualified for production of the device with minimum feature sizes of 180 nm. However, a feature size below 130 nm, lower *k* material (*k*<2.7) will be required to counter the higher parasitic capacitance that accompanies smaller dimensions. These low-*k* materials are either organic or inorganic polymers. New spin-on materials, as well as a new CVD and vapor deposited films, offer potentially low-*k* solution [21-23].

With regard to the permittivity of low-*k* materials, it is well know that permittivity strongly depend on the frequency, as shown in Figure 2-4 [24]. In general, the dielectric constant has the form of

$$\varepsilon = 1 + \varepsilon_e + \varepsilon_a + \varepsilon_p \quad (2\text{-}5)$$

where ε_e, ε_a and ε_p corresponding to electric, atomic (ionic) and permanent dipolar contribution respectively to the dielectric constant. These contributions can be characterized by spectroscope, ellipsometry, infrared spectroscope and complex impedance measurements at frequencies from 100 Hz to 1 Hz [25]. The dielectric constant in the visible range (<=10^{16} Hz), in which the refractive index was measured consist of electronic polarization and is equal to the square of the refractive index [26]. In the infrared (<=10^{13} Hz), the dielectric constant is divided into two components: atomic and electronic polarization. However, when dielectric constant of dielectric constant measured at frequency of 1 Hz, the contribution of dielectric constant will mainly consist of electronic, atomic (ionic) and permanent dipolar polarization. Since the dielectric constant of different materials consist of different degree of polarization (electronic,

atomic (ionic) and permanent dipolar), the dielectric materials with lower polarization can possess lower dielectric constant.

2-4 Requirements and Leading candidates for low-*k* materials

Table 2-1 list the most promising candidates for the low-*k* interlevel dielectrics (ILDs), along with the key performance parameter. First winner is fluorinated silicon-oxide (FSG) delivering *k* of 3.5. For *k* below 3.0, organic polymers such as poly(arylene)ethers (PAE), benzoncyclobutene(BCB) and an aromatic hydrocarbon show promise, as do silicon-based CVD films. For ultralow-k (<2.0), feasible spin-on candidates include nanosilica films (*k*=1.3-2.5), porous polymers and polytetrafluoroethylene (*k*=1.9).

The best low-*k* dielectric material must meet at following criteria: (1) low permittivity, (2) high breakage voltage, (3) Low leakage current, (4) Thermal stability to >400^{o}C, (5) good adhesion to the metal and dielectric, (6) no metallic contamination, (7) no significant outgassing, (8) no moisture adsorption or excessive permeability to moisture. Besides these basic criteria, the low-*k* materials also should perform reliably upon integration with the manufacturing process, exhibiting high thermal stability, mechanical stability and compatibility with etching, stripping, cleaning and polishing processes [27] (Table 2-2).

As the minimum feature size in integrated circuits below 130 nm, high aspect ration structure will be required. Damascene and dual damascene architecture, in conjunction with copper metallization, involve etching a pattern in the dielectric, blanket deposited of

copper and subsequent planarization by etch back or chemical-mechanical polishing. Etching and filling these structures is a challenge because of the higher aspect ratio of this pattern. CMP is the dominant method of planarization and this process imposes an external force that the multiplayer structure must sustain. Therefore, the ILD must be compatible with Cu CMP [28].

The desired electrical properties of the future low-*k* materials, beside a low dielectric constant, low dissipation, high breakdown strength, high bulk resistivity and lower leakage. The lowest dielectric constant is desired, but must be trade-off with the mechanical and chemical property requirements imposed by integrating the dielectric with metal interconnects and incorporated of the barrier layer that might be need.

In copper process, copper needs a barrier layer to prevent from oxidation, corrosion, and diffusion into dielectric. On the other hand, this layer is also used as via/trench etch stop layer. Therefore, a barrier layer of Cu interconnect must satisfy several requirements including barrier, adhesion and high etch selectivity. Since barrier layers increase the effective k of ILDs of interconnect, this barrier layer must be as thin as possible while maintaining barrier properties [29].

2-5 Properties of FSG Films

2-5-1 Deposition Method:

A variety of deposition method to form FSG films has been developed. Plasma-enhanced chemical vapor deposition (PE-CVD) and atmospheric chemical vapor deposition (APCVD) processes have been extensively investigated [30, 31]. FSG

deposited by AP-CVD system below 450^{o}C show tensile stress and tend to absorb moisture that resulting in increasing dielectric constant and have integration problem in ULSIs. On the other hand, two plasma deposition processes, conventional plasma source and high density plasma source with bias rf, have been mainly to produce more stable FSG films and commonly use in current integrating ULSIs.

A number of gas source have also been investigated [32]. Fluorine precursor can be divided into two types. One type has pre-existing Si-F bonds, such as silicon tetrafluoride (SiF_4) or fluorotriethoxysilane (FTES) [33,34], and the other is a clean gas without Si-F bonds, such as NF_3, CF_4 or C_2F_6. The forming FSG films by the latter precursor absorbed more water than films deposited by the former source gas. SiF_4 and FTES have Si-F bonds and help in reducing the number of dangling or weakly bound fluorine atoms in the FSG films.

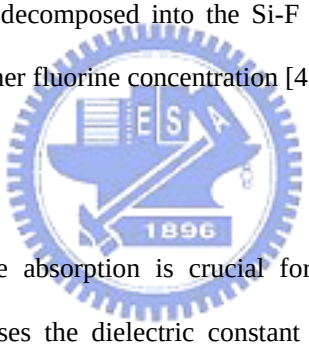
Generally speaking, precursors used commonly for the manufacture of ULSI are TEOS or SiH_4 in the presence of SiF_4 or FTES for the conventional PE-CVD technique [35,36], and SiH_4 in the presence of SiF_4 ($SiH_4/SiF_4/O_2/Ar$) for the HDP-CVD process [37, 38].

2-5-2 Infrared Spectra

The Si-F bonds absorption peak appear about 935 cm^{-1} in the infrared (IR) spectrum for FSG films by the addition of fluorine into silicon oxide films. Katsumate et al. [39] have suggested that the absorbance band of the Si-F bond was deconvoluted to three Gaussian bands and that that the development of the wave number feature on the 988 cm^{-1} absorption is indicative of the antisymmetric bond-stretching vibration of the Si-F_2

bonding group in the high fluorine concentration (>10 at. %). It was reported that Si-F_2 bonds reacted readily with moisture to form Si-OH bonds and result in corrosion in the metal wirings.

On the other hand, Lucovsky et al. [40] deny the existence of the Si-F_2 bonding group because there is no definitive IR spectroscopic evidence for the bonding around 935 cm^{-1} in the FSG films even fluorine concentration up to 12 at. %. Besides, the silicon monofluorine (Si-F) bond-stretching vibration (935 cm^{-1}) is approximately at the same frequency as the absorped-moisture vibration (920 cm^{-1}), since the similar equivalence of masses of F (19 amu) and OH (17 amu). As a result, it is difficult to conclude the absorption peak around 935 cm^{-1} is decomposed into the Si-F peak and the absorbed moisture peak for FSG films with higher fluorine concentration [41].



2-5-3 Moisture-Absorption

High resistance to the moisture absorption is crucial for choosing a dielectric material. Moisture absorption increases the dielectric constant of films, degrades the device performance and reduces the reliability. The main problem of FSG films is that Si-F bonds have a hygroscopic nature and not always very stable. Though higher fluorine concentration in the FSG film can reduce the dielectric constant, this FSG film readily absorbs moisture while stored in a clean room and results in a higher dielectric constant [42].

Miyajima et al. [43] have pointed out that ion bombardment, as well as gas-dissociation efficiency, is one of the key factors to obtain high resistance to moisture uptake. They have used TEOS/O_2/CF_4 gas to deposition FSG films by PE-CVD

technology, or helicon-wave- type HDP-CVD without rf biasing. They suggested that HDP produces ions such as O^+ and $O2^+$ with higher ion energy than PE-CVD, and these ions densify the Si-O network, reducing the carbon and hydrogen content.

Plasma gas treatment was also provided to improve the moisture resistance of FSG films. Takeishi et al. [44] have proposed an N_2O-plasma treatment to stabilize the FSG films. They found that this N_2O plasma treatment at 400^oC is effective to block moisture absorption. Although this treatment rarely increase the dielectric constant of FSG films, it also have improved the adhesion of the FSG films with the subsequent depositions of foreign passivation films, such as silicon nitride, silicon oxynitride, etc, in addition to blocking moisture absorption.

2-5-4 HDP-CVD FSG Film

Since voids formed in the 0.35 um wide spacing with the aspect ratios of more than 1.75 in the case of using PE-CVD FSG films, HDP-CVD method with radio frequency rf biasing attract more attention to deposit IMD films in ULSIs [45,46] because it can provide gap-filling capacity. In this technique, the deposition and physical sputter-etching processes are carried out simultaneously. This rf biased HDP-CVD method utilizes a dependency of an Ar sputter-etch rate upon an incidence angle. The rf power supplied to the substrate generates a large self-bias voltage that accelerates the ionized Ar atoms to the substrate effectively. The sputter rate at the corner of the interconnect is higher than on any other surface and this effect is contributed to good filling of the narrow gaps.

The schematic drawing of HDP-CVD chamber is shown in Figure 2-5. An inductively coupled plasma (ICP) was used to produce high-density plasma source. The

wafer needs effective cooling to maintain temperature and uniformity across it, because the bias rf power pulls the energetic ions out of the plasma and directs then at the wafer surface. The electro-static chuck (ESC) with a cooling liquid circulating through it was used in this equipment, and substrate temperature during the deposition was controlled by regulating the He pressure between the substrate backside and the ESC surface. The reaction gases used for this biased HDP-CVD FSG films are SiF_4, SiH_4, O_2 and Ar. The Fluorine concentration is mainly controlled by varying the ratio of SiF_4/SiH_4 ratio.

2-6 Carbon-doped Organic Silicate glass

As the feature size of very large scale integrated circuits continues to shrink and the density of devices on a chip increases, a material of particular importance identified by the Semiconductor Industry Association national technology roadmap is the low dielectric constant material (k<3) for interlevel isolation. A low-k dielectric is required for reducing power consumption in high frequency devices, reducing crosstalk between metallic interconnects, and reducing circuit RC time constants. The reduction in time constant is necessary for increasing speed and functionality on a chip.

Various organic and inorganic materials have been considered to replace PE-CVD deposited SiO_2, or FSG film for further reduction in dielectric constant.

There are many strategies to further reduce the dielectric constant. One strategy is to add alkyl groups to the silicon oxide based dielectric materials. Changing the component and connectivity of atomic constituents will also vary the dielectric constant and other properties such as the thermal stability.

Among the low-k candidates, the carbon-doped silicon oxide (SiCOH) film attracts

more attention and is highly suitable for ultra large-scale integrated applications because of the *k* value less than 3.0. SiCO films, which the silicon oxide incorporating terminating methyl (CH_3) groups in the oxide network can be considered a hybrid between organic and inorganic materials. The SiCOH films can potentially combine the advantages of both categories of materials [47-50].

2-6-1 Spin-on Deposition of low Dielectric Constant Materials

Spin-on deposition is one technique to deposit dielectric films for semiconductor fabrication. “Spin-on materials” is a material, in a liquid state, which can be deposited on a wafer by spin-coating method. Since spin-on material contain volatile solvent, an extra baking process is needed to perform to remove solvent from the as-spun film. Finally, the resultant sample is processing in furnace alloying to prepare excellent spin-on material. Generally speaking, spin-on materials have some advantages in IC fabrication, such as good local planarization capability, gap-filling capability, and low fabrication cost. Among various organic polymer such as fluorinated polyimide (FPI), poly arylene ether (PAE), benzocyclobutene (CBC), including SiLK and Flare, have been extensively investigated. [51-55]. These organic spin-on low-*k* materials have better thermal and mechanical stabilities than aliphatic polymers low-*k* materials, which results in the improvement of dimensional, compositional, and topographical integrity during continuous high-temperature thermal cycle. Moreover, most organic polymers low-*k* materials possess a superior characteristic of resistance to moisture uptake due to low content of polar molecules. Although these organic polymers have such more advantages, they suffer the most challenges in the compatibility of integration, such as etching

selectivity, manufacturability and chemical mechanical polishing (CMP) compatibility, because their material characteristics are completely different from that of SiO_2-based dielectrics.

There are another spin-on organosilicae glasses, such as methylsilsesquioxane (MSQ) and Hybrid-Organic-Siloxane-Polymer (HOSP), are the promising low-*k* materials [56, 57]. These films have been developed by increasing the number the methyl group, which decrease the film density and reduce film polarization, resulting in a low dielectric constant [58]. However, these film qualities are easily degraded due to oxygen plasma-induced damage and hydroscopic behavior in the duration of photo-resist stripping [59]. This chemical instability of MSQ or HOSP film is one of the major integration issues as it used as low-*k* ILDs materials.

2-6-2 Chemical Vapor Deposition of low Dielectric Constant Materials

Different from the spin-on technology, chemical deposition is the other technique to deposit dielectric films for ULSI fabrication. This method provides a simple procedure to produce the low-*k* film, which does not need the baking and furnace thermal process to remove solvent or impurities. Moreover, because of their thermal and mechanical stability, SiO_2-based, low-dielectric constant materials containing alkyl groups, deposited by PE-CVD method have attracted much attention recently [60,61]. Among these low-*k* materials, an organic and inorganic hybrid-type SiCOH film deposited by PE-CVD technology is wildly accepted as a promising candidate for low-*k* material application in the dual damascene copper interconnections because of its compatibility to conventional ULSI circuit processing. These low-*k* materials form the nanopores in the films by the

steric hindrance effect of alkyl groups as well as have the carbon's lower polarization in Si-CH_3 groups, which result in the decrease in dielectric constant [62]. Varieties of precursors have been developed to deposited low-*k* SiCOH films by CVD technology. Table 2-3 outlines the low-*k* materials precursors, tested, and their structure formulae [63]. The common precursors being used are trimethylsilane (3MS) and tetramethylsilane (4MS). The dielectric constant of these low-*k* films can reach as low as 2.6-3.0. Furthermore, these low-*k* films are useful as inter-metal dielectrics, and exhibit stability and electrical properties, which can meet many specifications in device fabrication [64]. However, the detailed chemical structure of the PE-CVD SiCOH films is still unclear because the chemical structure of the PE-CVD films is determined by the process precursors, process conditions (temperature, pressure, and gas flow) and plasma properties (radicals, ions, and their density and energy distribution).

On the other hand, there are a number of problems with using these low-*k* films as dielectrics, compared to SiO_2 or FSG. The modulus and hardness are much lower than for SiO_2, which can create problems during the fabrication and packaging [65,66]. In addition, the thermal conductivity is lower than that of SiO_2, so heating of interconnects will be greater than that for SiO_2 [67].

2-7 Copper CVD Barrier Layer

It is known that that Cu is a serious contamination source for both silicon and silicon dioxide. Therefore, copper rapidly diffuses into SiO_2 films during heat treatments in the fabrication process. The ULSI structures should be altered to prevent Cu diffusion. Full encapsulation of Cu lines with a metal barrier layer is one possible solution, however, the

first difficulty with full encapsulation is using metal barrier film even though the damascene structure is employed. The second is inconsistency between the two requirements of the reliability and electric performance because the resistance of Cu lines becomes intolerable large when the barrier film thickness exceeds about 20 nm. Therefore, novel barrier materials and their processes are current topic in Cu metallization [68,69].

Although the low-*k* films tend to garner all the intension in the low-*k* marketplace, it is the etch stop, barrier and CMP stop films that allow successful dual-damascene integration. The development of amorphous hydro-generated SiC films with a *k*=4-6 (depending on the deposition conditions) offers the combination of good adhesion to copper, mechanical strength and better reliability need to replace high-*k* (7-9) Si-N based barriers [70].

With Si-C based films, they tend to add small quantities of nitrogen or oxygen to reduce leakage in the films. Adding oxygen increase more challenging to get good selectivity between low-*k* and barrier films. As for add nitrogen, it exist the potential risk of photo-resist poisoning. Resist poisoning occurs when an amine molecule, such as activated nitrogen in plasma chamber, interacts with acidic components in chemically amplified resist to neutralize and prevent its dissolution in developer. Poisoning is addressed through a combination of hard masks and specific integration scheme.

Among the ancillary dielectric films, one of the most importances is the capping film over the copper line. It needs to perform Cu oxide removal and how to perform this pretreatment has a profound effect on device reliability and electromigration because it dictates the cohesive forces between the materials.

Cu is an attractive material for interconnect metallization due to its low bulk resistivity and high reliability against electromigration. However, it tends to diffuse into the nearby dielectrics, causing the leakage current. For this reason, Cu interconnection wires need a layer of refractory metal as a diffusion barrier around it to prevent Cu diffusion.

Table 2-1. Low dielectric constant Materials for ULSI Interconnects.

Dielectric	Dielectric constant(k)	Glass Transition temperature (Tg: °C)	Refractive Index	Water absorption(%)	Stress(Mpa)	Gap fill (μm)	Weight Loss (%wt) at 450°C	Cure Temperature (°C)
FSG(silicon oxyfluoride)	**3.4-4.1**	**>800**	**1.42**	**<1.5**	**-130**	**<0.35**	**none**	**no issue**
HSQ(hydrogen silsesquioxa	**2.9**	**>500**	**1.37**	**<0.5**	**70-80**	**<0.10**	**<3**	**350-450**
Nanoporous silica	**1.3-2.5**	**>500**	**1.15**	**TBD**	**0**	**<0.25**	**none**	**400**
Fluorinated polyimide	**2.6-2.9**	**>400**	**△RI>0.15(ai**	**1.5**	**2**	**<0.5**	**<0.1**	**350**
Poly(arylene) ether	**2.6-2.8**	**260-450**	**1.67**	**<0.4**	**60**	**<0.15**	**<1.0**	**375-425**
Parylene AF_4 (aliphatic tetrafluorinated poly-p-xylylene)	**1.548**	**T_{melt}>510**	**△RI 2.5 >0.09(ai)**		**100**	**0.18**	**0.5**	**420-450**
PTFE (polytetrafluoroethylene)	**1.9**	**-100**	**1.34**	**<0.01**	**25-27**	**<0.30**	**0.8**	**360-390**
DVS-BCB (divinyl-siloxane bisbenzocyclobutene)	**2.65**	**>350**	**1.561**	**<0.2**	**30-35**	**<0.22**	**<1.0**	**300**
Aromatic hydrocarbon	**2.65**	**>490**	**1.628**	**<0.25**	**55-60**	**<0.05**	**<1.0**	**400-450**
Hybrid-silsesquioxanes	**<3.0**	**T_{melt}>250**	**1.58**	**0**	**30-40**	**<0.1**	**6**	**450**

Table 2-2. The requirements for low-*k* dielectrics.

Requirements for Low-*k* Dielectrics	
Film Properties	**Manufacturing**
Dielectric Constant: - Bulk: $k < 2.7$ - Effective: k=3.0~3.6 Thermal Stability: - High thermal conductivity - $T_g > 400^oC$, stable above 425^oC for short periods - Low expansion Electrical properties: - High reliability - Leakage current: Similar to SiO_2 - Breakdown field: Similar to SiO_2 - Dissipation Factor: <0.01 - Low charge trapping Film Composition: - Low film stress - >2 mm thick cracking threshold	Integration: - Good adhesion to metals (Ta, TaN, TiN, Cu), oxides/nitrides - CMP compatible - High gap-fill and planarization - Minimize need for liner/capping films - Etch Selectivity to nitrides, oxides, oxynitrides - O_2 ash/solventcompatible - Avoid C_2H_6, C_3H_8 (CVD) - Avoid toxic solvents (spin-on dielectrics)

Table 2-3. The structure of low-*k* precursors.

Molecule	Si-CH_3:Si	O:Si	Si-H:Si	Chemical Formula
MTES	1:1	3:1	na	$Si(OC_2H_5)_3(CH_3)$
DEMS	1:1	2:1	1:1	$SiH(OC_2H_5)_2(CH_3)$
DMOMS	1:1	2:1	1:1	$SiH(OCH_3)_2(CH_3)$
TOMACATS	1:1	1:1	1:1	$(SiH(CH_3)O)_4${cyclic}
DM-DOSH	2:1	2:1	na	$(CH_3)_2Si(O_2C_3H_6)${cyclic}
DMDMOS	2:1	2:1	na	$Si(OCH_3)_2(CH_3)_2$
1MS	1:1	na	3:1	$SiH_3(CH_3)$
2MS	2:1	na	2:1	$SiH_2(CH_3)_2$
3MS	3:1	na	1:1	$SiH(CH_3)_3$
4MS	4:1	na	na	$Si(CH_3)_4$

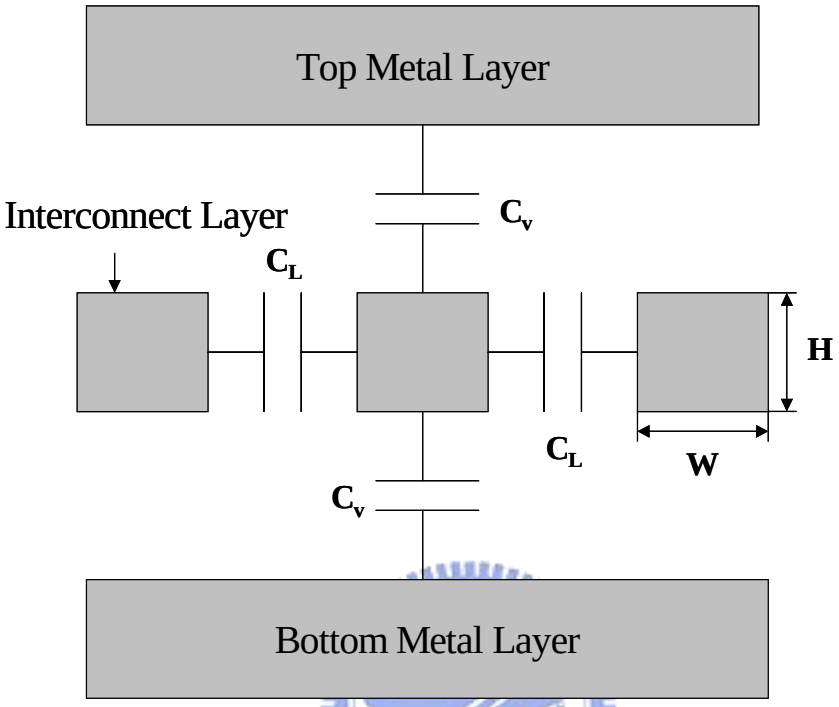


Figure 2-1. The cross-section of interconnect system with parasitic capacitance.

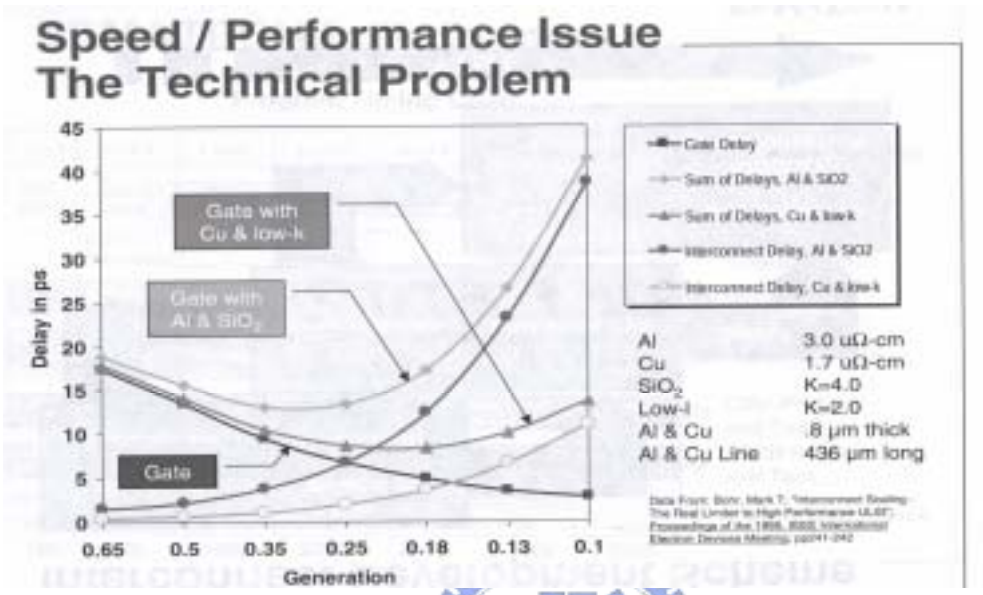


Figure 2-2. Decrease in interconnect delay and improved performance are achieved using copper and low-*k* dielectrics.

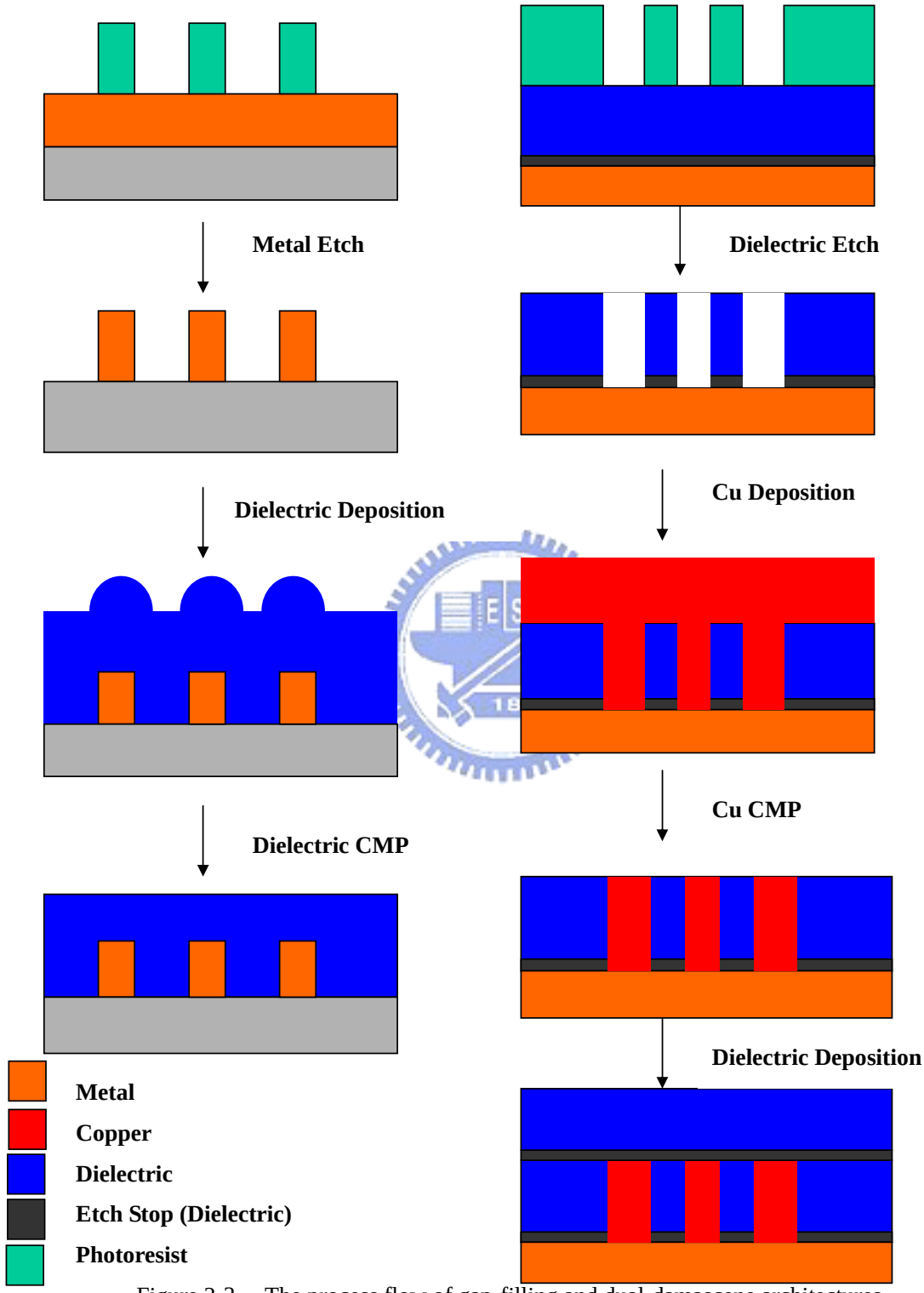


Figure 2-3. The process flow of gap-filling and dual-damascene architectures.

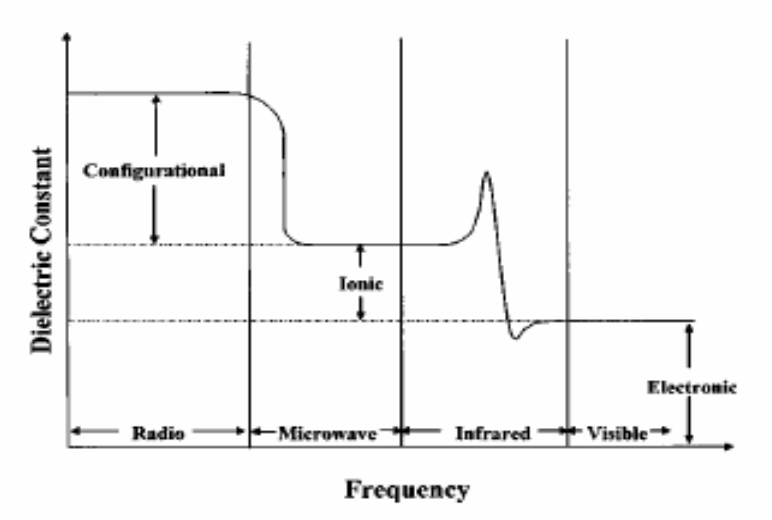


Figure 2-4. The dispersion of dielectric constant.

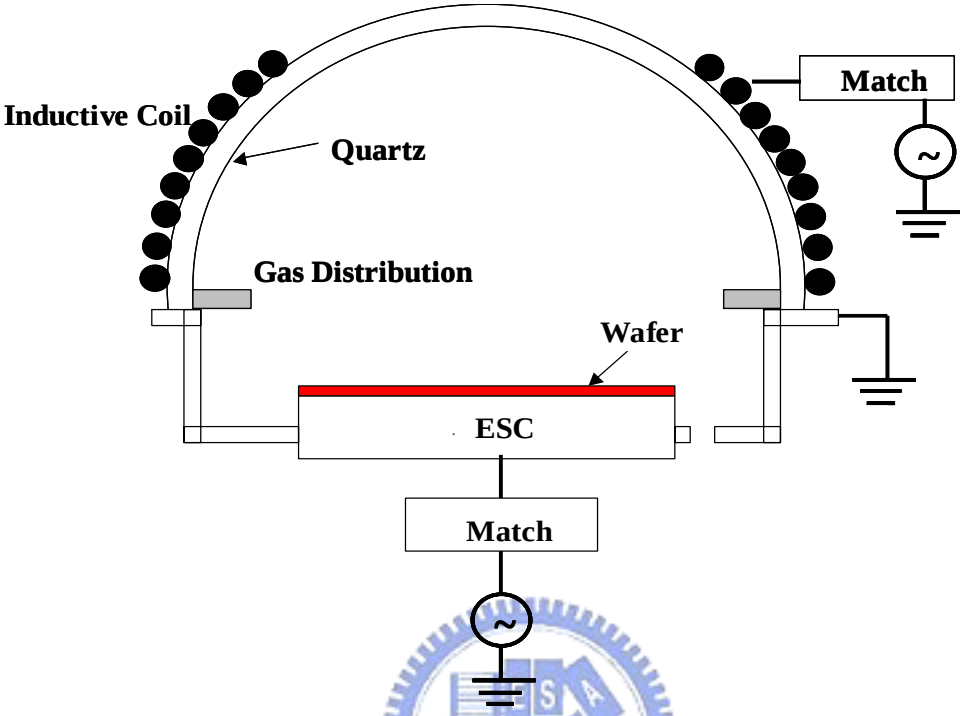


Figure 2-5. Schematic diagram of a biased-HDP-CVD system for the deposition of FSG films.

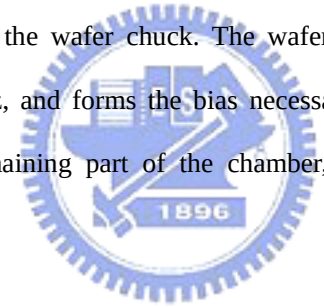
Chapter 3

Materials and Experimental

3-1 Deposition System

3-1-1 High Density Plasma Chemical Vapor Deposition (HDP-CVD)

The HDP-CVD system was used to deposit the FSG films. Figure 3-1 illustrates a schematic configuration of the microwave HDP plasma CVD system. Microwave power of 2.00 MHz frequency is coupled into the chamber by the cylindrical coil across a large quartz dome. The very top of the dome is replaced by a plat silicon section, which forms the grounded counter electronic to the wafer chuck. The wafer chuck is capacitively powered, up to 3000W at 1.8 MHz, and forms the bias necessary for the Argon (Ar) ion-sputtering component. The remaining part of the chamber, below the dome and around the wafer, is grounded.



The wafer was firmly held to the chuck by the electrostatic chuck (ESC), which allowing proper temperature control of the wafer during deposition. Electrostatic chucks operate on the principle of Columbic charge attraction, similar to the concept of a capacitor where charges separated by a dielectric create an attractive electrostatic force.

The independent helium-cooling (IHC) module is used to deliver and control the helium pressure delivered to the wafer backside. Due to the large ion bombardment component of the process, high heat flux enters the wafer, causing high wafer temperature. There is an inadequate mode of removing the heat from the wafer due to the low process pressure regime. In order to control the temperature and prevent overheating

of the wafer during processing, backside helium cooling was used to control the wafer temperature.

3-1-2 Plasma Chemical Vapor Deposition (PE-CVD)

Figure 3-2 illustrates a schematic configuration of the Lamp Heated Plasma-Enhanced CVD system. The process gas is distributed evenly onto the wafer through the hundreds of holes in the showerhead. The susceptor assembly holds the wafer directly below the gas distribution plate. A lamp module mounted directly below the process chamber radiantly heats the susceptor through a frosted quartz window. The susceptor is grounded to RF energy. The plasma is created by transmitting RF with a 13.56 MHz frequency generator into the chamber. During the normal operation, the chamber body temperature is between 40°C to 60°C, and the susceptor temperature is approximately 400°C.

3-2 Testing Method

3-2-1 Gap-filling Check

7000Å thick of Al patterns with metal width/gap of 0.23 μm/0.23 μm, 0.21 μm /0.21 μm, 0.19 μm /0.19 μm was used for the gap fill study. The gap fill capability of FSG films was verified by the cross-section SEM.

3-2-2 Heating Test

The low-*k* film samples were annealed in a furnace at temperature from 300 to

700°C for 1 h. in nitrogen ambient.

3-2-3 Moisture stress test

Pressure cooking test (PCT) was carried out as moisture stress test on the deposited film. The PCT condition is at 100% relative humidity (RH), 120°C, and 2 atmosphere for 2 h.

3-3 Characterizations and Analysis

3-3-1 Fourier Transform Infrared Spectroscopy (FTIR)

Fourier Transform Infrared Spectroscopy (FTIR) should be the most widely used analytic method for the molecular structure characterization. All samples were qualitatively analyzed by FTIR (Bia-rad Model QS300) from 400 to 4000 cm^{-1} with 4 cm^{-1} resolution by using a globar as the infrared light source. The infrared light transmitted through the sample at normal incidence then through a KBr grating into the MCT detector. The absorption features of the samples were recorded by subtracting the absorption spectra of a blanket Si substrate as the background signals.

3-3-2 X-ray Photoelectron Spectroscopy (XPS)

Surface analysis by XPS is accomplished by irradiating A sample with monoenergetic soft X-ray and analyzing the energy of the detected photoelectrons. The

XPS measurements were carried on Thermal VG-Scientific (VG-310F) model by using twin anode of Mg Ka and AlKa, operating at 1253.6eV and 1486eV, respectively. The X-ray source is at an angle of 54.7 with respect to the analyzer. An In-situ 3KeV Ar^+ ion gun was applied to sputter the sample. Energy calibration was done by using the Au 4f peak at 83.8 eV.

3-3-3 Auger Electron Spectroscopy (AES)

AES is an analytical technique used to determine the elemental composition. In many cases, the chemical state of the atoms in the surface region of a solid material. It is nondestructive, uncombined with depth profiling measurement. The AES analysis was conducted in a Perkin-Elmer PHI 670AM scanning Auger microprobe. The chamber was evacuated to a pressure of ~10 torr after samples loaded. The beam voltage for survey scan and depth profile are 20 kV and 10 kV, respectively, and the resolution is 1 eV for the survey scan. In AES, the derivation from dN(E)/dE is used rather frequency. The need for differentiation arises because the number of the background secondary electrons is usually larger than the number of Auger electros.

3-3-4 Secondary Ion Mass Spectroscopy (SIMS)

SIMS used in this study is CAMECA IMS 6f system which is magnetic sector SIMS. The analysis conditions were O_2^+ primary ion source with 3 kV impact energy. Raster area was 200 um X 200 um square with 66 um diameter analysis area. Electron gun was used for neutralization, the current was set at about 10 mA.

3-3-5 Field Emission Scanning Electron Microscopy (FE-SEM)

The topography and the cross sectional morphology of the specimen were examined by the Field Emission Scanning Electron Microscopy (FE-SEM) (Hitachi Model S-5000) with a resolution of 2 nm.

3-3-6 Transmission Electron Microscopy (TEM)

The cross section of the sample was examined by the TEM (80KV, Zeiss Model EM902) with a line to line resolution of 0.344 nm.

3-3-7 Thermal Desorption Spectroscopy (TDS)

The gas desorption of deposited films was examined by the Hitachi TDS-APIMS (thermal desorption system-atmospheric pressure ionized mass spectrum), the rate of raised temperature is 20^{o}C/min., ranging from room temperature to 800^{o}C. The intensity of mass spectrum is calibrated by sample mass.

3-3-8 Nuclear Magnetic Resonance (NMR)

Solid state NMR data were collected on a Varan Unity Plus 300MHz NMR spectrometer at 75.4 MHz for 13C and 59.5 MHz for 29 Si. The high-resolution spectra were measured using CP-MAS with sideband suppression (TOSS) on a 7 mm Magic Angle NMR probe at a spin rate of 400 Hz at room temperature. A pulse width of 4.0-4.5 usec. was used with relaxation times of 3-5 sec. Chemical shifts are reported relative to external hexamethylbenzene for carbon and talc for silicon spectra.

3-3-9 Nano-indentation

Nano-indentation utilizes a diamond tip that is pressed into the material of interest, and subsequently retracted, which monitoring the required force and indent depth. Nano-indentation was used to measure the hardness and Young's module of the deposited films. To avoid the effect of substrate, the maximum loading depth does not exceed the one-tenth of the film thickness.

3-3-10 Capacitance-Voltage Characteristics (C-V)

The dielectric constant and leakage current of all the films were measured by determined the capacitance-voltage (C-V) and I –voltage (I-V) characteristics (Keithley Model 595) at 1 MHz. The mask with a diameter of 250 um was covered on our films. The Pt layer was coated on the mask as the upper electrode for the C-V measuring of MIS (metal-insulator-semiconductor) structure. The dielectric constant was therefore calculated by the capacitance recorded by Keithley Model 595 and the thickness of the film was determined by an optical measurement.

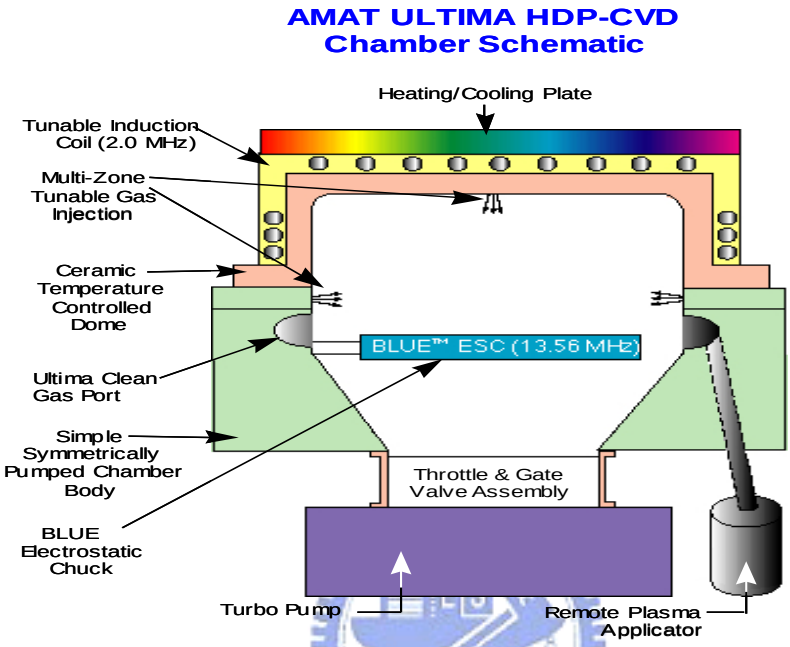


Figure 3-1. Schematic diagram of a biased-HDP-CVD system for the deposition of FSG films.

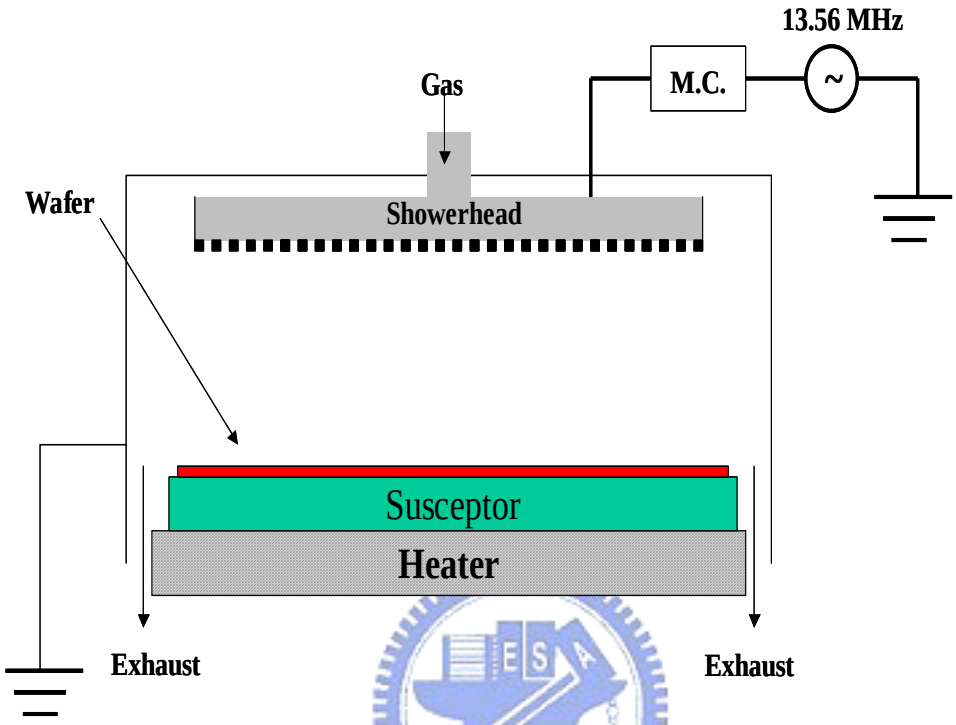


Figure 3-2. Schematic diagram of a PE-CVD system.

Chapter 4

Characterization of Fluorosilicate Glass

Silicon dioxide (SiO_2) films formed below 450^oC have often been used for the IMDs. However, the relatively dielectric constant of the SiO_2 film that is deposited by a plasma-enhanced chemical vapor deposition (PE-CVD) technique with a tetra-ethoxy-silane (TEOS) and O_2 gas system is more than 4.3. High-density plasma chemical vapor deposition (HDP-CVD) SiO_2 film has the lowest dielectric constant value (4.1-4.2) among these IMD films due to less moisture content. There is considerable interest in the IMDs with dielectric constant lower than SiO_2 film. Additionally, HDP-CVD also provides good gap-filling ability.

In the HDP-CVD technology, the deposition and the physical sputter etching processes are carried simultaneously. This biased HDP-CVD method utilizes a dependency of an Ar sputter-etching rate upon an incident angle. The rf power supplied to the substrate generates a large self-bias voltage that accelerates the ionized Ar atoms to the substrate effectively. The sputter rate at the corner of the interconnect is higher that on any other surface and this effect contributes to the good filling of the narrow gaps.

Fluorine-doped silicon oxide, i.e. fluorine glass (FSG), is one of the promising materials for low dielectric constants IMDs. Several reports indicate that the dielectric constant of silicon oxide films can be reduced by increasing the amount of fluorine, and the dielectric constant reduces about 3.0, when the FSG films usually have fluorine concentrations ranging from 2 to 14 at. %. FSG films are organic and easy to introduce into ULSI production without major changing other processes drastically in manufacturing devices.

On the other hand, fluorine concentration in the film greatly influences integration. Higher fluorine concentration can improve gap-filling characterization, however, it also cause moisture uptake and fluorine diffuse problems.

4-1 Characterizations and Reliability of Low Dielectric Constant HDP FSG Process

4-1-1 Motivation

When the minimum geometry in the integrated circuits (ICs) continues to shrink, the most challenging tasks in the interconnects are using new materials such as low-*k* and low R materials to reduce the RC delay [71]. With the reduction in capacitance, the signal propagation speed in the devices will increase and achieve a better performance. To adapt to these changes, Cu has been well accepted as the new low R material to replace Al/Cu alloy for metal interconnects in the semiconductor industry. Regarding to the low-*k* materials, there are various candidates such as FSG, Hydrogen Silsesquioxane (HSQ), Flare, Poly(arylene ether) (PAE), Benzocyclobutene (BCB). However, it is very hard for a low-*k* material to fulfill all the requirements [72]. Since HDP-USG or Sub-Atmosphere-CVD (SACVD) have been used for the dielectric layers for 0.25 μm devices, it would be easier to implement low-*k* CVD dielectric, such as FSG with dielectric constant lower than SiO_2, for sub-0.18 μm devices. Because of these reasons, many research and development groups have investigated the feasibility of using FSG in sub-0.18 μm processes. However, there are several integration issues related to the device reliability that need to be considered before implementing FSG in sub-0.18 μm processes. Therefore, the uniformity of F distribution; F

stability under high temperature and humid environment, gap-filling capability, line-to-line capacitance reduction, and via resistance were investigated in this work.

4-1-2 Experimental Procedures

FSG films were prepared using a HDP-CVD system with gas sources of SiF_4, SiH_4, O_2, and Ar. The USG film was also deposited in the same system with the gas source of SiH_4 and O_2. The substrate temperature was set at 420°C. The film thickness and refractive index of FSG films were measured using an elliposometer. The Si-F peak and F percentage were monitored by Fourier Infrared Spectroscopy (FTIR) and Secondary Ion Mass Spectroscopy (SIMS), respectively. The F% distribution was measured at the center of 8" Si wafer and at 8 mm away from the edge of the wafer. The dielectric constant was measured using a Mercury Probe at 1 MHz. On the other hand, FSG films were deposited on 2000Å USG/7000Å Al stack structure for thermal stability study. In addition, there were two kinds of cap layer for FSG used in this study: SRO and PE-OX. The SRO and PE-OX cap layer were deposited by a Plasma Enhanced CVD (PE-CVD) system. These films were annealed at 400°C for 3 h and then tested under pressure cook test at 100% RH, 120°C, 2 atmosphere for 2 h. 7000Å thick of Al patterns with metal width/gap of 0.23 μm/0.23 μm, 0.21 μm /0.21 μm, 0.19 μm /0.19 μm was used for the gap fill study. The gap fill capability of FSG films was verified by the cross-section SEM. The capacitance reduction and via resistance at different metal widths and gaps were measured by using a two-layered Al metal structure deposited with 600Å of USG liner, 8,000Å of FSG ILD layer, and 2,000Å of SRO cap layer.

4-1-3 Results and Discussions

1. F uniformity

The uniformity of F distribution in FSG films is the first integration issue we investigated. The concern for the non-uniform distribution of F is that the capacitance reduction and the device performance vary with the location of the devices on the wafer. This will lead to a wide distribution on device performance for devices processed on the same wafer, which is not practical for manufacturing.

It has been known that the introduction of F can reduce the dielectric constant of SiO_2 films [73-76]. It is because that F can reduce the ionic and electronic polarizability in the oxide films by replacing Si-O bond with Si-F or Si-O-F bonds [77]. Generally, the dielectric constant of FSG decreases with increasing the F content until it reaches the minimum and then increases with increasing the F content [76]. It has been reported that the stable FSG film happened at 3-5% of F percentage with SiF_4 as the gas source [76]. As F percentage larger than approx. 4.5%, the dielectric constant of FSG film increases due to the presence of highly polar Si-O-H bond when moisture is picked up by the films. However, the F percentage to achieve minimum dielectric constant depends on the reagents and the process conditions [73, 78].

Since SiF_4, SiH_4 and O_2 were used as the reagent sources for film deposition, FSG films with 3.3% to 4.9% of F were deposited on Si wafers for this study. The refractive index and dielectric constant of FSG films with different F concentrations were shown in Figure 4-1-1 and 4-1-2. It shows that the R.I. decreases from 1.444 to 1.436 as the F % increases from 3.3% to 4.9%. The dielectric constant also varies from 3.35 to 3.63 depending on the F % in the FSG films. All FSG films show non-uniform F % at the center and the edge locations of 8” Si wafers. It is found that the F% in FSG films is

higher at the edge of the wafer than that at the center. The difference is about 0.2 at. % of F which represents 0.2 in dielectric constant. The higher dielectric constant of 3.6 at the center compares to dielectric constant of 3.4 at the edge. It may be caused by the plasma density non-uniformity across the wafer and the in-let of the SiF_4 gas inlet location. This non-uniformity in F% and dielectric constant will cause the large variations in device performance depending on its location on the wafers

2. F stability

The second concern for the integration reliability of FSG film is the film stability. It has been know that FSG films are not stable if the F % is too high and reduces its resistance to moisture [73]. The absorbed moisture in FSG films will react with the Si-F bonds and become Si-O-H and HF. The increasing in highly polarized O-H bond will increase the dielectric constant. In addition, the HF and F diffused out of the films at high temperature will react with Al lines resulting in the Al corrosion [79].

The F stability in FSG film without any cap layer was under PCT for 2 h and 400°C annealing for 3 h was shown in Figure 4-1-3. The data shows that the F in FSG decreases from 3 x 10^{21} atoms/cm^3 at the FSG/USG interface to 2 x 10^{21} atoms/cm^3 at FSG/air interface. It indicates that F is not stable in FSG films and diffuses out of the films after the PCT and 400°C annealing.

It has been suggested that FSG films can be capped with 200 to 500 Å oxide film to prevent F diffusion out of the FSG film and enhanced the stability of FSG film [80]. In addition, exposing FSG to the CMP slurry will form HF due to the F dissolving in water. This cap layer can prevent FSG from direct contact with CMP solution. Therefore, two different cap oxide layers, SRO and PE-Oxide, as the diffusion barriers for HDP-FSG

were studies.

FSG films capped with SRO before and after PCT and 400°C annealing were shown in Figure 4-1-4 and 4-1-5, respectively. The FSG film capped with SRO shows that the F concentration is slightly lower than that before tests. It indicates that there are some F atoms depleted in FSG films. However, the F concentration is still very low before and after PCT and 400°C annealing at SRO/air interface. Instead, F concentration is slightly higher at the SRO/FSG interface after tests. This indicates that SRO layer can be a good barrier layer for F diffusion. In Figure 4-1-6, FSG film with SRO cap layer still remained stable after 48 h in ambient, PCT and annealing test. The depleted F in FSG film was accumulated at the SRO/FSG interface. For FSG films capped with PEOX, the F diffused into PEOX cap layer and generated an F concentration gradient in PEOX layer and FSG layer close the PEOX/FSG interface as shown in Figure 4-1-7. This indicates that using PEOX as the FSG cap layer can not block the F diffusion.

3. **Gap-Filling Capability**

The third concern for the integration reliability of FSG is the gap fill capability. As the minimum geometry of IC devices becomes smaller and smaller, the gaps between metal lines become smaller as well. Since the film deposition rate is lower at the side wall of metal gaps than at the bottom of the gap, there is a limitation for the smallest gap that dielectric film can fill it by CVD method. If the deposition rate is too fast, it will generate the voids in the gap. It has been reported that HDP-CVD can enhance the gap fill capability of USG for 0.25 μm processes due to the slower deposition rate of HDP [73]. In addition, F in SiO_2 may facilitate the deposition to fill a smaller gap. In the 0.18 μm design rule, the minimum metal gap should be close to 0.23 μm. Therefore, HDP-FSG

film needs be able to fill metal gap smaller than 0.23 μm before it can be used for 0.18 μm processes.

The gap fill capability was investigated by depositing FSG films on pattern wafers with different metal width/gap: 0.23 μm/0.23 μm, 0.21 μm/0.21 μm, and 0.19 μm/0.19 μm. The results show that FSG films can fill all 0.23 μm/0.23 μm patterns at the center and the edge pattern in the wafers as shown in Figure 4-1-8 and 4-1-9. However, FSG films can fill the 0.21 μm/0.21 μm patterns at the center but not the 0.21 μm/0.21 μm at the edge of wafer. Especially, the gap fill is the worst for gaps in the wafer at notch area (Figure 4-1-10). For 0.19 μm/0.19 μm patterns, large holes were observed both in the center and the edge of wafer. It is found that the aspect ratio is approx. 3.4 at the center of wafer, is approx. 3.8 at the edge of wafer, and is approx. 4 for wafer notch region. Apparently, the FSG can only fill the 0.21 μm/0.21 μm gas with aspect ratio up to approx. 3.6 and there is void generated when the aspect ratio increases to 3.8. Therefore, with the capability of filling 0.23 μm/0.23 μm gaps, FSG can still be used for 0.18 μm processes.

4. **The capacitance reduction and via resistance**

The last concern for the reliability is the capacitance reduction and via resistance of FSG film. Since the purpose of using low-*k* materials is to reduce the capacitance for smaller geometry, the capacitance reduction will direct affect the device performance. In addition, the via resistance for FSG film needs to be investigated to ensure that FSG can be processed without affecting the via yield. Since SRO is good diffusion barrier for F, devices with 600Å USG/8000Å FSG/2,000Å SRO sandwich structures were processed for capacitance and via resistance measurement.

The line-to-line capacitance of patterns with FSG as the dielectric layer was

measured at different metal widths and gaps. For the metal line-to-line capacitance, it was found that the there was approx. 7.45% to 7.7% reduction in capacitance for 0.23 μm/0.23 μm pattern and approx. 6.75% to 7% reduction in capacitance in 0.23 μm/0.46 μm pattern as shown in Figure 4-1-11 and 4-1-12. In addition, the capacitance reduction also varies with the metal width as shown in Figure 4-1-13. It shows that FSG with wider metal line has a larger impact than the thinner metal line on the line-to-line capacitance. It is believed that the larger capacitance observed at wider metal lines is due to a larger fringe capacitance between wider metal lines. The via resistance of FSG at different unlanded via mis-alignment is shown in Figure 4-1-14. It shows that the FSG has similar unlanded via resistance to USG. It is consistent with the results that FSG can have similar via yield as USG.

4-1-4 Summary

In our study, it was found that there is approx. 0.2 % of F variation between the center and the edge of wafers. This non-uniform F distribution leads to the variation in dielectric constant for about 0.2 at the center and the edge of wafers. Because of that, the device performance will vary for devices processed on the same wafer and it will be a concern to put FSG into production. The SIMS data shows that the thermal stability of FSG can be enhanced by using a cap layer and SRO is superior than PE-OX in blocking the F diffusion at high temperature and moisture environment. HDP-FSG can fill the gap as small as 0.23 μm gap which indicates that FSG can be used for the 0.18 μm processes. However, it will be more difficult to use FSG in process less than 0.18 μm. In 600Å USG/8000Å FSG/2,000Å SRO cap layered structure, HDP-FSG shows 7.45 to 7.7% line-to-line capacitance reduction and has similar via resistance to that of USG film.

Therefore, HDP-FSG with SRO cap layer can be used for 0.18 μm processes if the issue of the F% variation in the FSG film can be improved.

4-2 Effect of Deposition Temperature on Thermal Stability in High-Density Plasma Chemical Vapor Deposition Fluorine-Doped Silicon Dioxide

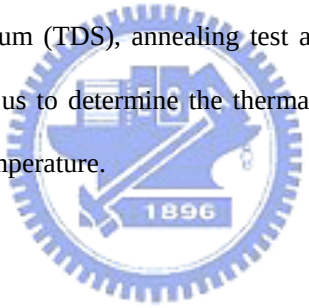
4-2-1 Motivation

With the progress of high integration and modern ultra-large-scale integration (ULSI) with gate widths of less than 0.25 μm, it has become necessary to improve device operating speed, which is limited by the capacitance of inter-metal dielectric (IMD) capacitance. To reduce the IMD capacitance, fluorine-doped silicon dioxide (FSG) [81] films deposited by high-density plasma chemical vapor deposition (HDP-CVD) have been introduced in an advanced IMD application. The HDP-CVD technique has been demonstrated to have good gap-filling capability and film stability [82,83]. Moreover, Yang et al. [84] in 1998 successfully incorporated FSG films into 0.18 μm logic devices. As a consequence, FSG films are considered a suitable and manufacturable low-*k* IMD for below 0.25 μm devices.

Many researchers have studied the formation process of fluorine-doped silicon dioxide films, viewing it as having a low dielectric constant, excellent gap-filling ability due to in-situ etching by SiF_4, and being void free. They pointed out that the higher fluorine concentration would lower the dielectric constant [85-88] and improve the gap-filling ability. However, these researchers also express caution that FSG films have a

thermal stability issue that affects the integration. The subsequent deposition of FSG capped silicon-dioxide (SiO_2), metal film, and passivation layer has shown blistering after the alloying process [89]. As a result, new precursors, reaction methods, and optimized process conditions have been proposed to improve the thermal stability of FSG films [90-93].

In this work, we conducted a comprehensive study of the dependence on the deposition temperature of the physical properties and thermal stability of FSG films prepared by HDP-CVD using Ar, O_2, SiH_4, and SiF_4 gas. The relevance of the deposition temperature in influencing the properties of FSG films was reported. Also, a comparative analysis of thermal desorption spectrum (TDS), annealing test and secondary-ion mass spectrometer (SIMS) results allowed us to determine the thermal stability of individual FSG films with varying deposition temperature.



4-2-2 Experimental Procedures

The FSG films were prepared in an Ultima HDP-CVD Applied Materials Centura 5200 system using $Ar/O_2/SiH_4/SiF_4$ as reaction gas. The gas flow rate of Ar, O_2, SiH_4, and SiF_4 were 50, 110, 45, and 30 cm^3/min., respectively. The deposition temperature was detected at the backside of the deposited wafer by a wafer temperature monitor (WTM). The backside He pressure was adjusted to control the deposition temperature, which varied from 350 ^{o} to 450^{o}C. The as-deposited films were analyzed for thickness and refractive index (RI, at 633 nm) by reflectometry and/or ellipsometry using the Nano-Spec 9100. This thickness of the FSG film is the net-deposition (ND) thickness,

which is the sum of deposition, sputter and etch. The sputter (S) rate was measured by sputtering the FSG films for 60 seconds on a blanket wafer using Ar gas. The pure deposition (PD) thickness (no sputter /etch effect) was calculated by setting the bias-RF as zero on a blanket wafer. Therefore, the removal thickness of sputter and etch (S+E) effects should be the PD thickness minus the ND thickness. Besides, the etch (E) rate was calculated through the removal thickness of sputter and etch (S+E) minus the thickness of S. TDS and furnace alloy samples were deposited directly on bare silicon wafers. In addition, SIMS was used to analyze the film structure based on a silicon wafer that is covered with a silicon-dioxide film, FSG film with different temperature, and capped silicon-dioxide oxide.

The furnace annealing condition reached 425°C for 60 min. in nitrogen ambient and the alloying process required seven heating/cooling cycles in total. Next, the fluorine concentration was measured before and after alloying by Fourier transform infrared spectroscopy (FT-IR) using the peak Si-F was about 930 cm^{-1} and also using X-ray fluorescence (XRF). A Bio-rad FT-IR spectroscope was used to collect absorption spectra and quantified the Si-F/Si-O peak-height ratios in reflectance mode. FT-IR analysis was performed at a resolution of 4 cm^{-1}, averaging 16 scans. XRF detected the non -Si-F-bonding fluorine in 200 second scans. The FSG films with different deposition temperatures were prepared, and then the gap-filling capability of the various FSG films was determined by scanning electron microscopy (SEM). Subsequently, the structure of short-loop samples was simulated on a 0.18 μm IMD scheme, to verify and support previous TDS and alloying results.

4-2-3 Results and Discussions

1. Film Property

Figure 4-2-1 shows the refractive index of FSG thin films, measured by ellipometry, as a function of the FSG deposition temperature. For these films deposited by HDP-CVD, the refractive indices are 1.40-1.45, which are lower than the 1.46, value of thermal oxide SiO_2. It is well known that the refraction index is closely related to the porosity of these SiO_2-based materials, being smaller for higher porosity. Therefore, porosity might be one reason for the lower refractive indices. However, as shown in Figure 4-2-1, the refractive index decreases appreciably with decreasing FSG film deposition temperature, but with increasing fluorine content. This shows that the lower refractive index may also influenced by fluorine incorporation into SiO_2. Further support for this may be found with FT-IR spectra. We find that at lower deposition temperature, the peak of the Si-O stretching band shifts to higher frequency, in the presence of a high concentration of fluorine in the structure. As a consequence, the Si-O-Si bonds are weakened so that they become less rigid and more stretchable, resulting in a cage structure (porosity) in the film. This structure causes the film's density to decrease. Therefore, the refractive index also decreases with decreasing deposition temperature. Agreeing with this result, the dielectric constant of the as-deposited FSG film decreases to 3.346 at 350^{o}C from 3.964 at 450^{o}C. The reduction of electronic polarization by more Si-F bonds and by an increment in porosity in the FSG film, both contribute to a lower dielectric constant. Table 4-2-1 summarizes the trends for increasing deposition temperatures. The deposition rate increase as FSG deposition temperature decreases owes to fluorine having less thermal energy in which to provide plasma etching. For higher

deposition temperatures, the FSG film becomes denser as a result of the plasma etching ability to remove weak bonds, and results in a material having lower wet etch rates. It is worth noticing that the hardness of the FSG films decrease as deposition temperature decreases due to increase in porosity and decrease in cross-linking of terminal Si-F bonds. The hardness of the low-*k* film is an essential property during processing with chemical mechanical polishing (CMP).

2. Gap-Filling Ability

As the minimum geometry of integrated-circuit devices becomes increasingly smaller, the separation between metal lines becomes smaller, as well. Because the deposition rate is lower at the side wall of the metal gaps than at the bottom of the gap, HDP-CVD has been introduced to enhance the gap-filling ability owing to the sputter ability of HDP. However, it still has difficulties in filling higher-aspect ratio gaps, without voids (Figure 4-2-2a). On the other hand, we can use the etching ability of fluorine to facilitate the deposition to fill the smaller gap (Figure 4-2-2b). Therefore, to investigate the effect of deposition temperature on gap-filling ability, we separated the HDP-CVD FSG deposition process into three main reactions: deposition (D), sputter (S), and etch (E). Furthermore, we also defined the parameter D/(S+E) as the gap-filling index. The better the gap-filling capability, the smaller the D/(S+E) value. The calculated results are summarized in Table 4-2-2. As seen in this table, the E/(S+E) value quantifies the contribution of the etch component of the total removal in the HDP-CVD FSG process, and this value increases with the rise of deposition temperature. The result also shows that the sputter rate is temperature independent in our experimental temperature range. Thus, the etch rate contribution to the total removal rate increases with temperature.

There is about a 5% increase in etch rate with an increase of 50^{o}C temperature, which causes a decrease of the D/(S+E) ratio. Therefore, we infer that FSG films with higher deposition temperature prepared by HDP-CVD have high gap-filling capacity compared to those with lower deposition temperature.

The gap-filling ability was investigated by depositing FSG films with different deposition temperatures wafers pattered with different metal widths/gaps. Figure 4-2-3 reveals that 350^{o}C-deposited FSG film can fill into the metal gap with 0.25 μm spacing, but not reach the void-free requirement for a 0.21 μm gap (Figure 4-2-3a). On the other hand, a higher deposition temperature (~450^{o}C) can fill a 0.21 μm metal gaps (aspect ratio was 3.6) and with no metal clipping, which implies that the etch ability of the F-atom has increased abruptly at the higher temperature on the wafer. Again, we also demonstrate that the deposition rate decreases with increased deposition temperature due to the fact that F etches SiO_2 more effectively at high temperature.

3. Thermal Stability-Out gassing Issues

In real interconnect fabrication, thermal treatment is an indispensable step. Here, the interconnect medium consists of up to 8 separate layers, all of which are deposited at about 400^{o}C. As a result, a suitable interconnect dielectric should possess excellent thermal resistance. To study the thermal stability of FSG films with varying deposition temperature, the films were annealed in N_2 ambient for 1 h at 425^{o}C. The film thickness, RI, and fluorine concentration (FT-IR value) after annealing all remained stable even after repeated annealing tests (seven times) through the entire range of deposition temperatures. This points out that the Si-O and Si-F bonds in FSG films have enough thermal resistance against a 425^{o}C heat treatment. However, the fluorine content

measured by XRF gradually declined and reached saturation after the third annealing test. Moreover, the magnitude of this decline is dependent upon the deposition temperature of FSG films. The FSG film with lower deposition temperature has a larger change in XRF value, as shown in Figure 4-2-4. FTIR was used to monitor Si-F/Si-O ratio, calibrated with Rutherford back-scattering (RBS), and XRF detected total fluorine content (including bonding Si-F and non -Si-F- bonding fluorine). Consequently, we can use Eqn. (4-2-1) to calculate the amount of non -Si-F- bonding:

$$XRF/FTIR=1+ (non\text{ -Si-F-})/Si\text{-}F \qquad \textbf{(4-2-1)}$$

The higher XRF/FTIR ratio means a higher amount of non -Si-F- bonding fluorine. As shown in Figure 4-2-5, the lower deposition temperature of the FSG process has more non -Si-F- bonding fluorine. This result can explain the result of Figure 4-2-4. As the FSG film with lower deposition temperature was immersed into N_2 ambient at elevated temperature, more non -Si-F- bonding fluorine outgassed in the thermal process. Furthermore, after three cycles of the annealing process, for the FSG film with deposition temperature above 400°C, the outgassing reached saturation. On the contrary, the fluorine at.% (XRF value) kept decreasing for FSG films with deposition temperature below 400°C, even after seven cycles of the annealing process. This implies that FSG films deposited at temperatures lower than 400°C have greater amounts of either weak Si-F bonding or non-bonded fluorine (free fluorine). Hence, the weaker Si-F units will be broken, or free fluorine will be outgassed by the thermal process. Considering this outgas as excess fluorine, this excess could possibly be avoided by use of a lower gas ratio (SiF_4/SiX_4) and thereby keep the fluorine concentration stable after heat treatment. It is speculated that more SiF_4 (less SiH_4) would create a greater F% concentration without

being bonded with the Si atom. Of course, lowering the gas ratio might also impact the *k*-lowering property of fluorine. So a proper balance must be struck. A comprehensive study will be reported in another paper.

The thermal stability of FSG films is also studied using thermal desorption spectroscopy (TDS). Gas desorption from films, especially at lower temperature, has been a concern for device reliability issues, such as the failure of pressure cooling, thermal cycle, and thermal stress tests. The TDS spectra with respect to the mass fragment 18M/e, 19M/e and 20M/e for FSG films with different deposition temperatures are checked (not show). Corresponding to these masses, H_2O, F and HF desorption from FSG films at lower temperature for lower deposition temperature, which summarized in Table. 4-2-3. As shown, the desorption temperature of Ar is relatively insensitive to the FSG film deposition temperature. On the other hand, the desorption temperatures of H_2O, F, and HF are strongly dependant upon the deposition temperature. Higher-deposition-temperature FSG films have higher desorption temperature and with lower desorption pressure. Higher onset of evolution of desorption temperature means that the film has greater thermal stability during post-thermal processes. Consequently, we have demonstrated that FSG films with higher deposition temperature have less moisture content, greater thermal stability, and better suitability for the IMD application in the back-end process.

4. Fluorine Stability-Diffusion Issues

Fluorine stability with respect to diffusion within FSG films strongly influences its utility in IMD integration, with Al wiring delamination as one important area of concern. Fluorine stability was investigated by secondary-ion mass spectrometry using a sandwich

structure, consisting of oxide/FSG/oxide, where the oxides are 2000-Å of SiO_2. This sandwich structure was deposited on the Si substrate. All the samples were annealed at 425^oC for 1 h in N_2 atmosphere. The annealing test was performed seven times.

As observed in Figure 4-2-6(a), when the FSG film underwent thermal treatment, the fluorine atoms diffused into the adjacent oxide films. However, this diffusion was rather modest and the fluorine profile remained quite sharp at the FSG/SiO_2 interface. Therefore, we concluded that the driving force of fluorine diffusion is the overall thermal budget. Figure 4-2-6(b) compares the effect of deposition temperature on fluorine out-diffusion stability. It shows that the FSG film with lower deposition temperature exhibits a higher fluorine diffusion capability. The fluorine diffusion length for the FSG film at 350^oC deposition temperature is about ~500Å, higher than that (~200Å) of the FSG film at 450^oC deposition temperature. Most of the diffused F is believed to be weak bonding or free fluorine. As a consequence, a lower deposition temperature of the FSG film causes weaker Si-F bonds will be broken and diffused, along with the free fluorine, affecting film stability.

5. Interconnect Pattern Wafer Test

The thermal stability of FSG films with varying deposition temperature is also confirmed using actual Al interconnect test structures. The effect of the deposition temperature on via resistance for the design rule (0.23 μm width /0.21 μm spacing) of 0.18 μm using FSG films as IMD was also checked. Via resistance has no significant difference in any deposition temperature, ranging 350° to 450°C (not shown). This implies that FSG films with deposition temperature from 350° to 450^oC can be integrated well with photo and etch process. On the other hand, reliability and defects were

frequently detected on patterned wafers, especially in the case of lower deposition temperatures (350° to 400°C). A serious bubble defect was observed after completing a 7-layer metal structure. This type of defect was found on the metal pads, shown in Figure 4-2-7(a), similar with the result of Kawashima et al. [94] These defects arise from the diffusion of unstable fluorine and the reactions with the under-layer barrier layer (TiN), metal lines (Al), and passivation layer (Si_3N_4). Another defect type, i.e., peeling, is also observed for 350°C FSG film, shown in Figure 4-2-7(b). Peeling is hardly ever found in higher-deposition-temperature FSG films. Additionally, it always occurred after CMP polish. Lower hardness of the FSG film with lower-deposition temperature was suspected because the high down-force of the CMP process. To solve these problems of lower-temperature FSG film, one should increase the liner and capped layer thickness and reduce the down-force in the CMP process. However, a sacrifice of the effective dielectric constant and CMP planarization properties may occur.

4-2-4 Summary

The thermal stability for fluorine-doped silicon dioxide deposited by high-density plasma chemical vapor deposition is highly influenced by deposition temperature. All analyses, including SIMS, TDS, and annealing thermal tests, have shown that FSG films deposited above 400°C have better thermal stability. However, the high deposition temperature (over 450°C) creates metal (AlCu) extrusion and melting issues. Patterned wafers with short-loop results have also demonstrated that low deposition temperature results in F-bubble formation because of greater amount of more free fluorine. Results of this study demonstrate that the deposition temperature of FSG films is extremely

important for the films thermal stability.

4-3 A study on Fluorine Out-diffusion Effect of FSG with Different Capping Oxide

4-3-1 Motivation

When the IC device scale is keeping on shrinkage, the interconnection materials are also needed to be improved to meet the high performance and high-speed requirement [94]. The most challenge tasks in the interconnection material are the use of new materials, low resistance Cu and low capacitance dielectrics. Cu dual-damascene was used as the metal interconnect to replace AlCu metal line, W via and plug. Cu has been known as the low R material compared to AlCu alloy. In addition, it also provides good electronmigration (EM) performance [95]. For the inter layer dielectric material, there are several candidates for low-*k* material, including FSG, Hydrogen Silsesquioxane (HSQ), Flare, Silk, Black diamond [96]. Owing to FSG could be produced by HDP CVD, this had been used for HDP USG in 0.25 μm process, so it was easier to implement HDP FSG in 0.18 μm process. FSG could also be produced by PE-CVD. PE-FSG was used as sacrificial oxide for Chemical Mechanical Polishing (CMP) process. By using PE-FSG in sacrificial oxide, the inter metal dielectric process throughput could be improved. However, there were some integration considerations on using FSG in 0.18 μm process.

The physical properties of FSG were dependent on the F concentration. The higher the F concentration, the better the gap-filling and step coverage was. Higher F concentration also can lower the dielectric constant [97-100]. However, FSG films with a

higher F concentration had been shown to be unstable. The subsequent depositions of FSG capping oxide, metal film, passivation, had shown blistering after some alloys [101]. It also had been known that FSG films were not stable in moisture condition. The moisture would attack Si-F bond in FSG and transfer to Si-O-H and HF. In addition, the HF and F would diffuse out at high temperature and react with Al line resulting in Al corrosion [102].

Through this work, we found that using adequate FSG capping oxide and liner oxide, the thermal stability and adhesion of integrated FSG film could be improved. From a series of experiments, SRO is a good buffer material for FSG. It was stable and could block the F out-diffusion at a high temperature. SRO, used as FSG capping or liner oxide, had been proved to be a feasible method from production point of view.

4-3-2 Experimental Procedures

FSG films were deposited by using a HDP-CVD system with gas sources of SiF_4, SiH_4, O_2 and Ar. The substrate temperature was set at 420°C. The FSG stack films were made of single capping structure, 2kÅ capping oxide/ 6kÅ 4.35% HDP-FSG. There were three kinds of capping materials, SiN, SiON and PE-oxide. After stack films were deposited, films were annealed at 410°C for several hours. SIMS was used in detecting the F distribution along the depth profiles.

FSG films were deposited by PE-CVD system with the gas sources of SiF_4, SiH_4 and O_2. The FSG stack films were made of sandwich structure, 2kÅ capping oxide/6kÅ 6% PE-FSG/2kÅ liner oxide. Silicon Rich Oxides (SRO) with different reflection indexes were used for capping material and also as liner material. We named the various SRO

capped samples as sample#1, sample#2 and sample#3. After stack films deposition, 6 times alloys were applied on the samples at 410°C.

FSG films were deposited by PE-CVD system. During the FSG film deposition, we introduced the N_2 into the reaction chamber. One of the FSG films was grown with N_2 inlet (sample#5), the other was without N_2 inlet (sample#4). The layer structure is 2kÅ SRO/6kÅ 6% PE-FSG/2kÅ SRO.

SIMS analysis was performed by CAMECA ims-6f system. The analysis conditions were O_2^+ primary ion source with 3kV impact energy. Raster area was 200 μm*200 μm square with 66 μm diameter analysis area. Electron gun was used for neutralization, the current was set at about 10 mA.

4-3-3 Results and Discussions

1. Capping layer effect

Fluorine diffusing into to capping layer was studied by SIMS depth profiling. Figure 4-1-1 to 4-1-3 show the SIMS result on samples with different capping layer, indicating that fluorine diffuse out from FSG to capping layer can be effectively inhibited by using SiN and SiON as capping material. PE-CVD oxide as a FSG film capping material cannot inhibit the flourine diffusion out. During SIMS analysis, the ion and electron irradiation heat the insulator film and induced the FSG stack film blister. Meanwhile, we observed that the base pressure in SIMS UHV analysis chamber was getting higher from 1e-9 torr to 1e-8 torr as the film was blistering. This phenomenon implies that out-gasing from the FSG film while blister was happening. Figure 4-3-4 to 4-3-6 show the optical microscope picture of SIMS ion gun sputtered crates. No blister was found on PE-oxide

capped FSG film. On the other hand, the FSG stacked films show serious blister for SiN and SiON as capped layers. Although SiN and SiON films are good capping material to prevent fluorine diffusion out, the film adhesion due to out-gassing is a major concern during the complicated IC production and following reliability tests.

2. Nitrogen component in the capping layer effect

From Part 1, SRO was good a barrier layer to prevent fluorine from diffusing out. However, the nitrogen concentration in SRO films plays an important role in fluorine barrier performance. Figure 4-3-7 shows the SIMS depth profile on this sandwich structure, which capping layer is SRO films with varying nitrogen concentrations. As seen, the ability to inhibit F diffusion out was different with different SRO films. The SRO film with a higher nitrogen concentration in SRO film possesses the better the ability to block F diffusion out. In other consideration, SRO also shows good thermal stability during ion and electron irradiation.

3. Nitrogen component in the FSG layer

From the result of Part 2, nitrogen in the SRO film was related to F blocking capability. As a result, we designed this experiment to check if nitrogen is introduced into FSG film. The overlapping SIMS results are shown in Figure 4-3-8, indicating that fluorine had been driven out to SRO film after the post annealing. Additionally, as FSG film with a higher nitrogen content, the diffusion of fluorine becomes more serious.

4-3-4 Summary

From the above experiment, we concluded (1). SRO was good for FSG film capping and liner material. Fluorine could be effectively blocked. No film blister was observed

after 6 times alloy and ion gun irradiation. (2). Nitrogen was found in SRO material, and the nitrogen concentration was related to SRO film F-blocking-capability. The higher the nitrogen concentration in SRO film, the more effective on F blocking capability was. (3). By introducing N into FSG film, and using same capping and liner material, we found that higher N concentration in FSG film would make F diffusion out.

4-4 Novel FSG Integration Scheme- Treatment Effect

4-4-1 Motivation

As feature size shrinks continuously to deep sub-micron regime, low-*k* dielectric materials are adopted into damascene structures to reduce interconnection delay and increase device speed [103,104].

Fluorinated silica glass (FSG) films deposited by high-density plasma chemical vapor deposition (HDP-CVD) have been successfully implemented in advanced intermetal dielectric (IMD) application and mass fabrication. The FSG film has the advantages of low permittivity (k = 3.5-3.8), high gap-filling capability and especially simplicity of IMD integration [105,106]. However, high fluorine concentration of the FSG films, exceeding 5 at.%, induces water absorption and degrades film properties [79,107,108]. Moreover, fluorine out-gassing results in metal delamination due to the degradation of adhesion ability [109,110]. Several methods have been proposed to prevent the metal delamination [93,111-114]. N_2 treatment and capping of undoped-silicon-glass (USG; SiO_2) film on FSG layers have been demonstrated to eliminate the adhesion problem between FSG and Ti/TiN/AlCu/TiN metal stack [106, 110,

112]. However, the effect of process conditions of N_2 treatment and capping layers on the metal delamination is not fully studied in previous studies.

In this work, the optimum conditions of N_2 treatment and SiO_2 capping layers on the metal delamination were characterized and the mechanism of metal delamination was established as well.

4-4-2 Experimental Procedures

FSG films were deposited by Ultima HDP-CVD Applied Materials Centura 5200 system using SiH_4, SiF_4, O_2 and Ar as precursors. The subsequent N_2 treatment and USG capping layer deposition were carried out in the same chamber without vacuum breaking. These two processes were performed on FSG films with undergoing the FSG chemical mechanical polishing (CMP) process. The N_2 treatment was biased by radio frequency (rf) power. The precursors for the deposition of USG layer were SiH_4 and O_2. The fluorine concentration of FSG films was controlled at 4.5 at.% by the Si-F/Si-O ratio from Fourier transform infrared spectroscopy (FTIR) and by the calibration with Rutherford Back Scattering (RBS). FTIR spectrum was used to measure the peak intensity of the Si-F bonding. FTIR analysis was performed at a resolution of 4 cm^{-1} and averaged 16 scans. Absorption spectra were collected in reflectance mode using FTIR spectroscope Bio-Rad Win-IR PRO. The Si-F peak height was measured before and after annealing at 425^oC in N_2 ambient.

The fluorine concentration of the USG capping layer surface (<20Å) was analyzed by Dynamic Secondary Ion Mass Spectrometer (TOF-SIMS) with a gallium liquid metal ion gun (LMIG) as primary ion source. TOF-SIMS was operated in an ion microprobe

modem, in which the bunched, pulsed primary ion beam was raster across the sample surface.

Surface morphologies and cross-sectional images were examined using an optical microscope (OM) and a field emission scanning electron microscope (FESEM).

4-4-3 Results and Discussions

Figure 4-4-1 shows the repeating process flow of Al/Cu metallization in sub-0.18 μm scale device technologies, in which the Ti/TiN metals and HDP-FSG films were used as diffusion barrier and dielectric layers, respectively. After FSG-CMP, the subsequent N_2 treatment and USG capping layer deposition were carried out in the same chamber without vacuum breaking. The bias power, process time and N_2 flow rate of N_2 treatment were 400 W, 60 s and 300 sccm respectively. The initial and process temperatures of the SiO_2 deposition were ~380^oC and ~350^oC respectively. Adopting above process condition, the metal delamination easily occurred after W-plug deposition. The optical and SEM cross-sectional images in Figure 4-2-2 indicate that peeling appeared at the interface between the TiN barrier and FSG/SiO_2.

I. Effect of N_2 treatment on metal delamination

In order to realize the effect of N_2 treatment on the fluorine concentration at the surface of the USG capping layer, a compared process was implemented. A ~18 KÅ HDP-FSG layer was directly deposited on silicon substrate and followed by CMP until the thickness of the FSG films reached to ~6 KÅ. Then various N_2 plasma treatment conditions were performed and ~2 KÅ USG films were capped subsequently. The fluorine concentration at the USG surface was found to be strongly dependent on the

conditions of N_2 treatment, as shown in Table 4-3-1, in which the normalized fluorine concentration meant the 100-fold ratio of the fluorine concentration to the ^{28}Si concentration. Higher bias power or longer process time of N_2 treatment caused more fluorine content at the USG surface. It was also found that the bias power of N_2 treatment dominated over the treatment time in affecting the surface fluorine concentration of USG. At the same N_2 treatment time of 60 s, the higher bias power of 400 W led the surface fluorine concentration of USG to be 66% higher than that for the lower bias power of 300 W, while the bias power was controlled at 400 W, the longer treatment time of 60 s induced the surface fluorine concentration of USG only 32% higher than that for the shorter treatment time of 30 s.

Table 4-4-1 also summarizes the relationship between the various conditions of N_2 treatment and the incidence of the metal delamination. It was found that higher bias power and longer process time of N_2 treatment generated higher fluorine concentration at the USG surface resulting in higher probability of metal peeling. The results indicated that higher bias power and longer process time of N_2 treatment produced more actively fragmented fluorine species from the FSG films [73], and the unstable fluorine species diffused to the USG surface and then reacted with metal-stacked layer in subsequent thermal process. Furthermore, the surface fluorine concentration of USG decreased after annealing, however, the improvement of metal delamination was limited and peeling was still observed. The plausible reason was that the annealing process accelerated the unstable fluorine species to react with the TiN/Ti/Al layers leading to another peeling type.

Although the reduction of bias power and process time of N_2 treatment effectively

reduced the surface fluorine concentration of USG, the metal line delamination still randomly occurred in the processes. During the N_2 treatment with rf power, a negative voltage was exerted on the backside of the processing wafer; then the N_2 plasma had higher driving force to break the Si-F bonds of FSG films. Therefore, a feasible treatment needs to substitute for rf bias power to improve the stability of FSG films. As shown in Table 4-4-1, the adoption of plasma-enhanced N_2 treatment (PE-N_2) significantly decreased the surface fluorine concentration of USG resulting in the elimination of the metal delamination.

II. Effect of capping conditions on metal delamination

The FTIR Si-F peak intensity of the FSG films was found to be dependent on the initial deposition temperature of USG capping layers as shown in Table 4-4-2. Figure 4-4-3 shows the evolution of initial deposition temperature in different capping conditions, in which the cooling or pumping step inserted between the N_2 treatment and USG deposition was used to decrease the initial capping temperature. The Si-F peak intensity of the FSG surface was measured before and after annealing processes. The Si-F peak intensity increased after annealing when the initial deposition temperature of USG was estimated about 370~380°C. Slightly increase of the Si-F peak height after annealing was found when the initial capping temperature was about 360°C. In contrary, as initial capping temperature was 310~320°C, the Si-F peak height decreased after annealing. Interestingly, the occurrence of metal delamination showed strong correlation with the initial deposition temperature of USG. As the temperature was above 360^{o}C, serious peeling occurred on metal pads.

It was suggested that the actively fluorine species in the FSG films resulted from

high bias power and long process time of N_2 treatment or high initial deposition temperature of USG capping layers not only formed the Si-F bonds within the film, but also diffused to the USG surface, as shown in Figure 4-4-4. As the initial capping temperature of USG was higher than 380^{o}C, the trapped fluorine at the USG surface further induced the metal delamination after the subsequently metallization process. Figure 4-4-5 shows that a sharp fluorine peak occurred at the FSG/USG interface and highly fluorine concentration was present within the USG capping layer. In addition, the non-bonding fluorine was repaired to be the Si-F bond by thermal treatment. As shown in Table 4-4-2, the Si-F peak from FTIR spectra increased after annealing process.

On the other hand, when initial deposition temperature of USG was as low as 320^{o}C, the driving force was not enough for non-bonding fluorine to diffuse out. However, non-bonding fluorine bonded with Si to form the Si-F bond by the thermal energy at the beginning of USG deposition. Fluorine source was exhausted in USG/FSG surface resulting in no extra FTIR Si-F peak at the USG/FSG interface. As a result, the Si-F peak height decreased due to no additional fluorine to form Si-F bonds in following annealing process.

Moreover, it was found that using ex-situ USG deposition significantly decreased the Si-F peak after annealing (see Table 4-4-2) because the initial deposition temperature of USG was reduced to 300^{o}C. In expectation, this separated USG deposition method resulted in no metal line delamination.

To prevent the metal delamination, a modified process flow was proposed in Figure 4-4-6. Plasma-enhanced N_2 treatment and separated USG capping with the initial deposition temperature below 350 ^{o}C were used to broaden the process window. Based on

this new metallization process, a robust structure without metal peeling was obtained. Furthermore, the SIMS profile of Figure 4-4-7 shows that lower fluorine concentration was present in the USG film as compared with the result of Figure 4-4-5.

4-4-4 Summary

Fluorine stability was extremely important in HDP-FSG IMD application. In this study, the SIMS and FTIR results showed that high rf bias power and long process time of N_2 treatment or highly initial deposition temperature of USG capping layers generated actively fluorine species from the FSG films. The non-bonding fluorine species diffused to the USG surface and reacted with the subsequent Ti/TiN layer resulting in metal delamination. Plasma-enhanced N_2 treatment and separated USG capping with the initial deposition temperature below 350^{o}C by extra cooling step were found to be useful to prevent the metal delamination.

4-5-2 Integration of a Stack of Two Fluorine Doped Silicon Oxide Film with ULSI Interconnect Metallization

4-5-1 Motivation

As the minimum geometry in the integrated circuits (ICs) continues to shrink, Fluorine doped silicon oxide (FSG) film becomes an attractive solution for reducing the wiring capacitance in ultra large-scale circuits [107,115-117]. The FSG film has three (3) main advantages: First, it can be deposited both in an HDP-CVD (High-Density-Plasma Chemical Vapor Deposition) or conventional PE-CVD (Plasma Enhanced CVD) system

that become high quality and thermally stable films [75,84]. Second, FSG film can be integrated in a standard IMD (Inter-metal dielectric) architecture, due to the HDP-CVD FSG's gap-filling capability superiority over PEOX [76,77]. The combination of the two (2) processes for different FSG depositing systems, an HDP-CVD FSG film deposition to fill the inter-metal spacing followed by a capping layer deposited by PE-CVD FSG film is a feasible scheme, for both reliability and throughput. Third, the dielectric constant can be reduced from 4.2 of PE-CVD oxide film to 3.6 of FSG film, with a decreased capacitance between the lines [78,80].

In this study, we have integrated Fluorine doped silicon oxide film with a dielectric constant of 3.6 deposited using HDP-CVD and PE-CVD into sub-0.18 μm processes. We have optimized the HDP-CVD and PE-CVD processes for stable FSG film. The low dielectric constant inter-metal dielectric (IMD) was composed with the HDP-CVD FSG film for gap-filling and in the PE-CVD FSG layer for capping before the chemical mechanical polishing planarization. The HDP-CVD FSG layer's performance and PE-CVD FSG films were examined in terms of film properties and capability to be integrated in sub-micro devices.

4-5-2 Experimental Procedures

The HDP-CVD FSG films were prepared using an inductively coupled plasma CVD system with gas sources of SiF_4, SiH_4, O_2, and Ar. The substrate temperature was set at 420^{o}C**.** In the case of the PE-CVD FSG layers, the substrate temperature was 400^{o}C, deposited in a dual frequency (13.56 MHz and 350 kHz) PE-CVD system using $SiF_4/SiH_4/N_2O$ chemistry. Undoped silicon oxide (USG) films were also prepared by the

PE-CVD technique using SiH_4 and N_2O gas mixtures. The different refractive index (RI) of oxide films was deposited by adjusting the different gas ratio. The film's thickness and the FSG film's refractive index were measured using an elliposometer on 600 nm thick films deposited on Si wafer. The Si-F peak and F percentage were monitored by Fourier Transformation Infrared Spectroscopy (FTIR) (peak Si-F was about 930 cm^{-1}) and was calibrated with Rutherford Back Scattering (RBS). Film stress was measured with a Flexus stress gauge. The dielectric constant was measured using a mercury probe at 1 MHz. For the adhesion study, the FSG films were deposited on 0.2 μm USG/ 0.7 μm Al stack structure. In addition, the ability of fluorine diffusion was evaluated by a Secondary Ion Mass Spectrometry (SIMS) analysis using an oxide / FSG / oxide film sandwich structure. The capacitance reduction and via resistance at different metal widths and gaps were measured by using a two-layered Al metal structure deposited with 30 nm of Si-Rich oxide liner, 0.6 μm of HDP-CVD FSG layer, and a PE-CVD FSG 1.1 μm cap layer followed by CMP polish.

4-5-3 Results and Discussions

I. Adhesion Testing

It is well known that fluorine is an active atom, which reacts easily with other elements. Therefore, a risk of corrosion caused by fluorine exists when applying FSG film in integration on IC production. In order to verify this, the corrosion properties were investigated by depositing a FSG film stack on a TiN / AlCu / TiN / oxide layer/ Silicon substrate. No abnormal image was observed by the Optical Microscopy (OM) and SEM after depositing the FSG film. However, bubble-like defects were found following a

410^{o}C thermal test and can be seen in Figure 4-5-1. This seems to indicate some bonding was destroyed or weakened by the thermal-induced reaction. A cross-sectional analysis revealed observed peeling at the metal-FSG interface. Further evidence came from the Secondary Ion Mass Spectrometry (SIMS) analysis (shown in Figure 4-5-2), which indicates fluorine diffused into the TiN layer after the thermal treatment; indicating that a reaction between the fluorine and TiN took place forming a TiFx compound and the TiFx was desorbed. This desorbed species became trapped beneath the FSG film and decreased its adhesion ability, leading to blistering. SIMS analysis (not shown) also indicates the thermal cycle was the dominant factor on fluorine stability. The fluorine retains stability and will not diffuse out after deposition. By thermal treatment (the temperature is 410 ^{o}C in this experiment), fluorine will diffuse into the metal layer and react with Ti and form TiFx. As noted in Figure 4-5-3, the stress changes after the 410^{o}C thermal test also demonstrates this evocation. It exhibited that no stress change occurred for the FSG / TiN / AlCu / TiN / oxide layer even after 1 month in an air environment. Further, after thermal cycling at 410^{o}C, stress would change, which suggests that at elevated temperatures, a reaction may occur.

Because the IC process possesses many thermal budgets, the implication is that a good barrier layer is required to prevent the fluorine from diffusing into the metal layer. As a result, the varying oxide films were deposited in Plasma-Enhanced CVD by changing the SiH_4/N_2O ratio to evaluate the efficiency of the fluorine barrier effect. Figure 4-5-4 shows the different oxide layer and HDP-CVD FSG layer's SIMs profile. The results showed that the higher the Si concentration is in oxide films, the better its ability is to block F diffuse out. As a result, Silane-based silicon rich oxide film (SRO,

refractive index was 1.5, O:Si ratio < 2:1) was recognized as good fluorine barrier against diffusing out. The diffusing depth was about 20 nm SRO film containing a substantial number of unterminated silicon bonds, which quickly got free fluorine to form Si-F bonds. A 30 nm silicon-rich oxide film prior to HDP-CVD FSG film deposition was shown to be an effective solution to solve metal corrosion issue. No corrosion was demonstrated before and / or after the alloy process tests for the TiN / ALCu / TiN/30 nm Si-Rich oxide / FSG scheme.

II. The physical priorities of FSG film

In ultra large-scale single damascene technology, the HDP-CVD FSG has two (2) functions; providing low-dielectric constant films and achieving gap-filling capability. Using full HDP-CVD FSG film as IMD layer was an expensive and time-consuming HDP process because of the simultaneous sputter and deposition. From the manufacturing viewpoint, the full HDP-CVD FSG scheme was assessed as a low-throughput. As a result, the stack film makes of 0.6 μm thick HDP-CVD FSG film and followed deposited with 1.1μm thick PE-CVD FSG films seems to be an acceptable solution for the global interconnect scheme. The fundamental HDP-CVD FSG and PE-CVD FSG film's properties are detailed listed in Table 4-5-1. The fluorine concentration was chosen as 4.5 at% for HDP-CVD FSG films and 6.0 at% for PE-CVD FSG films.

As shown in Table 4-5-1, the PE-CVD FSG film's stress was more compressive, which is suitable for multi-layered metallization. Since the stress of the deposition film is essential for implementing the film as an IMD layer. Too low or large stress of the IMD film would induce integration problems. Figure 4-5-5 shows the crack SEM image for

implementing full HDP-CVD FSG film as an IMD layer. Depending on the IMD crack location, the HDP-CVD FSG film's low compressive stress was suspected to be the root cause that induced the IMD crack in multi-layer metallization. Two (2) main factors were used to improve the HDP-CVD FSG layer's film compressive stress. There were limited improvements. One was reducing deposition temperature. This had an unstable fluorine side effect. The other was decreasing the concentration in the FSG film, which downgraded the effect of lower dielectric constant material. The stress hysterisis curve for full HDP-CVD FSG and stack films are showed in Figure 4-5-6. The stress deviations were 1.2E8 dynes/cm^2 and 3.0E8 dynes/cm^2 for HDP-CVD FSG films and stack FSG layers, respectively after the 1st 500^{o}C thermal cycle. Higher stress hysterisis for stack layers implies that the film does change due to the combination of two (2) types of FSG films. The stress hysterisis was almost zero after the 2nd 500^{o}C thermal cycle. It also indicated that the stress (-1.2E9 dynes/cm^2, compressive) will be higher for HDP-CVD FSG and PE-CVD FSG film's stack layers after a 500^{o}C thermal cycle. That is, the stack films compensate the multi-layers metallization tensile stress, which reduces film crack in integration. By a long-time trace after adapting a stack of two (2) FSG films, no crack was found for the stack film scheme.

III. Integration Features

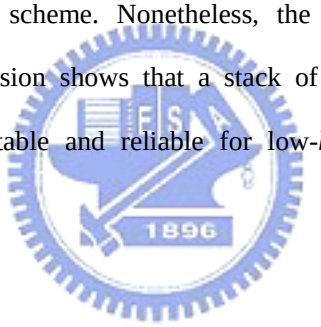
A partial integrated structure with the vias hole is reported in Figure 4-5-7. The via hole's critical dimension (CD), dry etch rate and chemical mechanical polishing rate has been listed in Table 4-5-2. The CD showed no significant differences for the two (2) different schemes. The via etch had been performed using the Applied Materials HDP etcher system. The etching rate was measured at 143.2 nm / min. HDP-CVD FSG film,

and 158.3 nm / min. for the PE-CVD FSG layers. In comparison, the undoped PEOX and PETEOS film etch rate was measured at 140.5 nm /min. This is lower than the FSG layer's. In a FSG film's stack, the mechanical polishing process was performed on PE-CVD FSG film. The PE-CVD FSG film's polishing rate (289.6 nm /min) was 40 nm and 60 nm higher than those of the HDP-CVD FSG layer and undoped PE-CVD oxide film on a blanket wafer. The same trend was found on pattern wafers. That is, it is as beneficial for improving throughput as taking two (2) stack FSG films as the IMD scheme. Considering the global planarization's effect, the HDP-CVD FSG layer's profile on control wafer would collapse at 85 mm from the wafer edge. This is because the smaller chamber spacing for the HDP-CVD hardware design was limited. However, no such phenomenon was found with PE-CVD FSG film, as shown in Figure 4-5-8. The 5th interlayer FSG film's edge profile was in a pattern wafer after CMP process, the collapse location on wafer's edge was extended from 85 mm to 95 mm (shown in Figure 4-5-9), which provides an improvement in total wafer edge yield.

IV. The capacitance reduction and via resistance

Because the purpose of using low-*k* materials is to reduce the capacitance for smaller geometry, the capacitance reduction will directly influence the device's performance. The line to line capacitance of patterns with different FSG IMD structures was measured at different metal widths and gaps. The line to line capacitance reduction for the stack FSG films varies with the metal spacing is shown in Figure 4-5-10. It indicates that wider metal spacing has a smaller impact than the thinner metal spacing on the line-to-line capacitance. The larger capacitance observed at wider metal spacing is the result of a larger fringe capacitance between the wider metal spacing. Comparing with

different inter-metal schemes with different metal spacing / widths, it shows that Si-rich oxide with 30 nm thickness was induced to decrease average line to line capacitance reduction from 12% to 10-11%. In addition, in comparing the full HDP-CVD FSG layer and stack layers, the line to line capacitance reduction was found comparable, which achieves a 10-11% reduction when compared to undoped silicon oxide film. A stack of FSG film's via resistance needs to be investigated to ensure that a stack of FSG scheme can be processed without affecting the via yield. The different IMD layer's via resistance at a different via hole is also checked. If compared with the full HDP-CVD FSG case, Rc_via for IMD consisted of a stack of HDP-CVD and PE-CVD FSG that was comparable with a full HDP-FSG scheme. Nonetheless, the Rc-via's variation is considered insignificant. The conclusion shows that a stack of HDP-CVD FSG and PE-CVD FSG film as IMD is suitable and reliable for low-*k* applications on the sub-micron processes.



4-5-4 Summary

The stack made of 0.6 μm thick HDP-CVD FSG film for gap-filling and followed by capping with 1.1 μm PE-CVD FSG films is a good compromise to fill narrow gaps between metal lines, to reduce the capacitance in the plane and between metal levels, and to optimize the throughput on a global isolation structure. Additionally, to prevent poor adhesion due to fluorine diffuse into metal layer, 30 nm thick SRO film was deposited prior to HDP-CVD FSG film. It has successfully demonstrated promising film properties as well as easy drop-in device and process integration feasibility for IMD applications in sub-0.18μm generations. No significant issue has been shown to realize the partial

integration of FSG films. On the other hand, implementing a stack of FSG layers as the IMD for the interconnect of the 0.18 μm generation exhibited 10-11% gain in the ring-oscillator's RC delay. Based on the electrical and reliability test results, it is believed that this stack deposited of HDP-CVD FSG film capped with a PE-CVD FSG layer is a good candidate for advanced sub-micro intermetal dielectric.

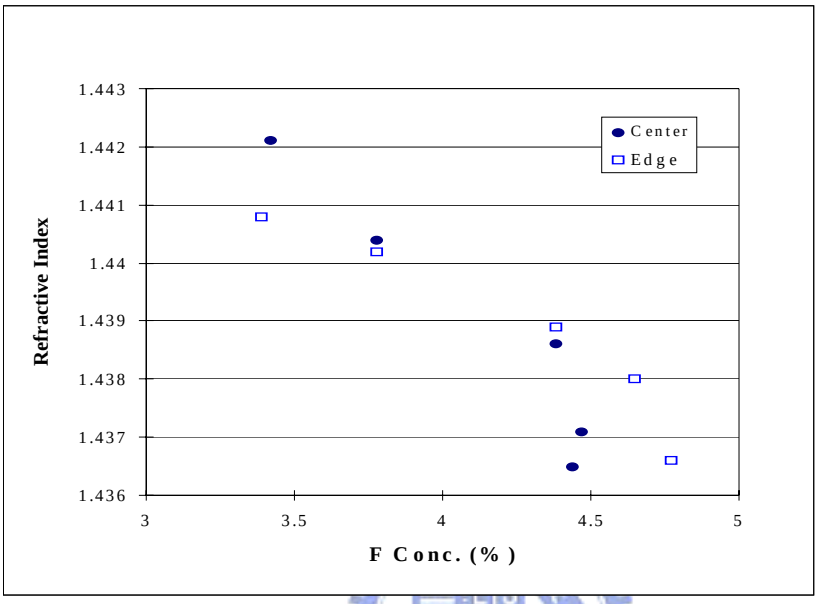


Figure 4-1-1. The R.I. of FSG films with different F concentrations at the center and the edge of wafers.

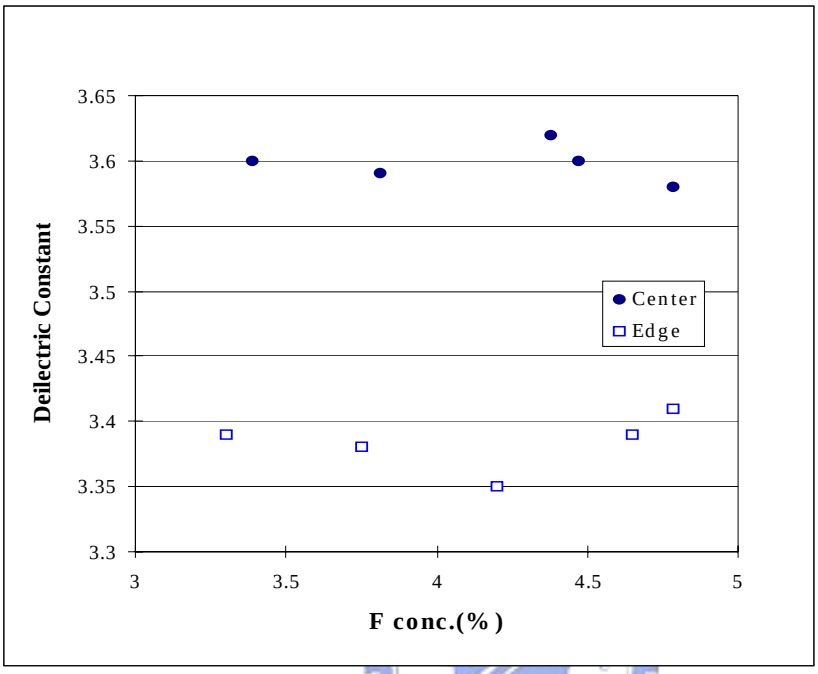


Figure 4-1-2. The DK of FSG films with different F concentrations at the center and the edge of wafers.

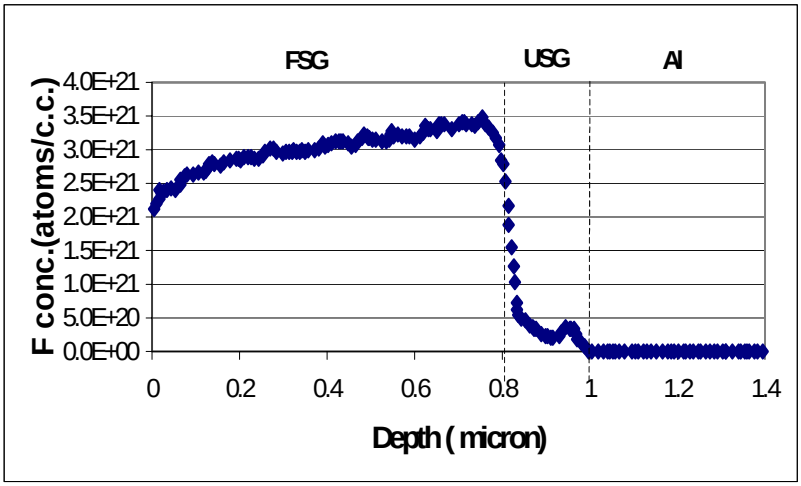


Figure 4-1-3. The F concentration of FSG film without cap layer after PCT for 2 hrs. and annealing at 400°C for 3 hrs.

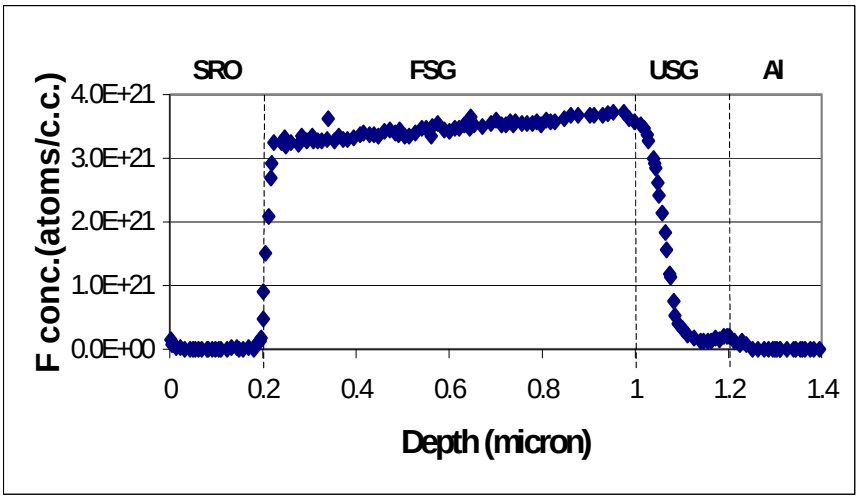


Figure 4-1-4. The F concentration of FSG film with SRO cap layer as deposited.

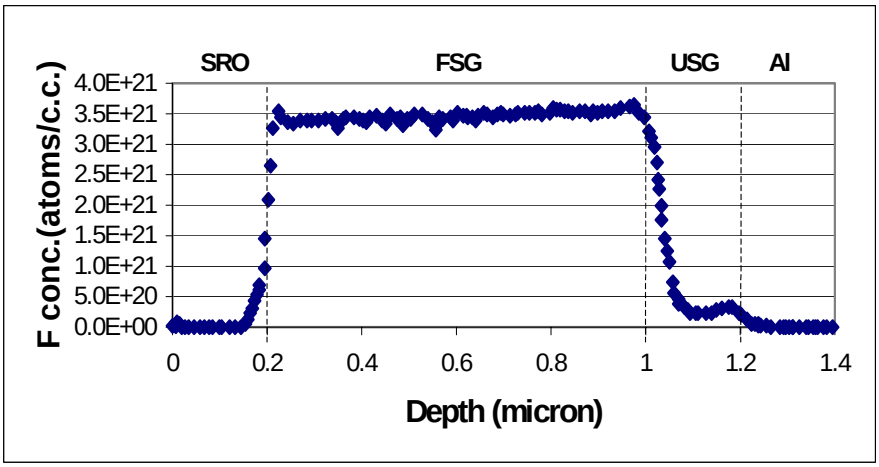


Figure 4-1-5. The F concentration of FSG film with SRO cap layer after annealing at 400°C for 3 hrs.

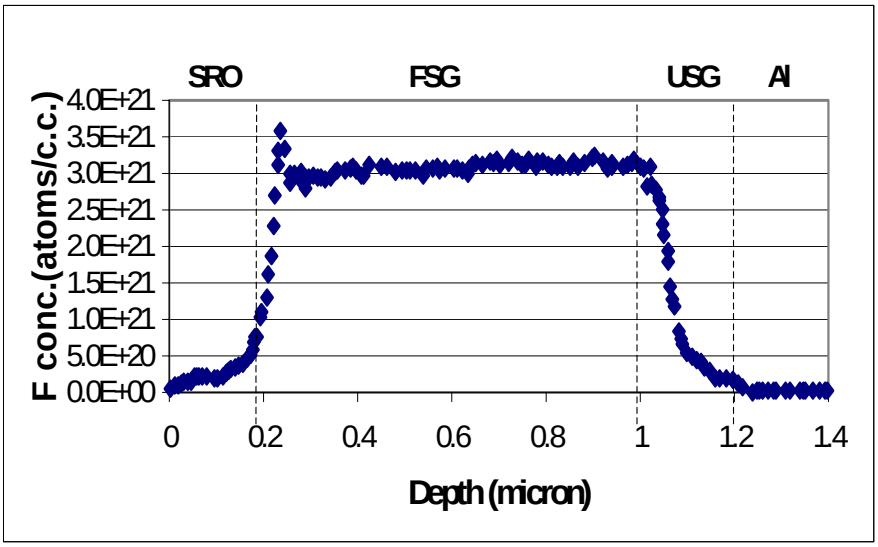


Figure 4-1-6. The F concentration of FSG film with SRO cap layer after PCT for 2 hrs. and annealing at 400°C for 3 hrs.

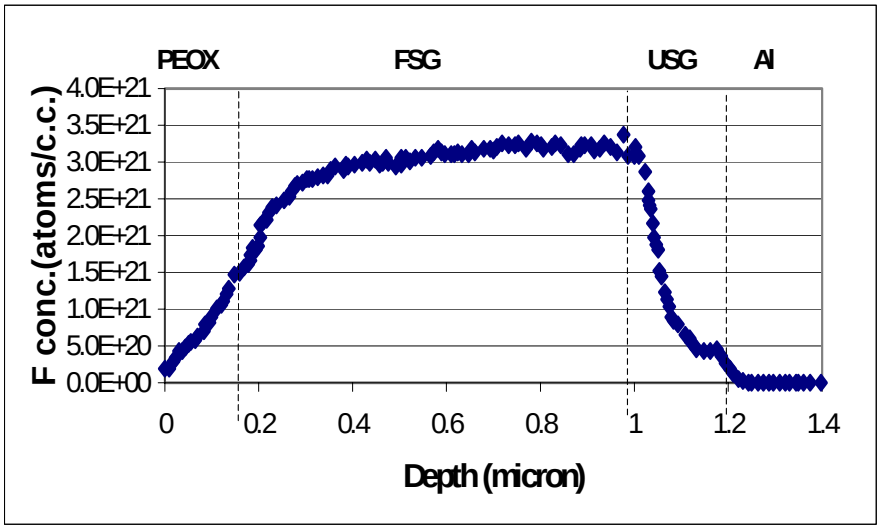


Figure 4-1-7. The F concentration of FSG film with PEOX cap layer after PCT for 2 hrs. and annealing at 400°C for 3 hrs.

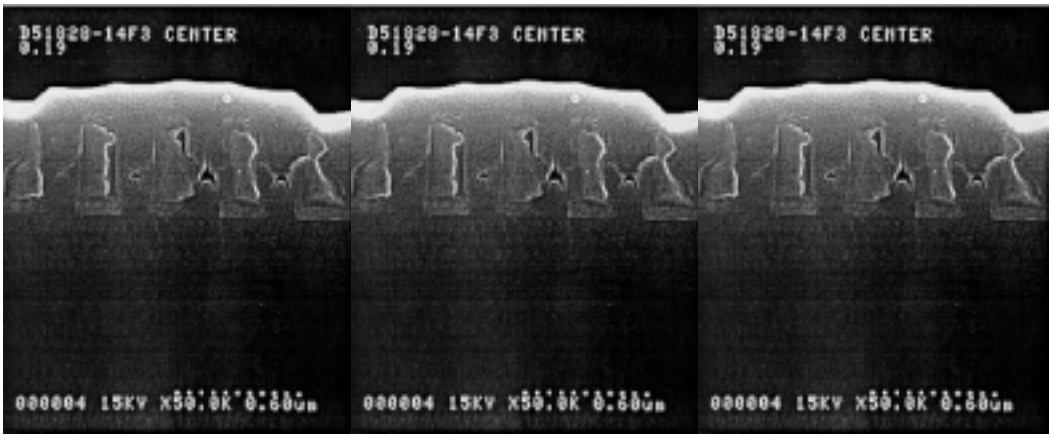


Figure 4-1-8 Different Patterns at Center of the wafer

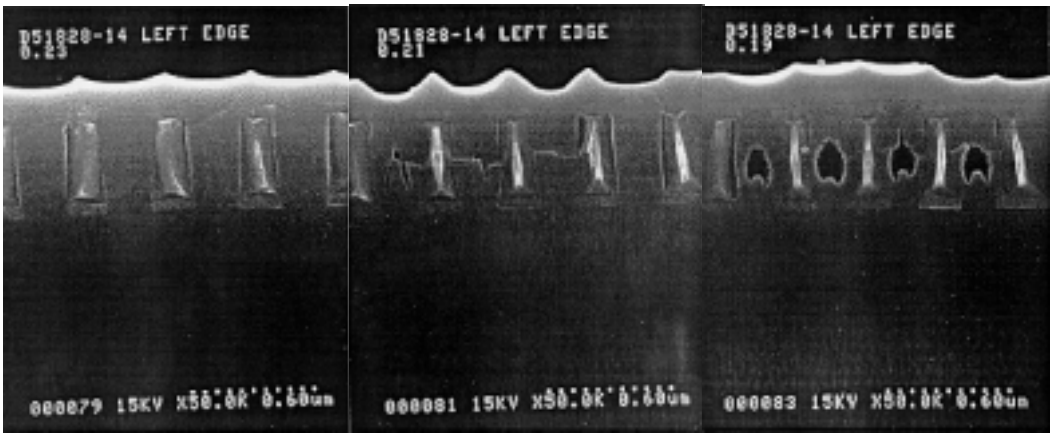


Figure 4-1-9 Different Patterns at Edge of the wafer

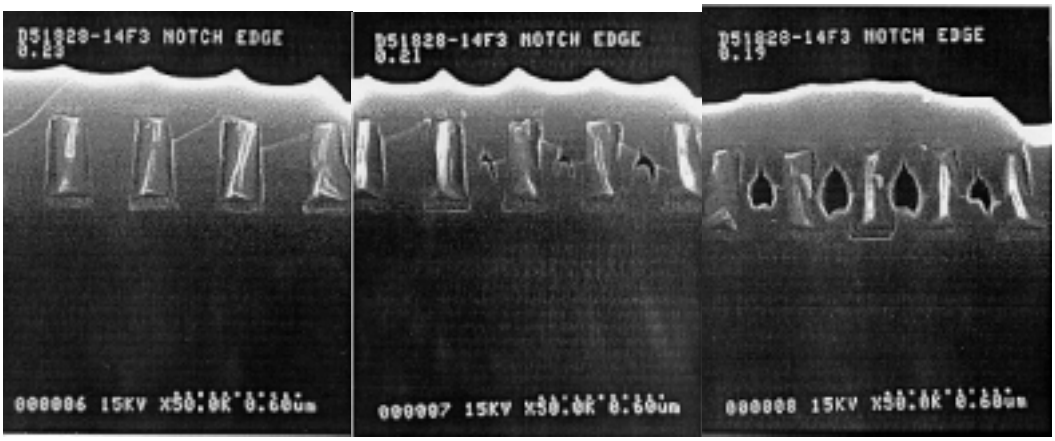


Figure 4-1-10 Different Patterns at Notch of the wafer

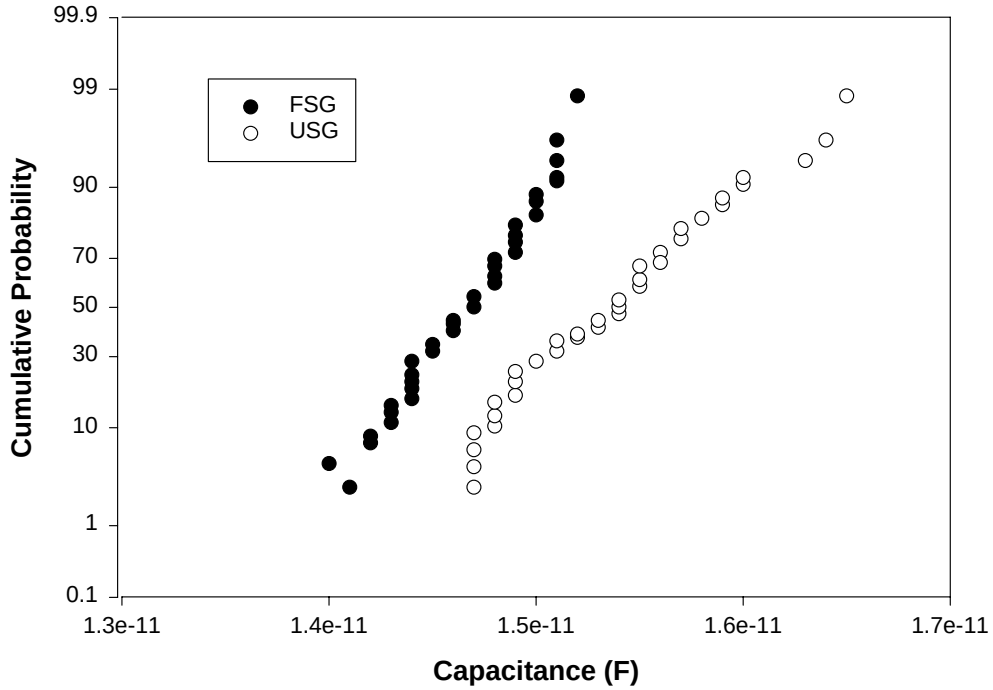


Figure 4-1-11. Line-to-line capacitance of FSG and USG for a 0.23/0.23 metal structure.

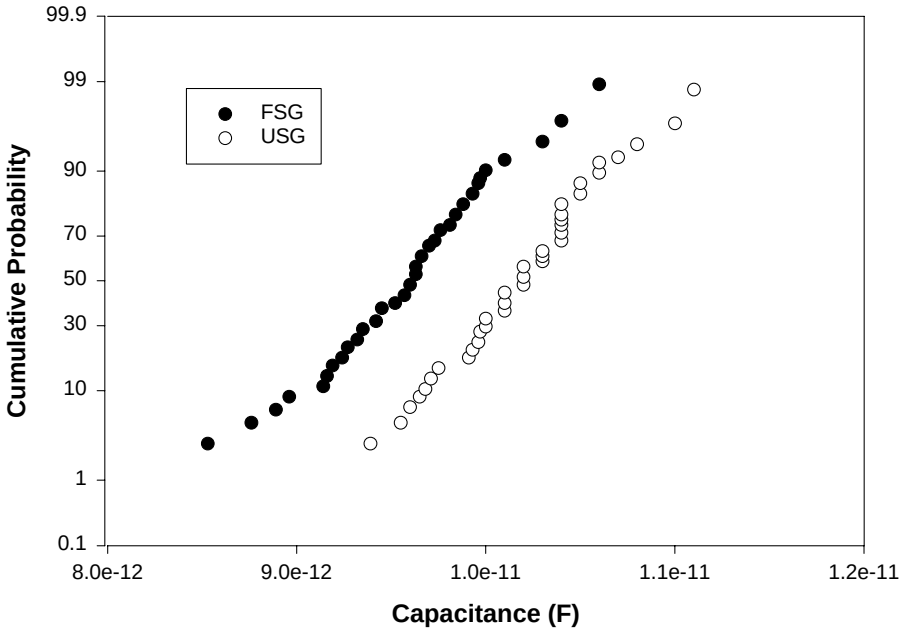


Figure 4-1-12. Line-to-line capacitance of FSG and USG for 0.23/0.46 metal structure.

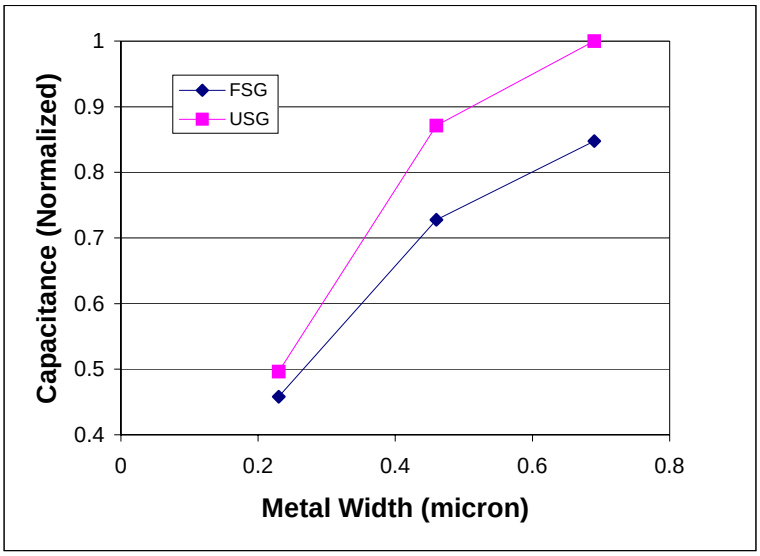


Figure 4-1-13. Normalized line-to-line capacitance of FSG and USG for different metal structure with 0.23 μm gap.

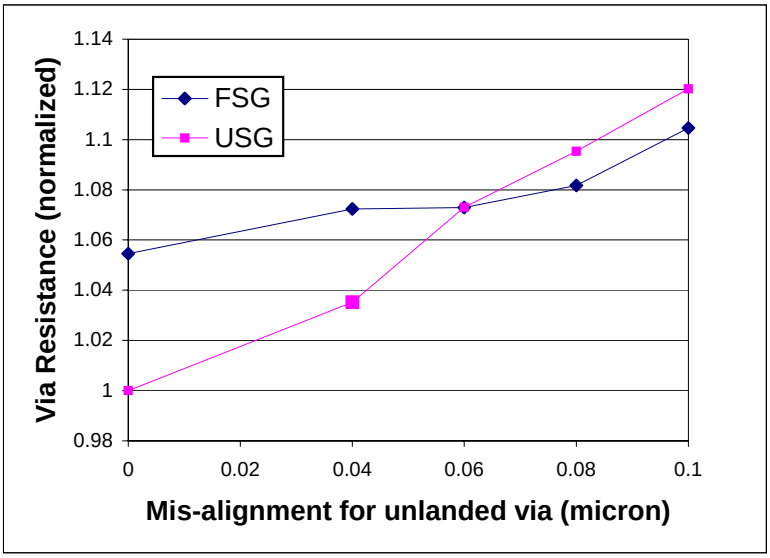


Figure 4-1-14. Normalized via resistance of FSG and USG for different mis-alignment of 0.26 μm via.

Table 4-2-1. The property of FSG film trends at 350°-450°C deposition temperature

		Deposition Rate	Fluorine Concentration % at. F	Dielectric Constant *k*	Refractive index RI	Stress	Wet Etch rate WER	Hardness H
Deposition Temperature	⇧	⇩	⇩	⇧	⇧	⇧	⇧	⇧

Table 4-2-2. The effect of deposition temperature on gap-filling parameters of FSG process.

Deposition Temperature (°C)	Deposition rate D (Å/min)	Sputter Rate S (Å/min)	Etch Rate E (Å/min)	E/(S+E)	E/S	D/(S+E)	D/S	D/E	E/S
350	3607	1541	1011	0.396	0.656	1.374	2.341	3.568	0.656
375	3553	1548	1028	0.399	0.656	1.340	2.295	3.456	0.664
400	3506	1553	1067	0.407	0.687	1.300	2.258	3.286	0.687
425	3480	1538	1080	0.412	0.702	1.291	2.263	3.223	0.702
450	3393	1542	1112	0.419	0.721	1.241	2.200	3.052	0.721

Table 4-2-3. TDS analysis for FSG films with varying deposition temperatures.

Deposition Temperature (^oC)	350	400	425	450
Ar onset of evolution (^oC)	450	455	445	467
Ar peak pressure (10^{-7} Torr)	0.1	0.1	0.1	0.1
H_2O onset of evolution (^oC)	452	467	467	520
H_2O peak pressure (10^{-7} Torr)	1.0	1.0	1.0	0.5
F onset of evolution (^oC)	435	450	467	490
F peak pressure (10^{-7} Torr)	1.0	1.0	1.0	0.5
HF onset of evolution (^oC)	410	420	450	467
HF peak pressure (10^{-7} Torr)	1.0	1.0	1.0	0.5

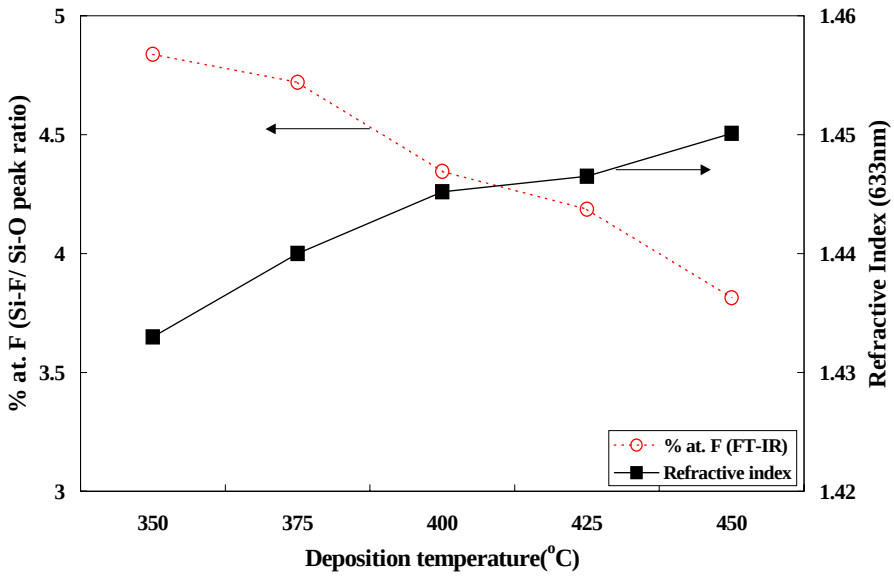
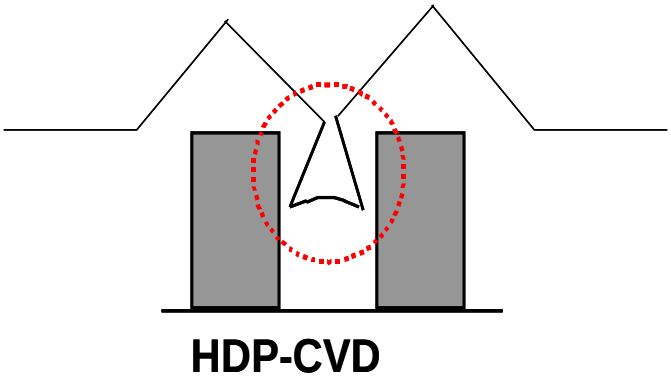


Figure 4-2-1. The effect of deposition temperature on the concentration of fluorine and refractive index for FSG film.

(a)



(b)

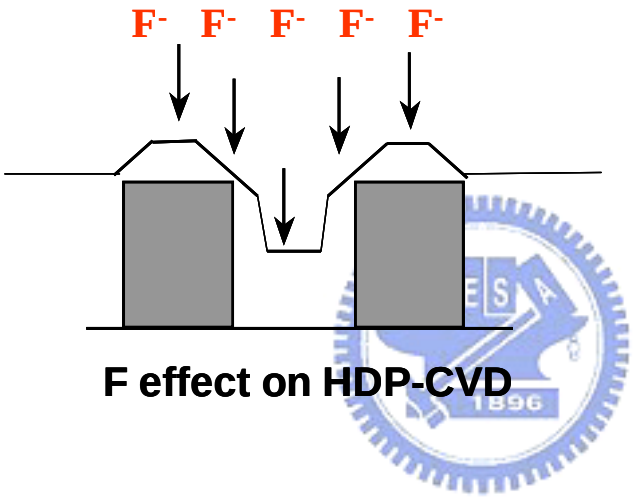


Figure 4-2-2. The concept of HDP-CVD gap-filling: (a) HDP-CVD, (b) F doped HDP-CVD.

(a) (b)

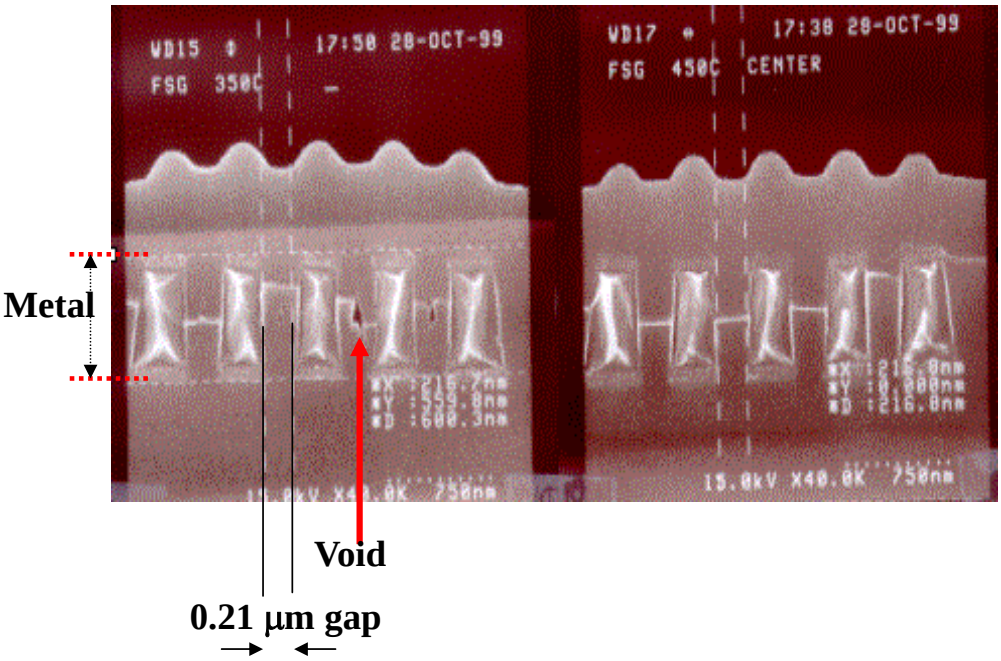


Figure 4-2-3. SEM image of FSG film for checking gap-filling (Height /gap=0.6 μm / 0.21 μm): (Left) 350°C, (Right) 450°C.

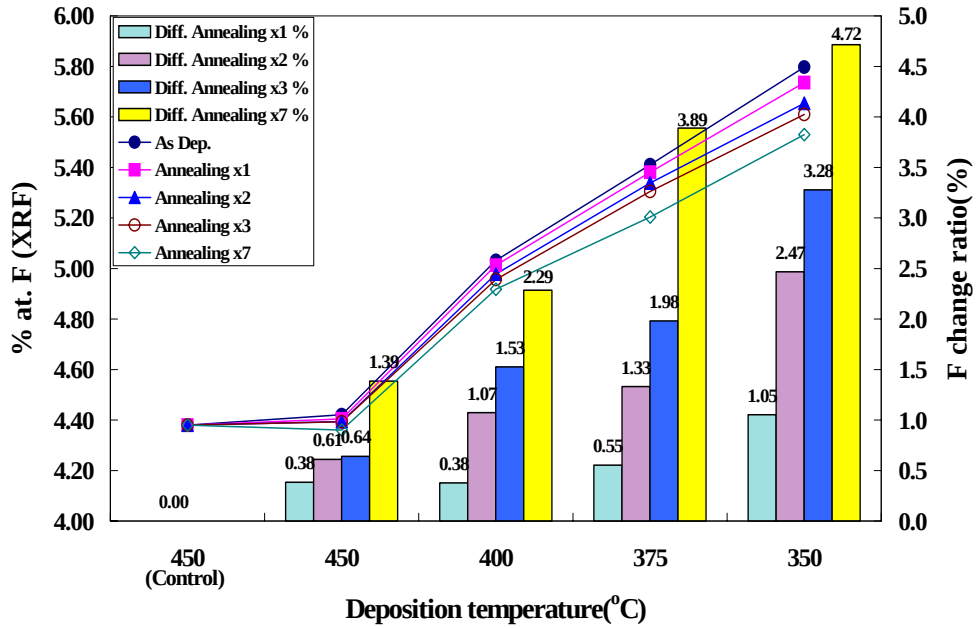


Figure 4-2-4. The difference of XRF of FSG films with varying deposition temperature.

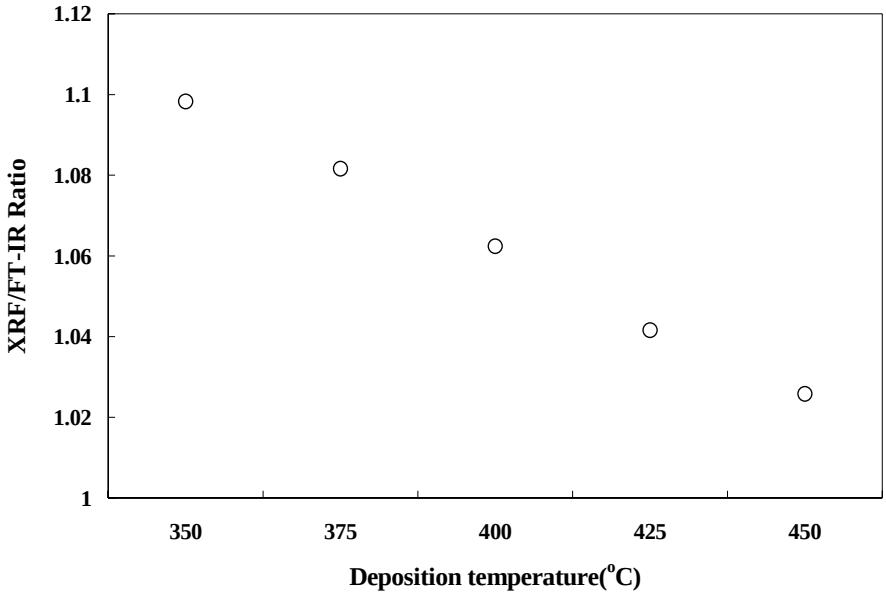
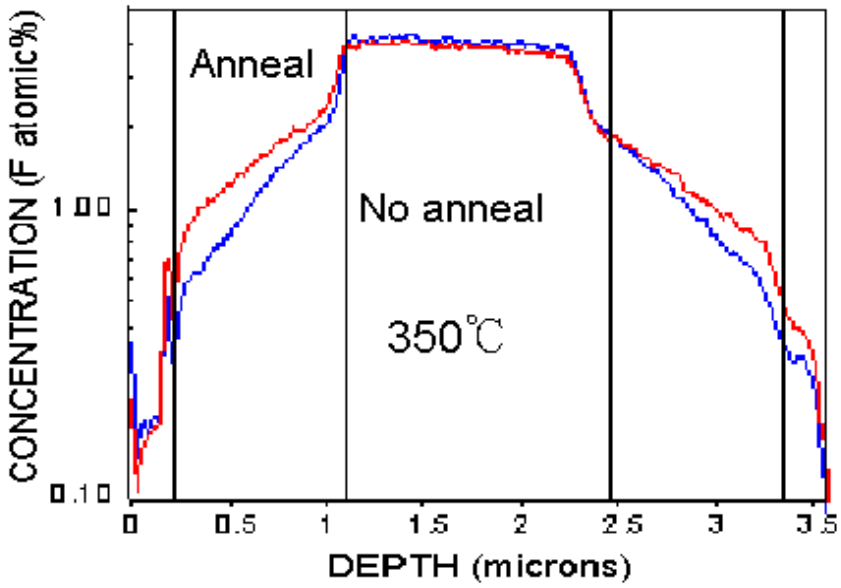


Figure 4-2-5. XRF/FTIR ratio of FSG films with varying deposition temperature.

(a)



(b)

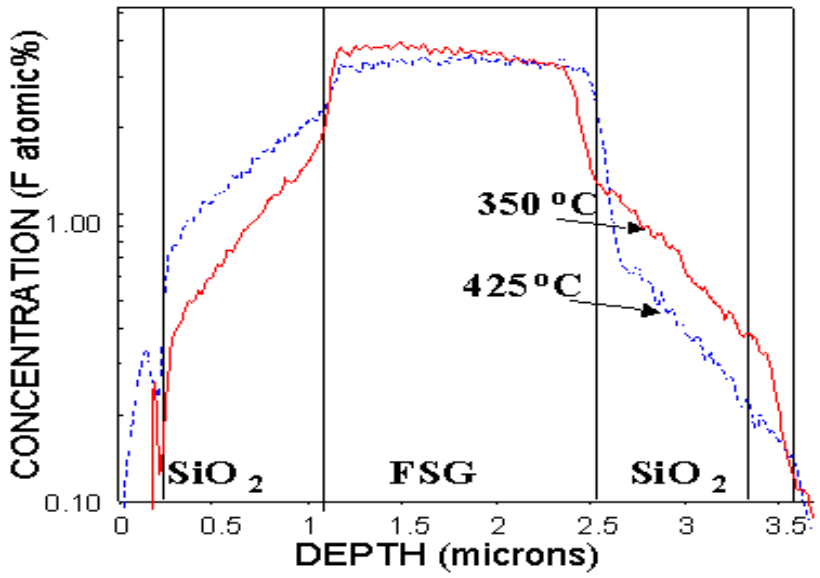
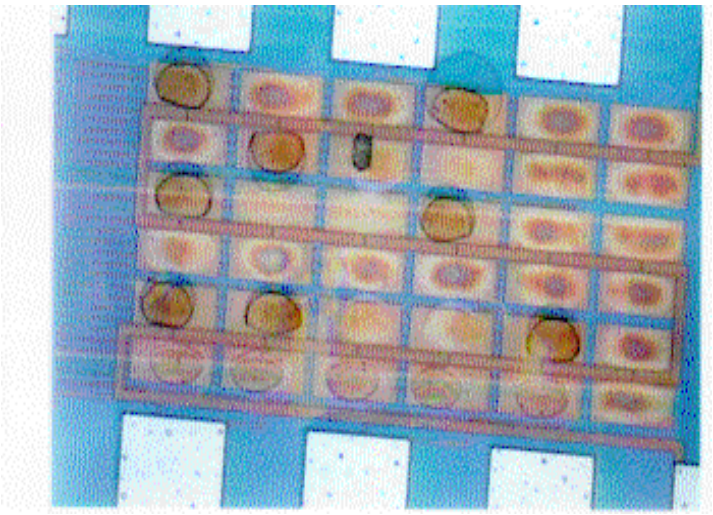


Figure 4-2-6. SIMS profile of FSG film: (a) Annealing effect (Deposition temperature=350 ^{o}C), (b) Deposition temperature effect.

(a)

.



(b)

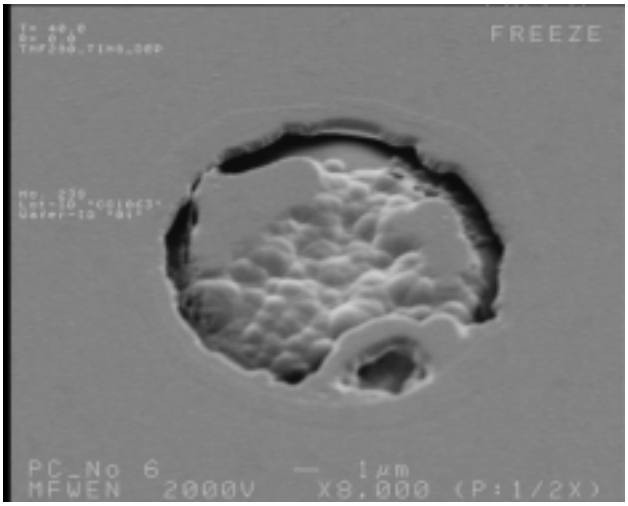


Figure 4-2-7: Integration problems of FSG film with 350^{o}C deposition temperature: (a) Optical microscope image of bubble defect on Al pad, (b) SEM image of film peeling.

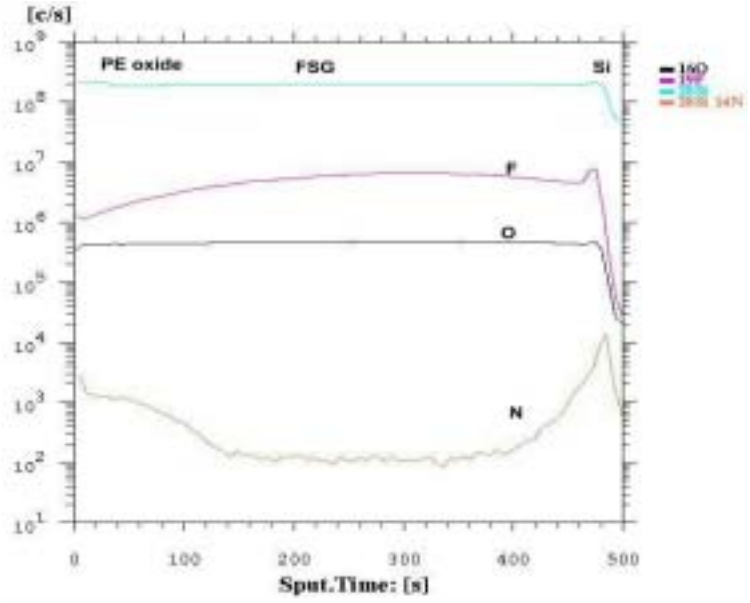


Figure 4-3-1. SIMS depth profile on PE oxide capped FSG film. F diffused out to PE oxide after annealing.

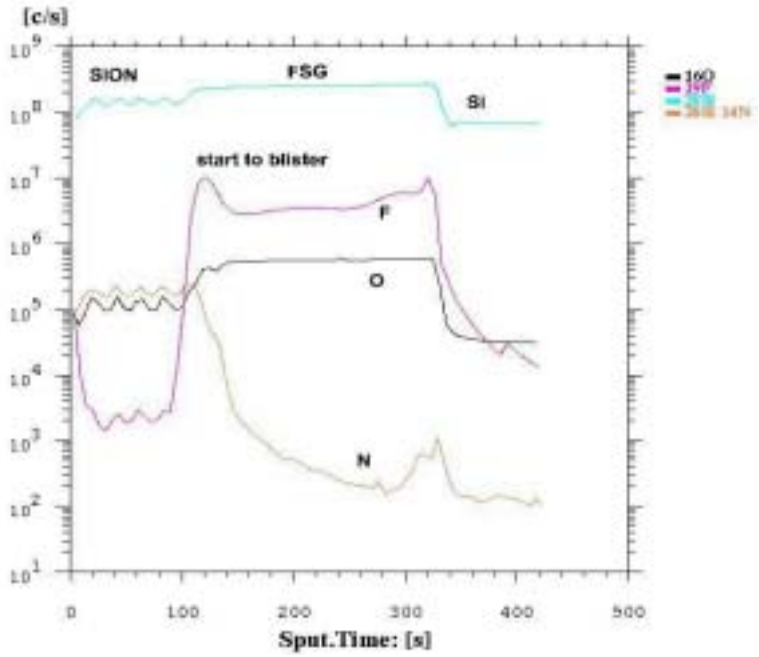


Figure 4-3-2. SIMS depth profile on SiON capped FSG film. Less F diffused out to SiON film was observed.

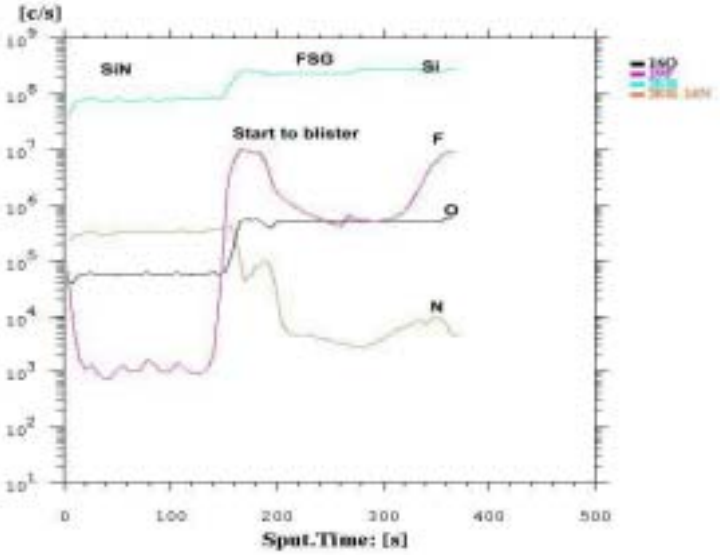


Figure 4-3-3. SIMS depth profile on SiN capped FSG film. Less F diffused out to SiN film was observed.

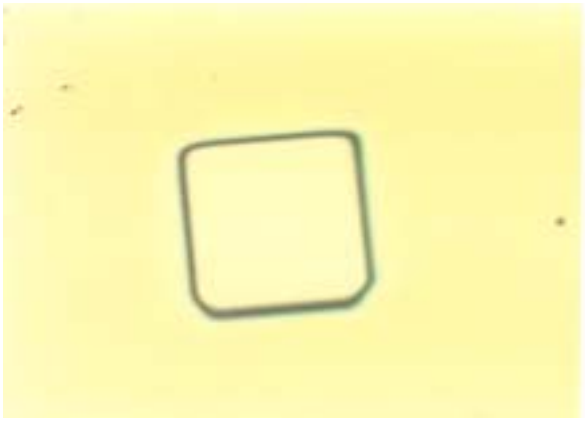


Figure 4-4-4. OM image of SIMS ion gun sputtered crater on PE oxide capped FSG film.

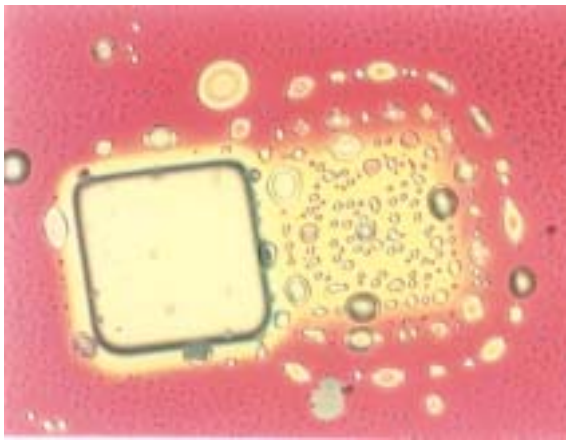


Figure 4-3-5. SIMS ion gun sputtered crater on SiON capped FSG film. Around the crater, serious film blister was observed.

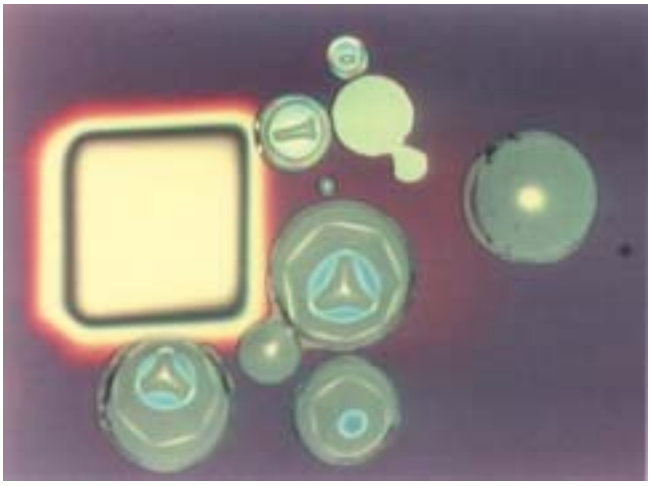


Figure 4-3-6. SIMS ion gun sputtered crater on SiN capped FSG film. Around the crater, serious film blister was observed.

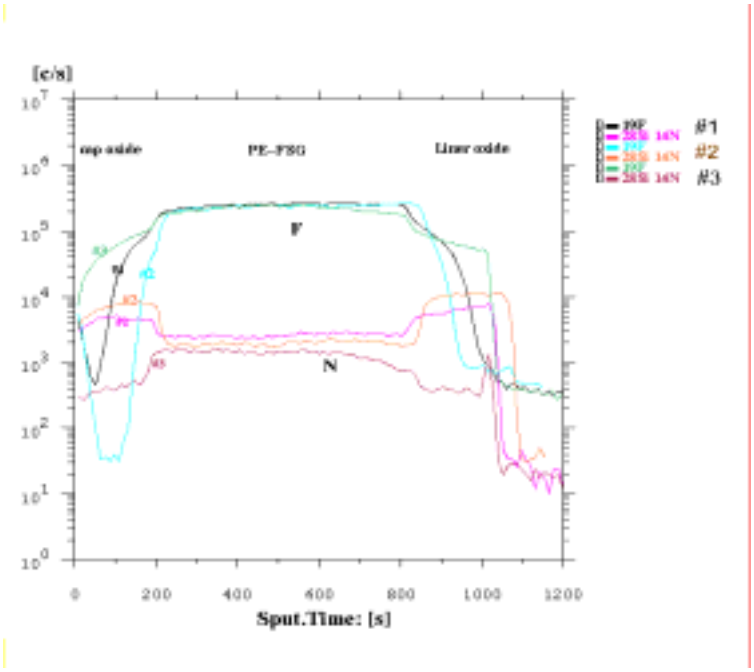


Figure 4-3-7. SIMS analysis on sandwich structure, SRO/FSG/SRO film. Different F diffusion phenomena were observed with different SRO capping material.

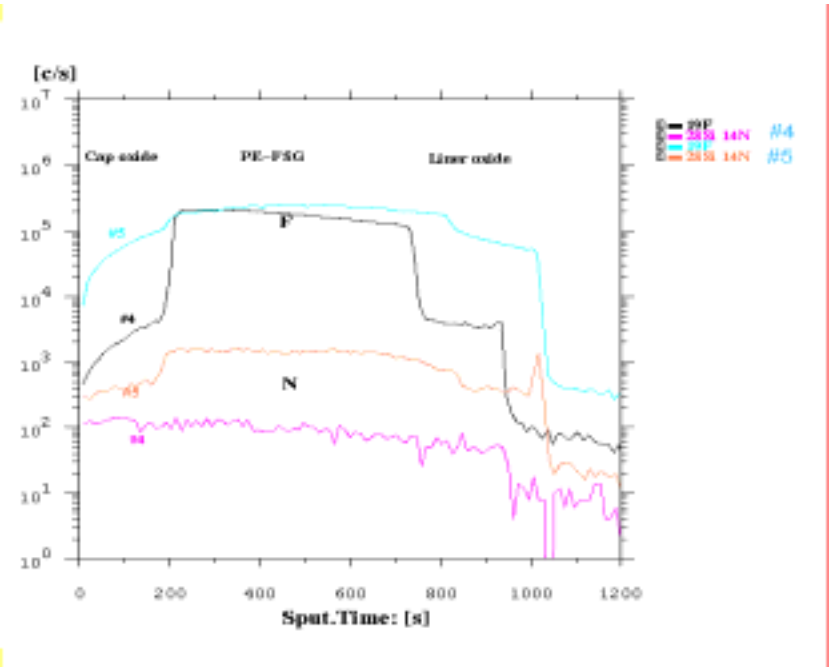


Figure 4-3-8. SIMS analysis on sandwich structure, SRO/FSG/SRO film. With much more N in FSG film, the F diffusion out to SRO was also much more seriou.

Table 4-4-1. Normalized fluorine concentration by TOF-SIMS analysis and metal delamination incidence for various N_2 treatment conditions.

Conditions			TOF-SIMS [F]	Delamination results
N_2 treatment	**Capping layer**	**Annealing**		
400W/60s	In-situ HDP-USG dep.	No	191	Peeling
400W/45s	In-situ HDP- USG dep.	No	156.2	Peeling
400W/30s	In-situ HDP- USG dep.	No	129.9	Peeling
400W/10s	In-situ HDP- USG dep.	No	100.5	Slight Peeling
350W/60s	In-situ HDP- USG dep.	No	102	Peeling
300W/60s	In-situ HDP- USG dep.	No	64.6	Slight Peeling
250W/65s	In-situ HDP- USG dep.	No	38.5	No Peeling
400W/60s	In-situ HDP- USG dep.	Yes	138	Peeling
PE-N_2 (300W/60s)	In-situ HDP- USG dep.	No	33.6	No Peeling

Table 4-4-2. FTIR results and metal delamination incidence for various USG capping conditions.

Conditions			FTIR Δ Si-F peak height	Initial USG dep. temperature (^{0}C)	Delamination results
N_2 treatment	Capping layer	Annealing			
400W/60s	In-situ HDP- USG dep.	No	0.105	~380	Peeling
400W/60s	In-situ HDP- USG dep.	Yes	0.204	~380	Peeling
400W/60s	Pump 20 s + In-situ HDP- USG dep.	Yes	0.058	~360	Slight Peeling
400W/60s	Cooling 10 s + In-situ HDP- USG dep.	Yes	-0.082	~340	No Peeling
400W/60s	Cooling 30s + In-situ HDP- USG dep.	Yes	-0.088	~320	No Peeling
400W/60s	Ex-situ HDP- USG dep.	Yes	-0.116	~310	No Peeling
300W/60s	In-situ HDP- USG dep.	Yes	-0.095	~320	No Peeling
PE-N_2 (300W/60s)	Ex-situ HDP- USG dep.	Yes	-0.121	~310	No Peeling

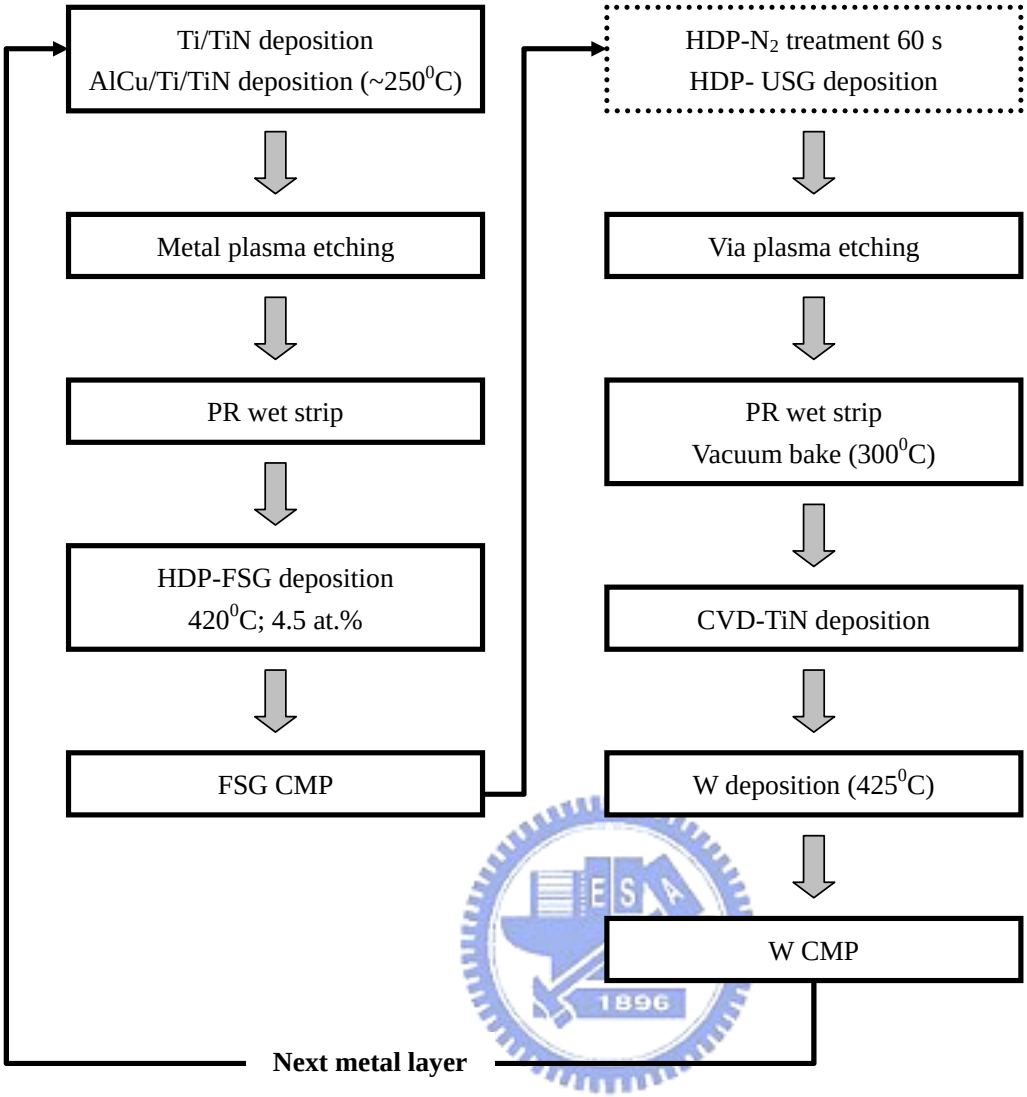
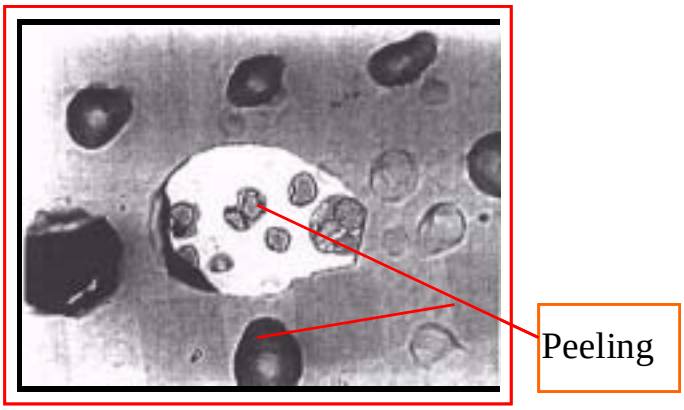


Figure 4-4-1. Repeating process flow for Al/Cu metallization.

(a)



(b)

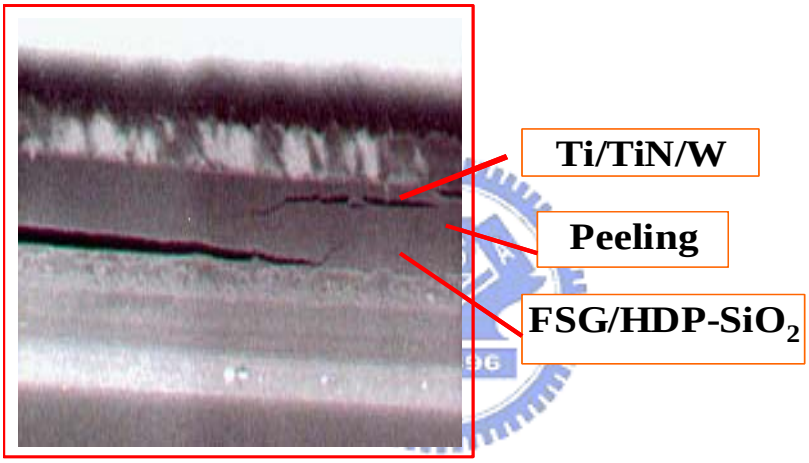


Figure 4-4-2. (a) OM and (b) SEM images of metal delamination.

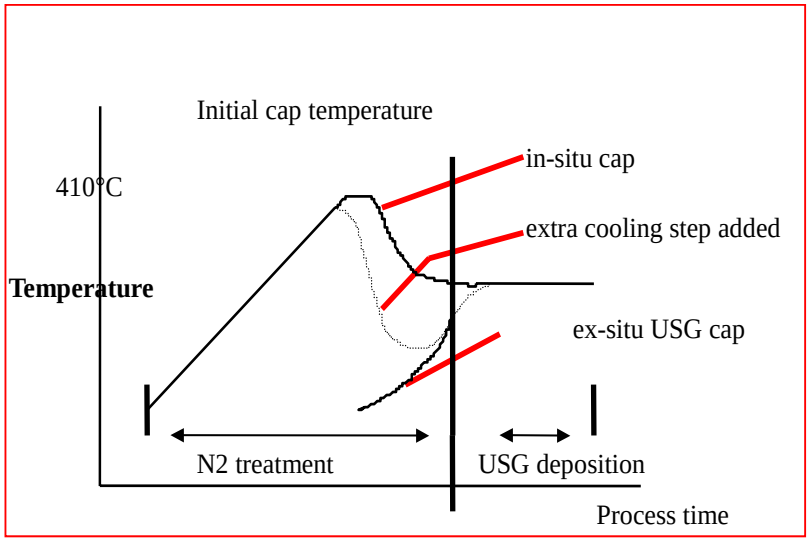


Figure 4-4-3. Evolution of initial deposition temperature in different USG capping conditions.

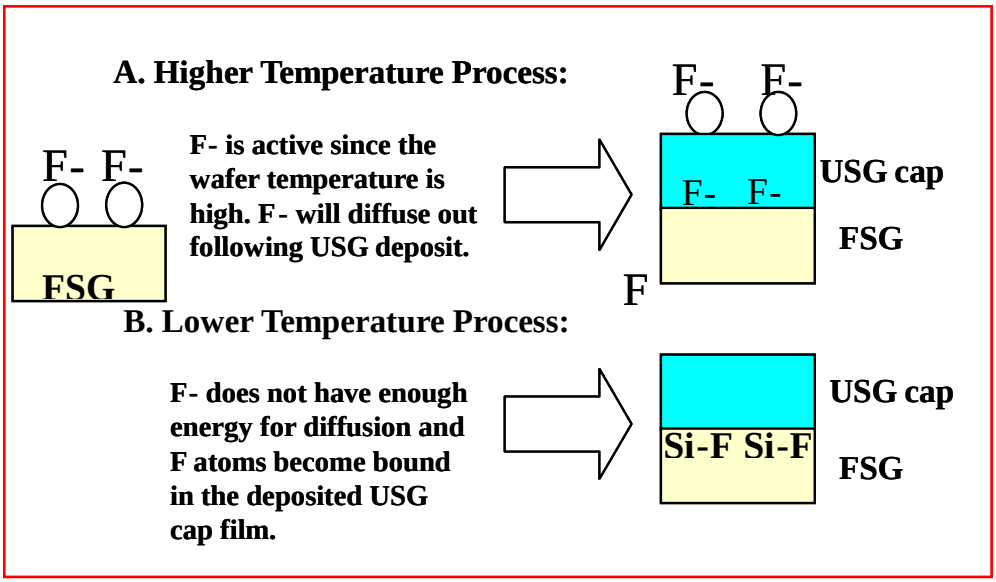


Figure 4-4-4. Proposed mechanism of fluorine diffusion under different initial deposition temperature of USG capping layers.

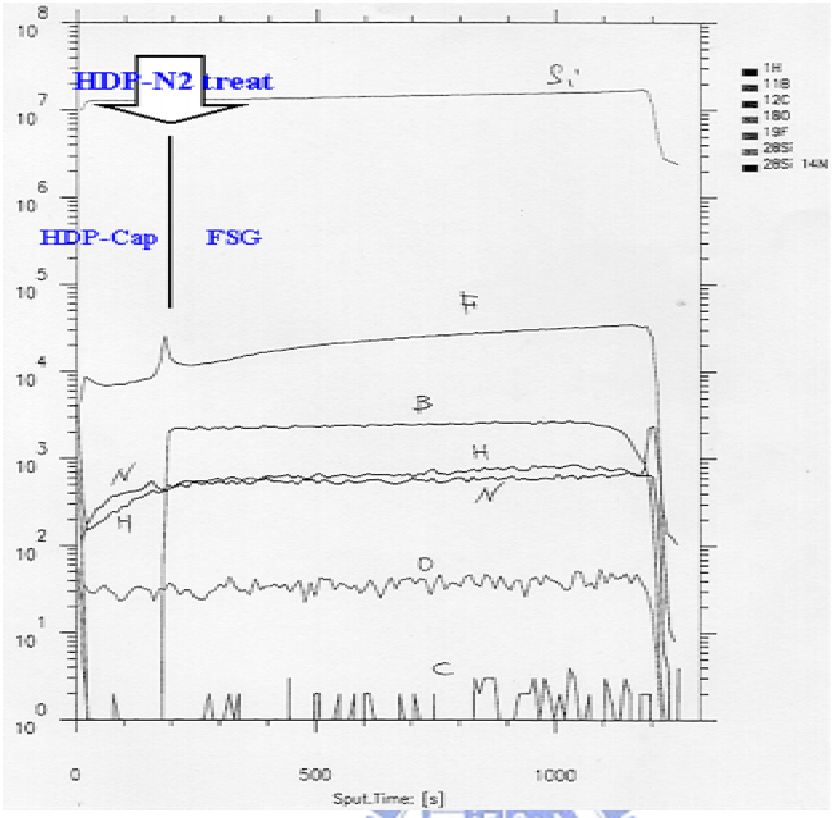


Figure 4-4-5. SIMS depth profile of the FSG film with in-situ HDP-N_2 treatment and HDP-USG capping layer.

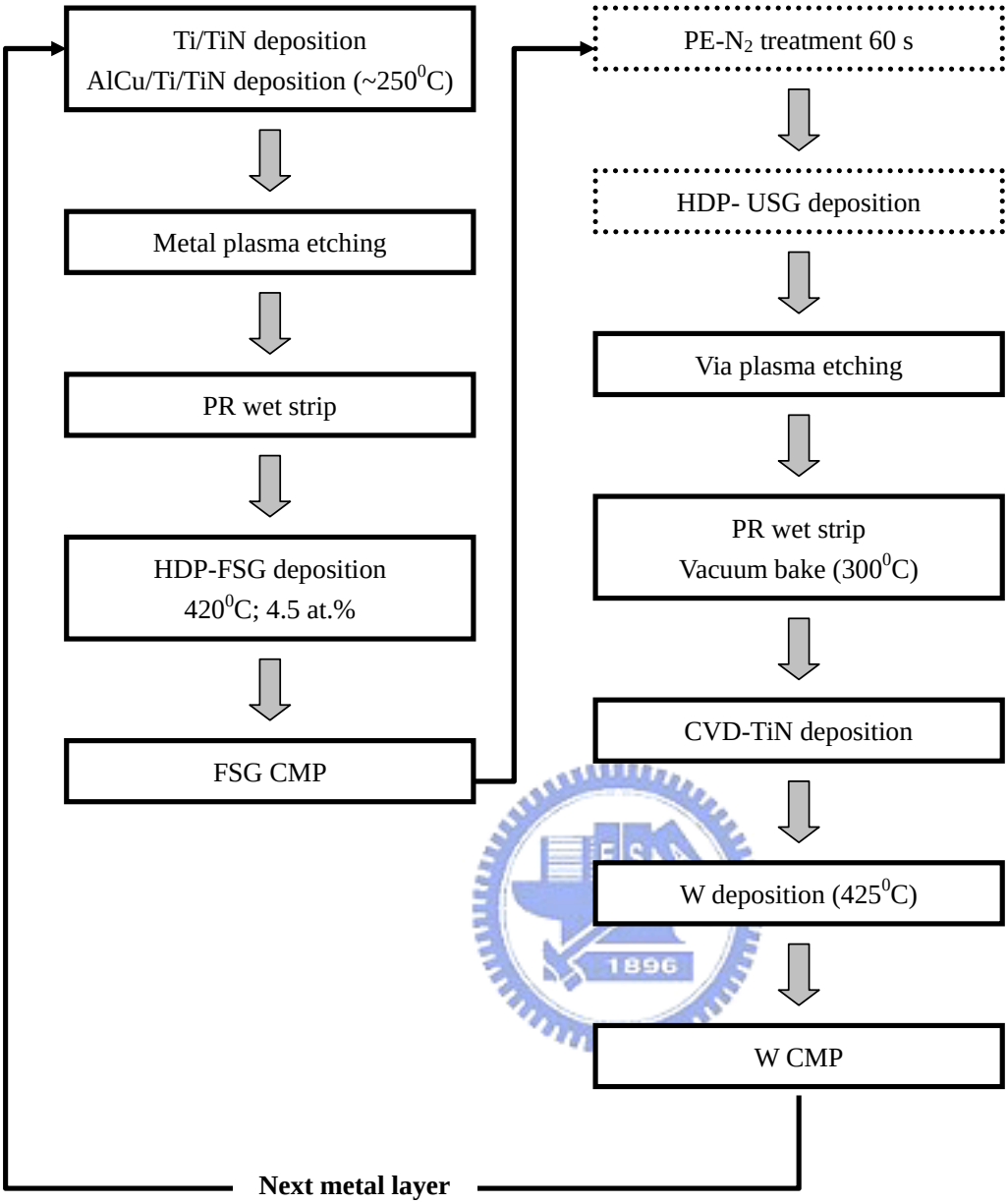


Figure 4-4-6. Optimized process flow for Al/Cu metallization.

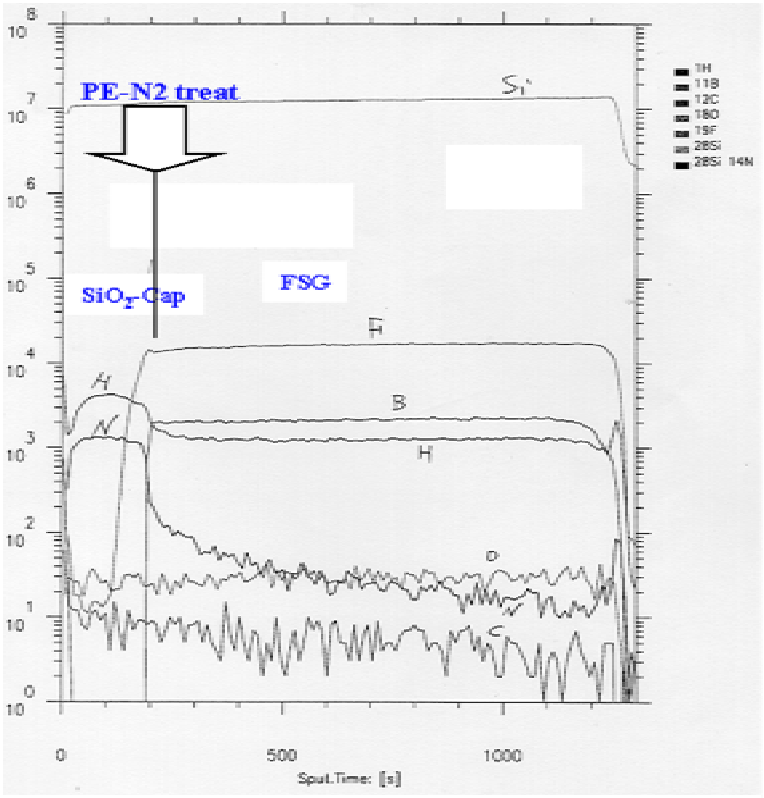


Figure 4-4-7. SIMS depth profile of the FSG film with PE-N_2 treatment and ex-situ HDP-USG capping layer.

Table 4-5-1. The film properties of HDP-CVD FSG and PE-CVD FSG layer.

	HDP-CVD FSG	PECVD FSG
Dep Rate(nm/min)	**321.5**	**687.4**
Uniformity(49P, 3mm Exclusion)	**1.943**	**1.421**
RI(633nm)	**1.4413**	**1.4416**
Stress	**-6.00E+08**	**-1.70E+09**
F%(SiF/Si-O)	**4.5**	**6**
Dielectric constant	**3.624**	**3.702**

Table 4-5-2. The integration properties of HDP-CVD FSG and PE-CVD FSG layer.

		HDP-CVD FSG	PECVD FSG	PECVD Oxide
Control wafer	Etch Rate(nm/min)	262.1	270.3	243.1
	CMP Polish rate(nm/min)	241.6	289.6	222.6
Pattern Wafer	Etch Rate(nm/min)	143.2	158.3	140.5
	CMP Polish Selective	1.026	1.045	1
	CD of Via	0.2562	0.2564	-

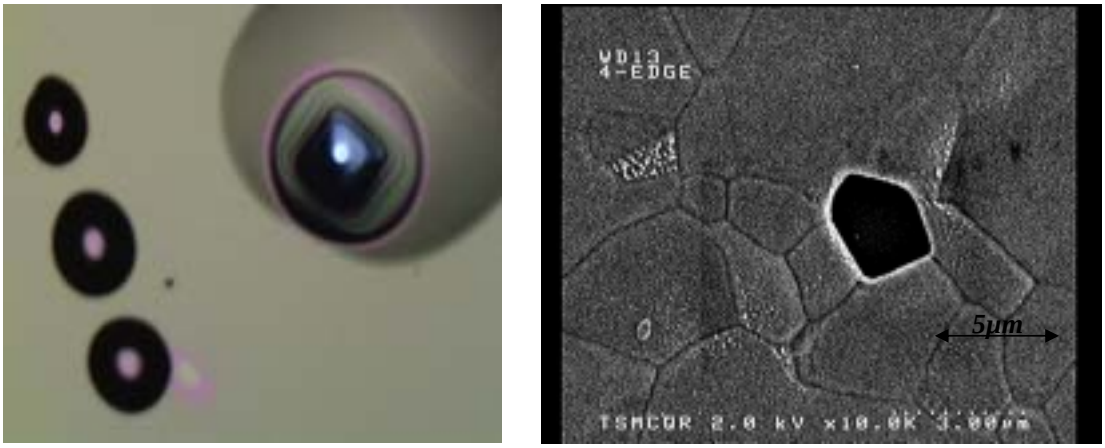


Figure 4-5-1. Corrosion images of FSG/TiN/AlCu/TiN/Oxide: (a) OM image and 9b) SEM image.

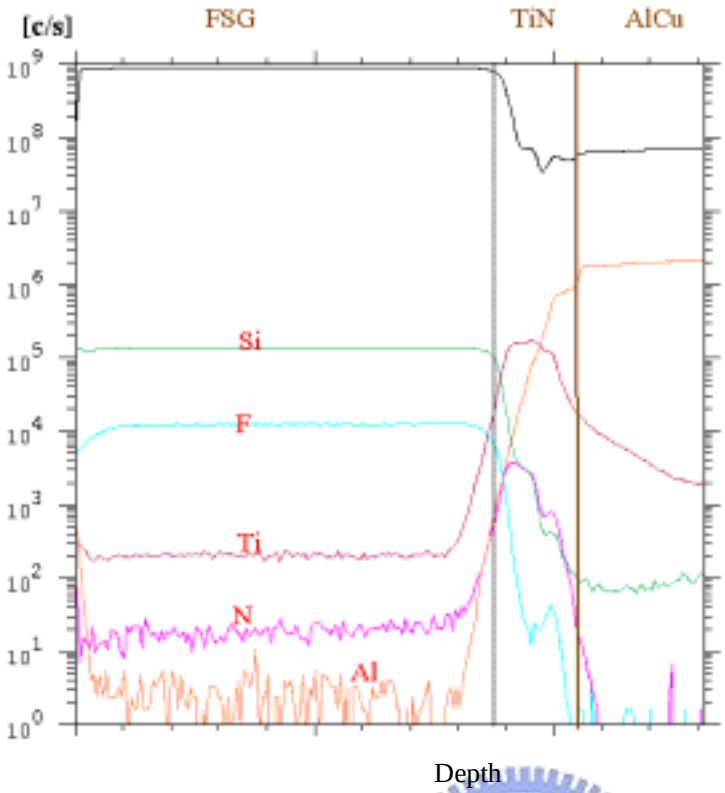


Figure 4-5-2. The SIMS profile for FSG/TiN/AlCu/TiN structure.

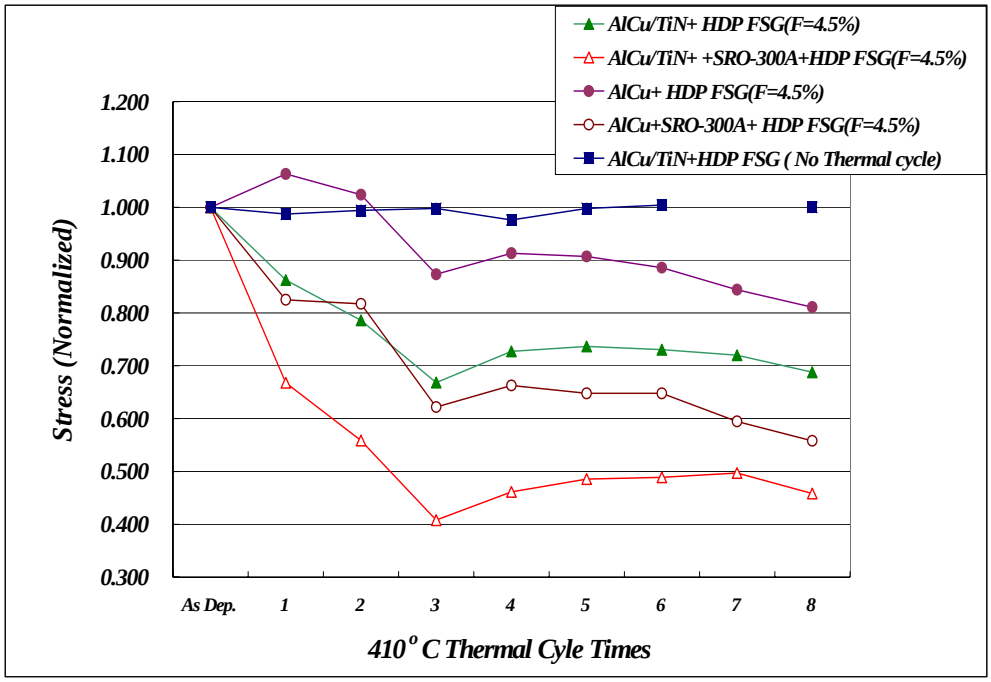


Figure 4-5-3. The stress change for FSG/TiN/AlCu/TiN structure after 410°C alloy test.

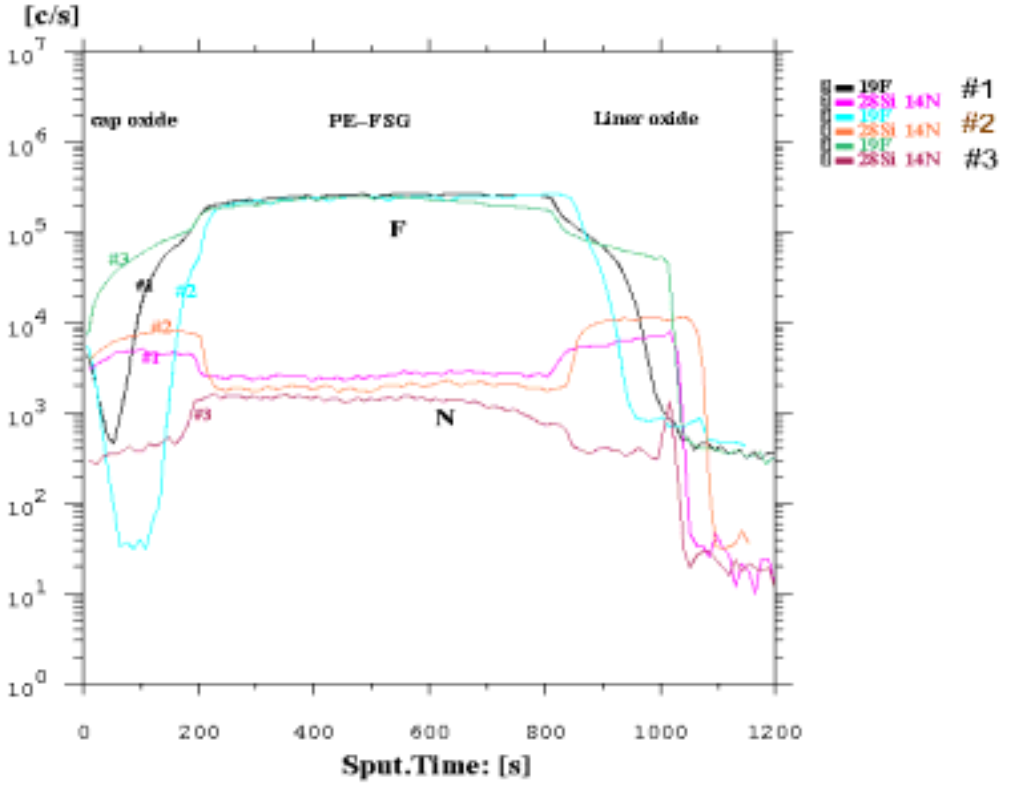


Figure 4-5-4. The F profile of FSG film with different oxide for oxide/FSG/oxide structure: (1) RI=1.80 oxide, 92) RI=1.460 oxide, and (3) RI=1.500 oxide.

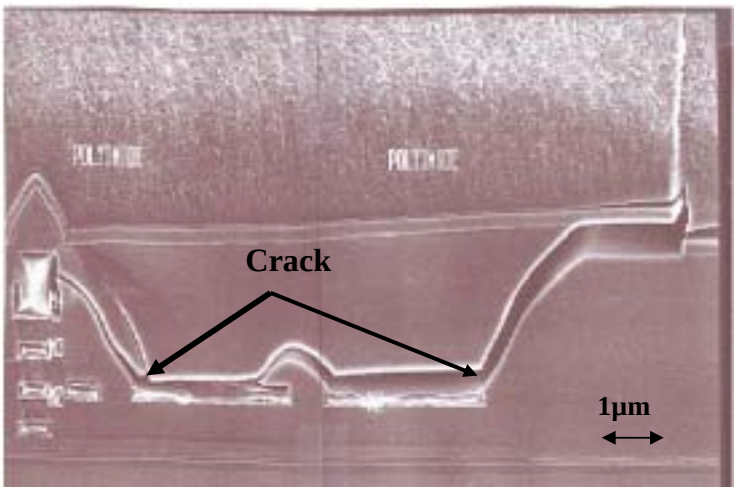
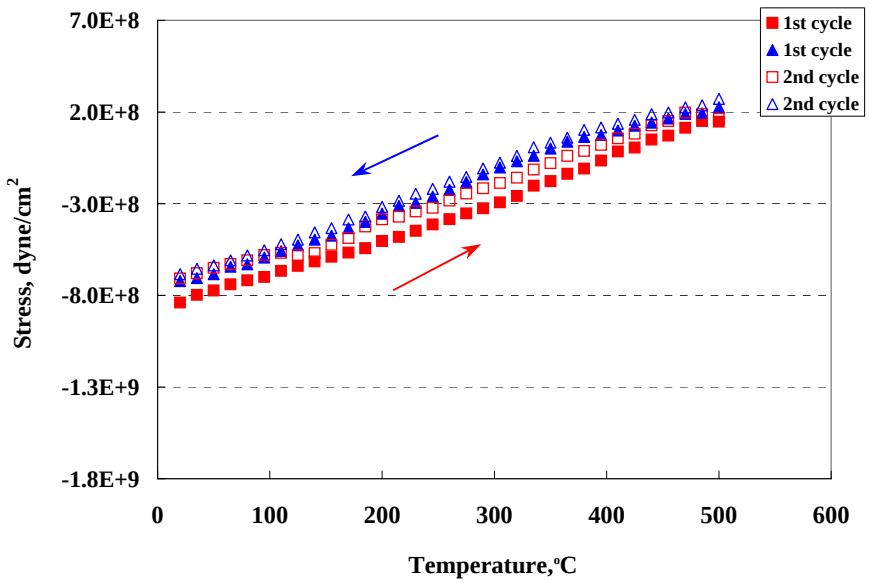


Figure 4-5-5. The SEM image of full HDP-CVD FSG IMD film crack on four-layer metal design.

(A)



(B)

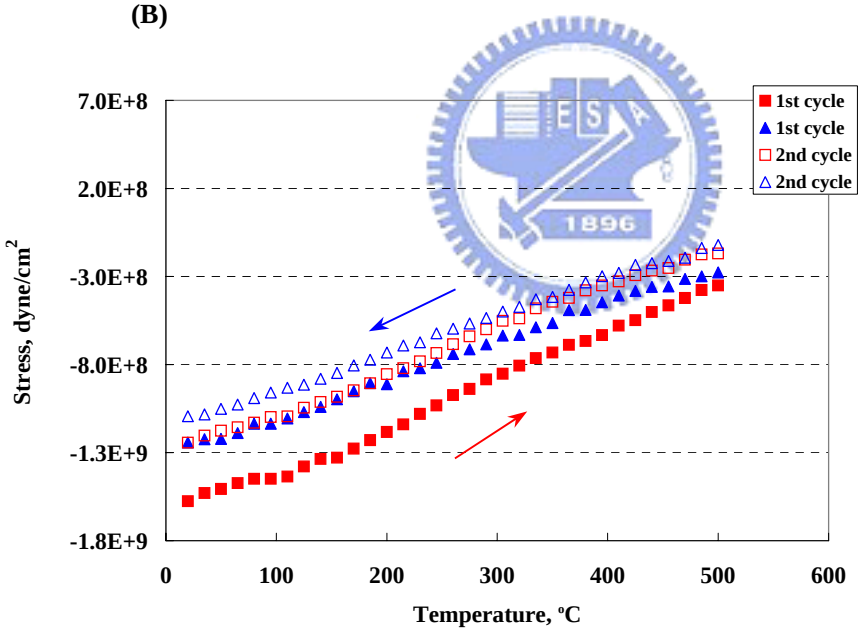


Figure 4-5-6. The stress hysterisis of FSG film: (A) Full HDPCVD FSG layer and (b) A stack of HDP-CVD and PE-CVD FSG layer.

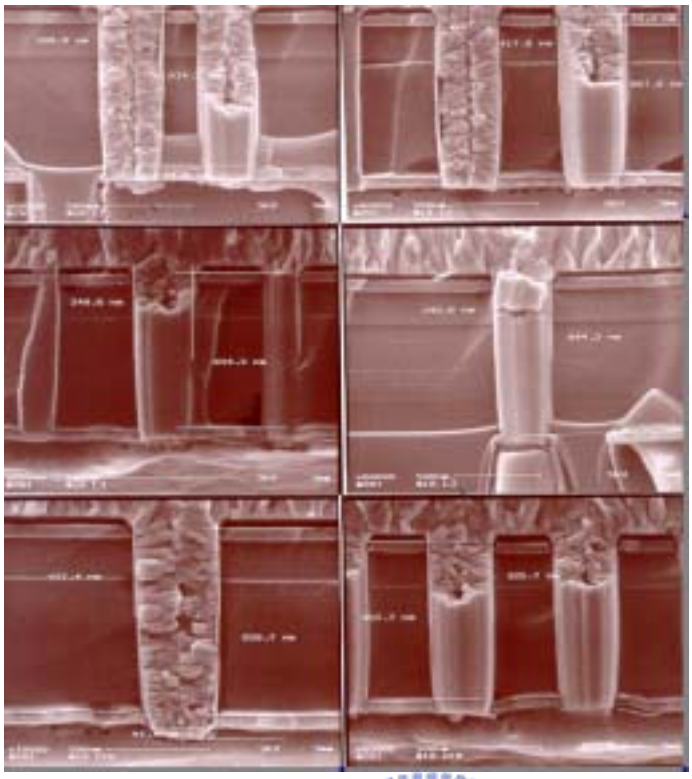
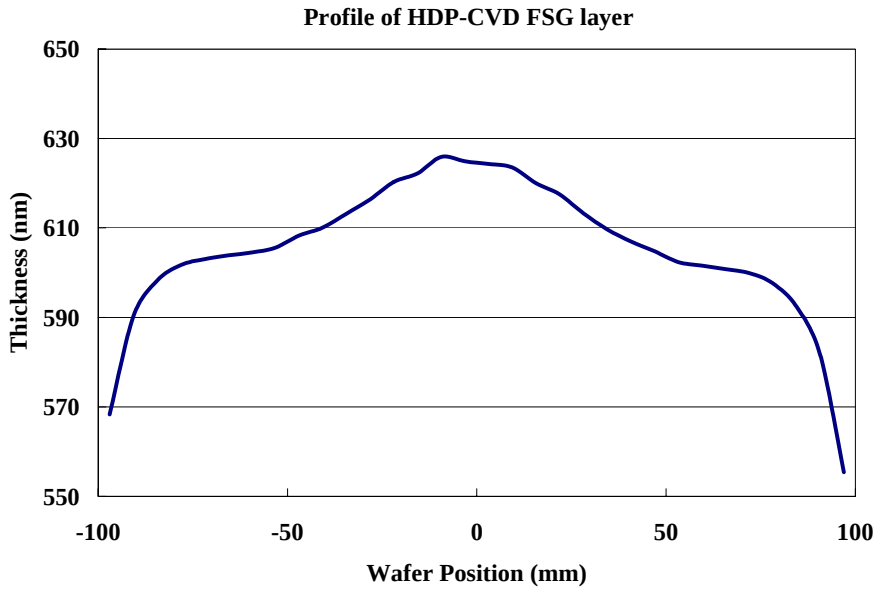


Figure 4-5-7. Partial integration of a stack of HDP-CVD FSG and PE-CVD FSG layer.

(A)



(B)

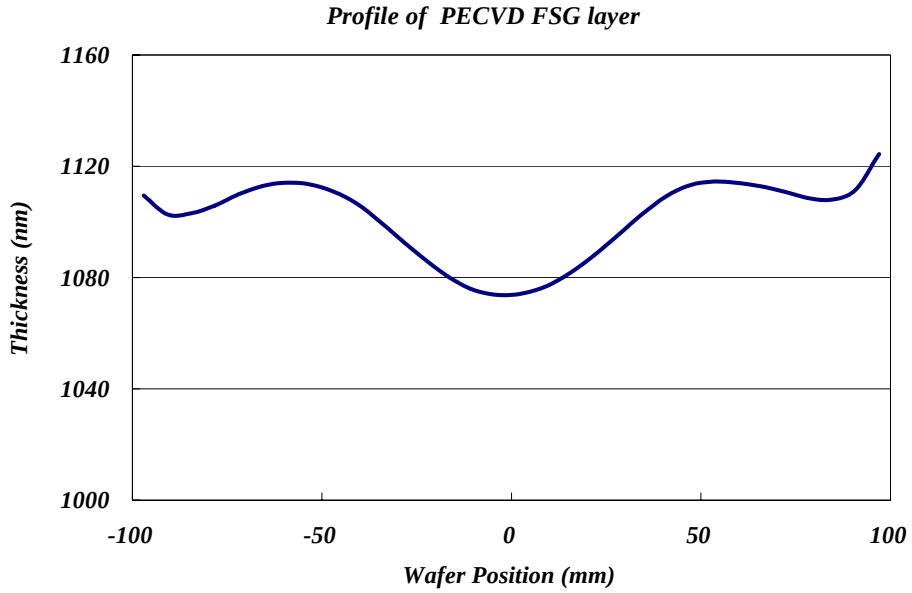


Figure 4-5-8. The profile of FSG film on 200mm control wafer: (Top) HDP-CVD FSG and (Bottom) PE-CVD FSG.

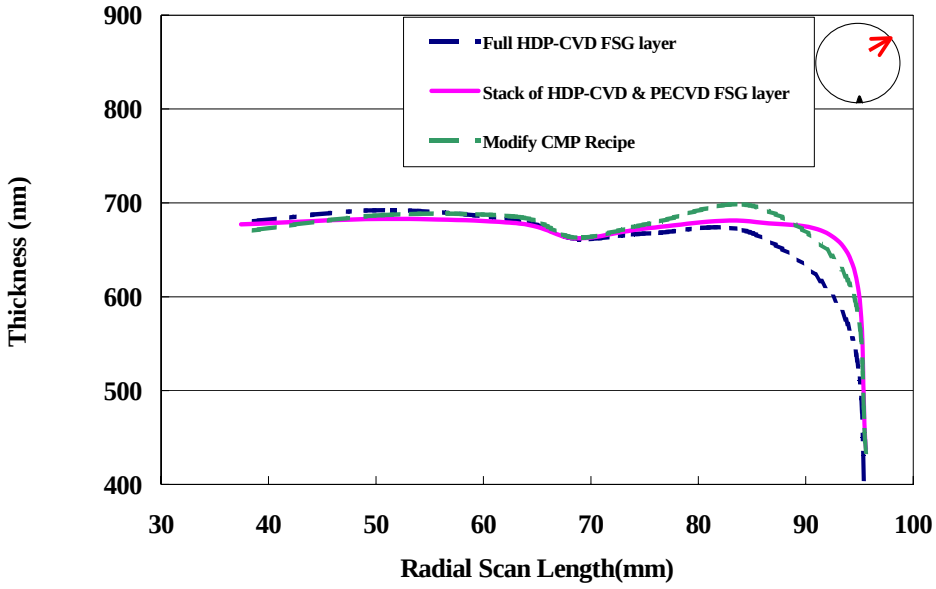


Figure 4-5-9. Edge profile of the fifth IMD-layers dielectric films in product with different FSG films after CMP.

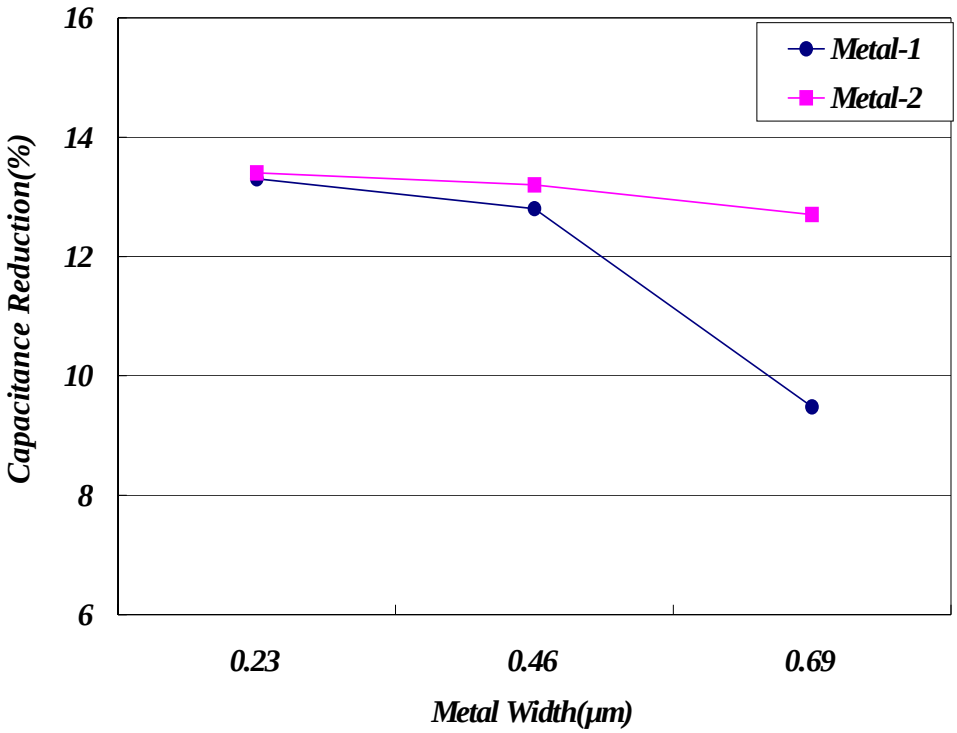


Figure 4-5-10. Line-to-line capacitance of FSG layer for different metal structure with 0.23 μm gap.

Chapter 5

Characterization of Carbon-doped silicate glass

As advanced microelectronics at the 0.13 μm technology, a low dielectric constant (k<3.0) dielectric insulator is needed to minimize signal propagation delay, crosstalk between adjacent metal lines, and power consumption, because FSG film cannot provide a further reduced dielectric constant (k <3.0). Various organic and inorganic materials have been considered as low-k materials. These low-k materials must also meet all integration requirements, including high thermal stability, low leakage current, low moisture uptake, good mechanical strength, high adhesion with other materials, and low stress.

There are many strategies for the vapor deposition of the low-k films. One strategy to reduce the dielectric constant is to add alkyl (CH_3) groups to the silicon oxide based dielectric materials. Changing the composition and connectivity of atomic constituents will also vary the dielectric constant; that is, introducing porogen into the films can reduce the dielectric constant.

Difficulties in device integration and manufacturing, however, have delayed the implementation of low-k materials. The reduced hardness of low-k films, and the change in elemental composition from traditional silicon dioxide, present challenges for the etch/strip, CMP, and assembly/package stages. Understanding the relationship between film preparation and film properties is crucial to designing a film that can meet integration requirements.

Carbon-doped oxide prepared by chemical vapor deposition has increasingly received more attention and has been adopted as the low-k material of choice for the below 0.13 μm technology node. In spite of the reduced dielectric constant, carbon-doped oxide low-k films have lower film hardness, thermal stability and hermeticity.

Optimization of the Plasma-Enhanced chemical vapor deposition (PE-CVD) carbon-doped oxide low-k film and the correlation between precursor, process, film structure,

and film properties, are essential.

5-1 Carrier Gas Effect on Structure and Electrical Properties of Low-Dielectric Constant SiCOH Film

5-1-1 Motivation

The continuous shrinkage of the device dimensions of the ultra-large-scale integrated (ULSI) chips imposes strong demands on the backend of the line (BEOL) interconnect structure. Low-dielectric-constant (low-*k*) SiCOH materials are required in the interconnect structure to reduce parasitic capacitance of multilevel interconnects, cross-talk noise between metal wires, and power dissipation from the RC coupling [118-120]. For these reasons, strong efforts have been conducted to find a suitable insulator material with a dielectric constant about 2.8-3.2.

There are intense industry-wide efforts to develop low-*k* materials as interlayer dielectrics. It is well known that the incorporation of carbon into SiO_2 would decrease its dielectric constant. Carbon-doped low-*k* films are usually deposited by plasma-enhanced chemical vapor deposition (PE-CVD) from a mixture of trimethylsiane [3MS, $(CH_3)_3SiH$] or tetramethylsilane [4MS, $(CH_3)_4Si$] with oxygen [121,122]. However, there is a trade-off between the dielectric constant and mechanical strength of these low-*k* films. A low-*k* film with a lower dielectric constant usually accompanied with a weaker mechanical strength and vice versa. As a result, optimization of the process conditions is inevitable for meeting the low-*k* films requirements, including a lower dielectric constant and an improved mechanical strength.

In this work, different carrier gases were added during the deposition process of the low-*k* film with 3MS and oxygen as the reaction gases in a PE-CVD system. The influence of carrier gas on the physical properties (thickness and refractive index), structure properties, electrical properties (dielectric constant and breakdown voltage), and mechanical strength of the low-*k* films are investigated.

5-1-2 Experimental Procedures

A low-*k* film was deposited from 3MS and O_2 using radio frequency 13.56 MHz plasma on an Applied Materials Producer system with a 200 mm chamber. Two different carrier gases (He, Ar) were used with the flow rate of 300 cm^3/min. For comparison, the low-*k* films were also deposited without carrier gas from the mixture of 3MS and O_2 (referred to as STD). The optimal 3MS/O_2 gas ratio was 6. The deposition pressure and RF power were maintained at 533 Pa and 600 W, respectively, throughout the deposition process. The deposition temperature was varying from 200 to 400^oC.

Film thickness and refractive index (RI, at 633 nm wavelength) were measured by reflectometer and/or ellipsometer using the Nano-Spec®9100. Forty-nine point measurements were conducted on each wafer and the uniformity is defined herein as

$$\text{Uniformity} = \frac{\text{Std.}}{\text{M}} \text{X}100\% \qquad \textbf{(5-1-1)}$$

where Std. is the standard deviation and M is the mean value from the 49-point measurements. Chemical bonding of the film was investigated using Fourier transform infrared spectroscopy (FT-IR) [Bio-Rad Win-IR PRO] and X-ray photoemission spectroscopy

(XPS) using the 30-nm thick film deposited on an 8-inch silicon wafer. XPS measurements were performed in a VG Microlab 310F system utilizing a MgKα X-ray source. The MTS Nano Indentor was used to measure the nano-hardness and Young's modulus of these films. The sample thickness for nano-hardness measurement was approximately 1 μm. The depth penetration was about 100 nm at ~ 0.3 mN down force, and each hardness entry is the average over 5 measurements. Dielectric constant and leakage current were measured by mercury (Hg) probe current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) methods (5100 CV system) at 1 MHz.

5-1-3 Results and Discussions

For the CVD reaction mechanism, the reaction sequence can be separated into several sequential steps. For the 3MS/O_2 low-*k* film deposition process used in this study, exhibited in Figure 5-1-1, 3MS and O_2 were used in the gas phase under the plasma environment to form the intermediate compounds, which could further react with O_2 to form by-products. The forming intermediates then diffuse through the gas media, which is mostly composed of an O radical and a carrier gas (if Ar or He was introduced), and are adsorbed onto the substrate, undergoing surface migration and reaction to form the low-*k* film. Other by-products desorb from the substrate surface and diffuse into the gas phase.

The reaction mechanism is mainly divided into three major process steps, the gas phase reaction, the gas phase diffusion, and the surface reaction. Each of the process steps in the reaction process has its own characteristics and depends on the process conditions used: (i)

gas-phase reaction relies on a function of the chamber pressure, reactant concentration (controlled by gas flows), and temperature inside the gas-phase, which depends on the thermo-conductivity of the gas-phase molecules; (ii) gas-phase diffusion is affected by the distance traveled by the intermediates, which scales with susceptor spacing. The mean free path (or diffusion coefficient) is a function of gas molecular size and chamber pressure; (iii) surface processes including adsorption, migration, surface reaction, and desorption, are functions of the surface temperature and less affected by the total pressure inside the chamber. All three major steps are the series reaction steps. Based on the kinetic theory, the film deposition rate is the net effect of all the above steps, including gas-phase reaction, diffusion, and surface reactions, and it is limited by the step with the slowest forming rate. Therefore, investigation of the deposition rate helps identify the restricting step and optimize the conditions for this process.

The temperature dependence of deposition rate of the low-*k* films with various types of carrier gases is shown in Figure 5-1-2. The deposition pressure and RF power were set at 533 Pa and 600 W, respectively. Regardless of the type of the carrier gas, the low-*k* film deposited using 3MS and O_2 gases displays a very strong surface temperature effect and follows a similar kinetic reaction mechanism. The decreasing deposition rate suggests the importance of the surface adsorption and desorption. Moreover, the activation energy of the reaction can be determined by the Arrhenius equation shown as follows.

$$R = A\exp(-E_a / KT) \quad \textbf{(5-1-2)}$$

where R is the deposition rate, A the Arrehenius constant, E_a the reaction activation energy, K the Boltzmann constant, and T is the absolute temperature. From Eq. (5-1-2), the activation energy for the low-*k* films with different carrier gases is comparable. The values are 0.642 eV and 0.666 eV for Ar and He carrier gases, respectively. On the other hand, the deposition rate of the low-*k* film using dilute Ar gas is clarified to be larger than that of He or without any carrier gases. The causes are (i) the carrier gas can rapidly ionize the reactants, 3MS and O_2, to form radicals and increase the concentration of the reactants. (ii) The ionization voltage of Ar gas is lower than that of He carrier gas, indicating that He gas is scarcely ionized. Therefore, compared to Ar carrier gas, the plasma strength in the process chamber using He is rather weaker. In addition, the uniformity of low-*k* film thickness [obtained from Eq. (5-1-1)] can be reduced from 2.5 to 1.5 % as a result of uniform plasma distribution for Ar carrier gas. This non-uniformity of thickness or RI causes the large variations in device performance depending on the location of the wafer. The low-*k* films deposited using 3MS, O_2, and Ar carrier gas have a more uniform thickness and dielectric constant from the center to the edge location of the wafer, which may be caused by a uniform plasma density across the wafer as Ar gas is incorporated into the reaction.

Further investigation of the effect of carrier gas on the low-*k* film was performed to study the deposition mechanism. Figure 5-1-3 shows that the deposition rate varies with the

deposition pressure. A drastic difference in the pressure dependence of deposition rate of the low-*k* films with different carrier gases can be observed in Figure 5-1-3. For Ar carrier gas, an optimized deposition rate is achieved as the chamber pressure changes. This can be interpreted as a change in the controlling step from reaction-limited to diffusion-limited step. In a low-pressure region (< 400 Pa), the reaction rate is relatively slow, due to insufficient gas-phase intermolecular collision. However, a faster diffusion rate is due to the long mean free path of the intermediates. Therefore, gas phase reaction controls the total deposition rate. In contrast, with either He carrier gas or without a carrier gas, a strong pressure effect is exhibited. The deposition rate is increased with decreasing the pressure. The reason for the difference between Ar and He carrier gas is the mean free path of the intermediates, resulting from the differences of the molecular size and collision diameter. Table 5-1-1 shows the physical properties of Ar and He gases.

Figure 5-1-4 compares the relationship between the dielectric constant (*k* value) and the refractive index of the low-*k* films using Ar or He carrier gases. As compared to the low-*k* film without a carrier gas, the *k* values of low-*k* films using Ar or He carrier gas are found to be slightly larger. Furthermore, the *k* value using Ar carrier gas is larger than that of He carrier gas at the same deposition pressure and temperature. From the FTIR absorption peak height ratio between the Si-CH_3 and Si-O bonds, a higher value is calculated using Ar carrier gas. The higher Si-CH_3 content in the low-*k* film is known to lead to the lower *k* value in

most cases. However, this result conflicts with the *k* value shown in Figure 5-1-4. It is worth noticing that the reduction of dielectric constant of the low-*k* film is attributed to a less polarization of Si-CH_3 bonds and a micro-porous structure. It is believed that the refractive index of a dielectric film reflects its density. A lower film density means it contains a more micro-porous structure. As a result, when the carrier gas (Ar or He) is introduced into the process chamber, the *k* value reduction of the deposited film is contributed from Si-CH_3 bonds and micro-porous voids. As shown in Figure 5-1-4, the low-*k* film using Ar carrier gas has a higher refractive index, which means this low-*k* film has a less micro-porous structure. In spite of the higher Si-CH_3 bonds, the low-*k* film with Ar carrier gas has a higher *k* value resulted from the micro-porous structure dominant in the reduction of the *k* value. The velocity of He is faster than that of Ar. As a result, He gas easily collides with 3MS that contains Si-CH_3 bonds, reducing the bonds in the precursor. On the other hand, Ar gas has a bombardment effect, to densify the low-*k* film. Therefore, a lower *k* value indicates that the deposited film using He carrier gas has more voids than that using Ar carrier gas.

To further investigate the role of the carrier gas on the chemical structure of low-*k* films, XPS was used to address the differences in the chemical structure. Table 5-1-2 lists the percentage of elements from XPS quantification. Films deposited by the carrier gases were determined to have a similar atomic ratio although there is still a slight increase in carbon atoms for the Ar carrier gas. This result matches with the result acquired from FTIR analyses.

Furthermore, we deconvoluted the Si (2p) spectra into the five main moieties using a curve-fitting method, as indicated in Figure 5-1-5. These five chemical distinct Si atoms arise from SiO_4 (103.4 eV), SiO_3 (102.2 eV), SiO_2 (101.1 eV), SiO_1 (10.2 eV) and SiO_0 (99.1 eV), respectively. Table 5-1-3 compares the Si (2p) spectra bonding energy of films deposited using various carrier gases. As shown in Table 5-1-3, all films exhibit a similar structure, resembling the FTIR spectrum. This indicates that the dominant Si binding energy is about 101.1 eV. As a consequence, it is implied that the main bonding of the films is -O-Si-O-Si-.

Figure 5-1-6 shows the leakage current density of the low-*k* films deposited using different carrier gases. The deposition pressure and RF power were 533 Pa and 600 W, respectively. It is found that the leakage current density of the low-*k* film deposited using Ar carrier gas is slightly lower than that of He carrier gas or without a carrier gas. The lower leakage current density of the low-*k* film using Ar carrier gas is a result of less porosity in the film. Additionally, the leakage current densities of the low-*k* films are approximately 10^{-9} A/cm^2 in an electric field of 2 MV/cm in our study, which are similar to other studies [123-125].

Figure 5-1-7 compares the dry etching rate of the low-*k* films deposited using various carrier gases. The dry etching process was performed under reactive ion etching processes using $CF_4/CHF_3/N_2/Ar$ as the reactant gases. The influence of the carrier gas on the dry etching rate is obvious shown in Figure 5-1-7. The lowest and highest etching rate is obtained

with Ar carrier gas and STD condition (without carrier gas), respectively, implying that the deposited low-*k* film using Ar carrier gas has a higher film density and a lower porosity. It suggests that the low-*k* film deposited in Ar plasma ambient is suitable for the inter-metallic-dielectric (IMD) layer because the metal-trench depth has less variation and can be well-controlled in a dual-damascene structure without a trench stopping scheme process.

Low hardness of the low-*k* film causes a peeling issue during the copper chemical mechanical polishing (Cu-CMP) processes. Therefore, the hardness of the low-*k* film should be taken into account as the low-*k* film is implemented into multilevel metallization. Mechanical hardness and Young's modulus of the low-*k* films deposited with different carrier gases are plotted as a function of the deposition temperature shown in Figure 5-1-8. It is noted that the hardness of the low-*k* film deposited with Ar carrier gas is higher than that of the other two deposition conditions for all temperature ranges. This result proves that the low-*k* film with Ar carrier gas is more suitable for the implementation as an IMD low-*k* film due to its high mechanical strength against the Cu-CMP processes. Figure 5-1-8 clearly indicates a trend on the improvement in hardness as well as Young's modulus when the deposition temperature is increased. However, the dielectric constant of the deposited film is increased with raising the deposition temperature. The hardness and the dielectric constant of the low-*k* film show a trade-off depending on the deposition temperature. Consequently, it is

essential to reach a compromise between the dielectric constant and the mechanical strength when the deposition temperature is determined.

5-1-4 Summary

PE-CVD low-*k* films utilizing 3MS and O_2 as source reactants and Ar or He as the carrier gas were characterized in this study. The deposition rate of the low-*k* film is increased as the carrier gas was introduced. However, a slight degradation on the dielectric constant of the deposited low-*k* films was occurred. Also, low-*k* films with Ar carrier gas exhibited the strong improvement in deposition rate, non-uniformity, leakage current density, and hardness due to the decrease of micro-pores in the deposited films.

5-2 Precursor Effect on Structure and Electrical Properties of Low Dielectric Constant SiCOH Film Using Trimethylsilane (3MS) and Diethoxymethylsilane (DEMS) Prepared by Plasma Enhanced Chemical Vapor Deposition

5-2-1 Motivations

As feature sizes of integrated circuits (ICs) shrink below 180 nm, interconnect resistance-capacitance (RC) delay begins to dominate overall device speed in Cu/low-*k* metallization. To decrease RC delay time, interconnection resistance has been reduced using

copper instead of aluminum while interlayer capacitance has been lowered by replacing conventional tetraethoxysilane (TEOS) SiO_2 (k~4.0) with low-*k* materials (*k*<4.0) [118,121,125].

The applicably low-*k* materials for manufacturing necessarily have characteristics of highly thermal stability (to 425^{o}C), highly mechanical stability and compatibility with etching, stripping, cleaning, and chemical mechanical polishing (CMP) processes. The early winner of low-*k* materials, fluorosilicate glass (FSG), is currently scaled into volume production. However, its dielectric constant (*k* = 3.5~3.8) is not low enough to significantly reduce the interconnect delay. In next technology generation, the promising material, organic carbon doped silicates (OSG), with *k* value of 2.8~3.2 will likely be the candidate [120-122,134,135].

Low-*k* films with *k* values of ~3.0 (after annealing) deposited by radio frequency (13.56 MHz) plasma-enhanced chemical vapor deposition (rf-PE-CVD) and using trimethylsilane (3MS) and oxygen as precursors have been investigated in recent literatures [119,136]. However, the 3MS-based low-k films were too soft to perform subsequent CMP processes. Recently, the PE-CVD-OSG films deposited by the diethoxymethylsilane (DEMS) precursor have received much attention. Compared with 3MS, DEMS [H-Si(CH_3)(OC_2H_5)$_2$] containing two S-OC_2H_5 bonds and one Si-CH_3 bond was anticipated to have a lower *k* value and higher hardness due to higher O/Si ratio in the DEMS the precursor.

In this work, the chemical and electrical properties of low-*k* films deposited by DEMS and 3MS precursors were investigated and the electrical reliability of both low-*k* films were compared using interconnect test devices as well.

5-2-2 Experimental Procedures

A. Sample preparation

All low-*k* films were deposited on p-type (100) silicon substrates by rf-PE-CVD. The chamber pressure, deposition temperature and rf power of PE-CVD were maintained at 6 Torr, 400^{o}C and 700 W, respectively. The reaction gases were DEMS, 3MS and oxygen. Different from 3MS (Dow Coring® Z3MS™ CVD precursor), DEMS (Air Product CVD precursor) was carried in vapor phase by inert helium gas to the reaction chamber. The detailed process parameters were listed in Table 5-2-1.

B. Film analyses

The electrical characteristics of low-*k* films were examined by capacitance-voltage (CV) measurements at 1 MHz. The thickness and refractive index (RI, at 633 nm) of as-deposited films were analyzed by reflectometer and/or ellipsometer (Nano-Spec® 9100). The functional groups of low-*k* films were identified by Fourier transform infrared spectroscopy (FT-IR) (Bio-Rad Win-IR PRO). The chemical composition of low-*k* films was identified using Rutherford Back Scattering (RBS) and X-ray photoelectron spectroscopy (XPS). Besides, the chemical environments and surface morphology of these two low-*k* films using 3MS and DEMS precursors were investigated by solid-state nuclear magnetic resonance (NMR). The nano-hardness and modulus of low-*k* films were measured by MTS Nano Indentor XP system. The sample thickness for nano-hardness measurements was approximately 1 μm and the depth penetration was about 100 nm at down force of ~ 0.3 mN. Adhesion strength and thermal stability of low-k films were determined by a stud-pull method and a thermal desorption spectroscopy (TDS) respectively.

5-2-3 Results and Discussions

A. Chemical composition and structure of blanket low-*k* films

Figure 5-2-1 shows the FTIR spectra of as-deposited low-*k* films using 3MS and DEMS as precursors. As shown in Figure 5-2-1, the absorption bands corresponding to CH_n (n = 1-3) stretching centered at ~2900 cm^{-1}, Si-H stretching at ~2200 cm^{-1}, CH_3 stretching at ~1250 cm^{-1}, Si-O bridging at 1020~1050 cm^{-1}, and a strong peak at ~780 cm^{-1} attributing to $–CH_3$ wagging and Si-C stretching were found. The relative intensity of these peaks was dependent on the deposition precursors. The 3MS-based films revealed strong Si-H bonds compared with the DEMS-based films. The weaker Si-H peak of the DEMS-based materials resulted from the weakly hydride bond with lower bonding energy acting like a sacrificial group in the plasma phase.

Atomic compositions of low-*k* films with *k* ~2.8 deposited using 3MS and DEMS are shown in Table 5-2-1. RBS analysis indicated that the H/C ratio of the DEMS-based films was very close to 3 while the H/C ratio of the 3MS-based films was less than 3 and close to 2. This implied that all hydrogen atoms were bonded with carbon atoms in the DEMS-based films, which agreed with the FTIR results. Both XPS and RBS also indicated that the 3MS-based films had higher carbon but lower oxygen content than those of the DEMS-based films.

To further determine the chemical structure of 3MS- and DEMS-based low-*k* films, high resolution Si (2p) and C (1s) spectra were adopted. The Si (2p) peak was deconvoluted into five main moieties, as shown in Figure 5-2-2(a) and 2(b). The binding energies of these five peaks were SiO_4 (103.4 eV), SiO_3 (102.2 eV), SiO_2 (101.1 eV), SiO_1 (100.2 eV) and SiO_0 (99.1 ev), respectively. For both low-*k* films, the major SiO_2 component was at 101.1 eV, which attributed to the –O-Si-O-Si-O- structure. However, it was worthily noted that the ratio

of SiO_0 (99.1 eV) of the DEMS-based films was lower than that of the 3MS-based films indicating that the 3MS-based films had more low-degreed Si-O crosslinkings. Therefore, the DEMS-based films had higher mechanical strength than that of the 3MS-based films.

As shown in Figures 5-2-3(c) and 5-2-3(d), the C (1s) spectra were deconvoluted into four main moieties. The binding energies of these four chemically distinct C atoms were 285.2, 284.1, 283.4 and 282.4 eV, respectively, which attributed to $–C-O_2$, -C-O-, H_3-C-Si-, and $C-Si_{4-x}H_x$. The dominated C moiety was $Si-CH_3$ at 283.4 eV for both low-*k* films. Compared with the 3MS-based films, the DEMS-based films had higher content of $Si-CH_3$, which was consistent with the FTIR results, resulting in lower *k* values of the DEMS-based films.

Figure 5-2-4 shows that the ^{29}Si- NMR spectra of 3MS- and DEMS-based films. It was found that the 3MS-based film had stronger trimethylsily {$SiO-Si-(CH_3)_3$} group located slightly downfield of ~0 ppm than that of the DEMS-based films. Both ^{29}Si- NMR and XPS results confirmed that the 3MS-based films had higher content of $Si-(CH_3)_3$ structure than that of the DEMS-based films leading to a lower hardness.

Table 5-2-3 compares the physical and electrical properties of the low-*k* films deposited by 3MS and DEMS precursors. In particular, the DEMS-based films had higher RI than that of the 3MS-based films whereas the DEMS-based films had lower density than that of the 3MS-based films. Generally, a higher RI means a higher film density and vice verse. However, the DEMS-based films had higher density with lower RI compared with the 3MS-based films due to higher Si-O network content in the DEMS-based films. This implies that these two materials had exactly different structure and composition, as mentioned above.

The dielectric constant at 1 MHz can be divided into three main items, electronic (k_e), ionic (k_{ion}) and orientational (k_{ori}) polarizations, as the following equation:

$$\text{Dielectric constant (1 MHz)} = k_e + k_{ion} + k_{ori} \quad \textbf{(5-2-1)}$$

Electronic polarization is the square of RI (n) at 633 nm wavelength. As shown in Table 5-2-3, the major difference in the dielectric constant of 3MS- and DEMS-based films was electronic polarization. Lower electronic polarization of the DEMS-based films resulted from the replacement of Si-C with Si-O bonds. Although the Si-O bond was more ionic than the Si-C bond, the ionic polarization had less effect than the electronic polarization on the dielectric constant of both low-*k* films. The electronic polarization dominated the overall dielectric constant.

The leakage current (~2.45E-9 A/cm^2) of the DEMS-based films was lower than that of the 3MS-based films while the breakdown voltage (~ 2 MV/cm) of the DEMS-based films was higher than that of the 3MS-based films. The superior electrical properties of the DEMS-based film might be due to its higher film density and oxygen-richer structure.

B. Thermal stability of low-*k* films

Figure 5-2-5 shows the dielectric constants and normalized thickness of low-*k* films after annealing in N_2 ambient for 1 h at elevated temperature. The dielectric constants and film thickness of both low-*k* films after annealing remained stable up to 600^{o}C. However, the dielectric of both 3MS- and DEMS-based films slightly decreased as the annealing

temperature was lower than 600^{o}C. The result might be due to the removal of a larger amount of moisture trapped in both low-*k* films. Further increasing the annealing temperature (> 600^{o}C) induced film shrinkage and an increase of dielectric constant in both low-*k* films. It was notably found that the 3MS-based films significantly degraded at annealing temperature of ~600^{o}C, whereas the DEMS-based films degraded at ~700^{o}C. It was proposed that the DEMS-based films had less Si-H bonds (weaker strength) and more Si-CH_3 bonds (higher strength) resulting in higher thermal resistance than that of the 3MS-based films. The thermal stability of these two low-*k* films was also studied using TDS (not shown). From the results, H_2 radical began to desorb at ~350^{o}C while Si-CH_3 bonds started to break to form CH_3 radical at ~500^{o}C. Furthermore, the slightly increase of desorption temperature and lower H_2O signal in TDS results for the DEMS-based film indicated that the DEMS-based films had higher thermal stability and higher resistance to moisture absorption due to its hydrophobic methyl groups.

C. Stability of low-*k* films under plasma treatments

In process integration, the low-*k* films inevitably exposed in plasma environments during the pre-treatment of barrier layer deposition and photo-resist ashing. The conventional plasma gases were N_2, NH_3, H_2 and O_2. Therefore, the stability under these plasma treatments was necessarily investigated. In this study, the low-*k* films were treated under different plasma for 3 min. For N_2, H_2 and NH_3 plasma treatments, there was no obvious change in

film properties after plasma treatment. The result indicated that both films deposited from 3MS and DEMS precursors remained stable under these gas plasma treatments. However, these two low-*k* films degraded drastically after O_2 plasma treatment by breaking the Si-CH_3 and C-H bonds. The result pointed out that it was necessary to prevent these low-*k* films from exposing to O_2 plasma environments or to modify the surface of the low-*k* films to against the oxygen radicals. In addition, as shown in Figure 5-2-6, the low-*k* films prepared by DEMS had higher oxygen plasma resistance compared to that of the 3MS-based films. The dielectric constant of the DEMS-based films increased to 3.8 after O_2 plasma treatment while the 3MS-based films had a higher *k* value of 4.5. The plausible reason was that the DEMS-based films had less Si-H bonds and more Si-O crosslinkings.

D. Adhesion strength of low-*k* films on various barrier layers

In Cu ILD architecture, the low-*k* films directly contact with different barrier layers such as SiN, SiCN and TaN. The interface condition between low-*k* films and barrier layers is essential for the reliability performance. Figure 5-2-7 compares the adhesion strength of low-*k* films on Si_3N_4, SiCN, SiOC, and TaN barrier films. It was found that the DEMS-based films had higher adhesion strength than that of the 3MS-based films on all barrier layers. The result might be due to the lower change of stress and higher surface roughness of the DEMS-based films.

E. Interconnect electrical performance of low-*k* films

The electrical performance and reliability of the low-*k* films deposited by 3MS and DEMS precursors were confirmed using Cu dual-damascene test structure. The resistance (Rc) of 0.18-μm vias in the test devices is shown in Figure 5-2-8. It was found that the DEMS-based films had more convergence distribution of Rc than that of the 3MS-based films. In addition, the effective *k* value of low-*k* films from lateral line-to-line capacitance of 0.16-μm wide spacing between the first-level interconnects were measured before and after heating test as shown in Figure 5-2-9. The effective *k* value of the DEMS-based films was 3.0 after fabricating the second–level interconnect and slightly lower than 3.2 of the 3MS-based films. Moreover, after a heating test at 425^{o}C for 2 hr, the effective *k* value of both low-*k* films still remained the same value. The result clearly indicated that the real ILD structure using low-*k* films deposited by 3MS and DEMS precursors had highly thermal resistance, consisting with the results of the blanket films. Figure 5-2-10 illustrates the metal line-to-line leakage current from the first-level interconnects of the test device for both low-*k* films. Similar with the blanket film properties, the leakage current of the DEMS-based films was lower than that of the 3MS-based films. From above results, we conclude that the low-*k* films using DEMS as precursor was suitable for ILD applications.

5-2-4 Summary

The characteristics of the low-*k* films deposited by PE-CVD using 3MS and DEMS as precursors were investigated. FTIR, XPS and ^{29}Si NMR results show that both low-*k* films had similarly element components but differently bonding structures. The DEMS-based films had a lower dielectric constant, higher hardness and higher chemical and thermal stability than those of the 3MS-based films. From the results of blanket films and four-level interconnect test devices, the DEMS-based films were found to have superior electrical performance than that of the 3MS-based films. Above results clearly reveal that the DEMS-based films are the promising low-*k* materials in the next technology generation.

5-3 Temperature Effect on Structure and Electrical Properties of Low-Dielectric Constant SiCOH Film

5-3-1 Motivation

As feature dimensions of the device in integrated circuits (IC) shrink to 180 nm and below, the interconnect delay has become a critical issue to determine the overall IC chip performance [108, 118]. To minimize the resistive and capacitive delay of interconnects, the combination of copper (Cu) and low-*k* dielectrics in the prevalent Cu dual-damascene architecture has been introduced to replace the conventional aluminum lines and SiO_2 insulator [122, 134, 144].

Low-*k* materials (**k**=2.7~3.2) are widely being considered over SiO_2 (*k*=4.2) for interlayer dielectric insulation. However, current low-*k* films are extremely difficult to integrate into semiconductor devices. Most emerging low-*k* materials are soft, weak, and

adhere poorly to other materials and are unable to withstand the semiconductor processing thus leading to crack and delamination. Consequently, low-*k* dielectrics are being comprehensively studied and developed in the light of the various reactant precursors (trimethylsilane, tetramethysilane, hexamethyldisiloxane and dimethyldimethoxysilane) [119, 120, 123, 136] and deposition techniques (spin-on or CVD) [126, 130, 138, 140] to improve these issues. It has been reported that organic-doped silicates produced by the CVD technology are the leading candidates based on their lower dielectric value, better mechanical strength, lower process costs and simplicity of processing [141, 142].

Previous studies show that the precursor type has a strong effect upon the thermal and optical properties of low-*k* film properties [145, 146]. However, for a given precursor, tunning process conditions is crucial in determining low-*k* film properties and integration performance with Cu [73, 143]. It is widely known that the quality of PE-CVD films is largely influenced by the deposition temperature; films deposited at a higher deposition temperature have better chemical and electrical properties. On the other hand, a higher deposition temperature may induce metal diffusion into its adjacent layers during the manufacturing processing. Consequently, the optimum deposition temperature is of great importance for the application of low dielectric as ILD layer in Cu copper dual damascene architecture.

In this work, the effect of deposition temperatures on the characteristics of DEMS-based low-*k* films is investigated. The dependence of the film composition and properties, and film properties integrated with Cu and ILD as a function of the deposition temperature are reported in detail. Furthermore, the electrical performance and reliability result with varying deposition temperatures are also compared using an interconnect test structure.

5-3-2 Experimental Procedures

Low-*k* films were deposited on 200 mm, p-type (100) Si substrate by PE-CVD methods using Applied Materials™ Producer system. DEMS and oxygen (O_2) were used as reactant gases with a flow rate of 250 and 50 cm^3/min., respectively. Helium (He) was used as the carrier gas helium at a flow rate of 150 cm^3/min. The chamber pressure and RF power were maintained at 6 Torr and 700 Watts, respectively, throughout the deposition process. The deposition temperature was varied from 250 to 425^oC to study the effect of deposition temperatures on the CVD low-*k* films property.

The as-deposited films exposed to heat and moisture stress tests. For the heat stress tests, the samples were annealed in a furnace at temperature from 400 to 800^oC for 1 h in nitrogen (N_2) ambient. Samples were exposed to 2 atm, 120^oC, and 100% relative humidity (RH) for 168 h for the moisture stress test.

Four-level Cu dual-damascene test device structures with 0.13 μm feature size were fabricated using DEMS-based low-*k* films deposited at different deposition temperatures. The structures used approximately 8000 Å of ILD low-*k* film was deposited on a 50 nm-thick PE-CVD silicon-carbide (SiCN) film.

Dielectric constant characterization was measured by mercury (Hg) probe capacitance-voltage (*C*-*V*) methods (5100 CV system) at 1 MHz. Film thickness and refractive index (RI, at 633 nm wavelength) were measured by reflectometer and/or ellipsometer using the Nano-Spec®9100. Nine point measurements were conducted on each wafer and averaged. Chemical bonding and composition of the film were investigated using Fourier transform infrared spectroscopy (FT-IR) [Bio-Rad Win-IR PRO], X-ray

photoelectron spectroscopy (XPS) and Rutherford backscattering spectroscopy (RBS). An MTS Nano Indentor XP system was used to measure the hardness and modulus of the films; sample thickness for nano-hardness measurement was approximately 1 μm with a penetration depth of about 100 nm at ~ 0.3 mN down force. Five indents were taken and averaged for the hardness and modulus.

5-3-3 Results and Discussions

Figure 5-3-1 shows the variation of refractive index and dielectric constant of DEMS-based low-*k* films as a function of the deposition temperature for blanket films. Film refractive index and dielectric constant increase as the deposition temperature is increased, indicating that the composition and bonding structure could be changing with the deposition temperature. The as-deposited low-*k* films with a lower deposition temperature have higher proportion of Si-CH_3 bonds obtained from Si-CH_3 (1273 cm^{-1}) to Si-O (1042 cm^{-1}) peak ratio in FTIR spectra. The organic Si-CH_3 bonds reduce the density and polarization of the deposited low-*k* films [118, 130]. As a result, the low-*k* films with a lower deposition temperature have a lower dielectric constant and refractive index (reference value of 1.46 of the thermal oxide).

Figure 5-3-2 shows the FTIR spectra of the as-deposited films deposited at 250, 350, and 425^{o}C, where the spectrum was measured in a dry N_2 ambient to eliminate a moisture-related background. Several salient features exist in the evolution of the absorption peaks. Clearly, the silanol peak (Si-OH) at about 3500 cm^{-1} is not present in the FTIR spectra for all range of

deposition temperatures, implying that the low-*k* films with deposition temperatures ranging from 250 to 425^{o}C used herein are not prone to moisture uptake in the normal ambient. As shown in Figure 5-3-2, all low-*k* films show a strong absorption peak at 1042 cm^{-1} corresponding to Si-O stretching bonds. An absorption peak at 780 and 1273 cm^{-1} are assigned to the symmetric deformation vibration of CH_3 in the Si-CH_3 group. The absorption at about 2900 cm^{-1} is assigned to the CH_3 stretching mode. Additionally, it can be seen from Figure 5-3-2 that the peak position of Si-O-Si stretching mode shifts slightly to a lower wavenumber with decreasing deposition temperature. The apparent decreasing wavenumber of the Si-O absorption is in part due to a changing bond angle of the Si-O-Si network. As a consequence, the Si-O-Si bonds are weakened so that they become less rigid and "more stretchable", resulting in a higher stretching frequency [73]. For the low-*k* films deposited at different temperatures, there is an obvious shoulder at about 1130 cm^{-1} in all the FTIR absorption spectra, associated with the broad Si-O-Si peak. It was suggested that this shoulder corresponds to Si-O-Si in a cage structure which can lead to micropores and consequently a lower film density and dielectric constant. In addition, we compared the integration absorption area ratio of the Si-O main peak at 1042 cm^{-1} and the shoulder at 1130 cm^{-1} for DEMS-based low-*k* films with different deposition temperatures, it can be found that the Si-O-Si stretching cage-like mode increases as the deposition temperature is decreased. Furthermore, there is a decrease in the Si-CH_3 (1273 cm^{-1})/Si-O (1042 cm^{-1}) peak area ratio

of the low-*k* film from 18% to ~9% as the deposition temperature is increased from 250 to 425^{o}C. Since the dielectric constant is mainly determined by the Si-CH_3/Si-O ratio, low-*k* films with a lower deposition temperature have a lower dielectric constant, in agreement with the results of Figure 5-3-1.

XPS measurements were performed to check the film stoichiometry. Figure 5-3-3 shows the O/Si and C/Si atomic concentration ratio in the film network as a function of the deposition temperature. A pure silica network should have an O/Si ratio of 2. As one of the oxygens bonded to silicon is replaced by CH_3 terminal group, the O/Si and C/Si ratios should approach about 1.5 and 1, respectively. When more oxygen atoms are replaced by CH_3 groups, the O/Si decrease whereas the C/Si ratio increases. On the other hand, the carbon ratio can somewhat decline if the carbon atom is shared between two Si atoms, e.g., a bridging methylene group. At a higher deposition temperature, the O/Si ratio increases up to about 1.5, indicating building of the mono-methyl silica network. On contrarily, the C/Si ratio decreases from 0.73 to 0.635 as the deposition temperature is increased from 250 to 425^{o}C. The result implies that the Si-CH_2-Si moiety was formed in the low-*k* film and it contains more Si-CH_n-Si bridge siloxane network as increasing deposition temperature. Due to the measurement limit of XPS, RBS analysis was performed to analyze atomic composition for the low-*k* films produced from DEMS. As shown in Table 5-3-1, it indicates that a H/C atomic ratio is very close to 3 for DEMS-based low-*k* films in all the deposition temperature ranges. This implies that all hydrogen atoms are mainly bonded with carbon atoms. On the other hand, C and H atomic percentage decrease with increasing whereas Si atomic percentage keeps constant. As a result, C/Si and H/Si ratio decrease for the case of higher-deposition temperatures. The results imply that the low-*k* films deposited at higher temperatures contain Si-CH_2-Si moiety and those deposited at lower temperatures contain

more Si-CH_3 groups. Based on XPS and RBS analysis result, the possible structure of the low-*k* films deposited using DEMS with varying deposition temperatures as follows:

$(CH_3)HSi(OC_2H_5)_2 + O_2 \rightarrow -(H_3C\text{-}SiO_2\text{-}(CH_2)_s\text{-}SiO_2\text{-}O\text{-}SiO_2\text{-}CH_3\text{-})_n-$ at T > 350°C

$(CH_3)HSi(OC_2H_5)_2 + O_2 \rightarrow -(-(H_3C)_x\text{-}SiO_{2-x}\text{-}O\text{-}SiO_{2-s}(CH_3)_s)_n-$ at T < 350°C

Analysis of DEMS-based low-*k* films with varying deposition temperatures by ^{13}C-NMR indicates a dominate peak assigned to Si-CH_3 at ~0ppm with slightly asymmetry on its downfield shoulder likely arising from network carbon groups such as Si-CH_2-, Si-CH- bonds. ^{29}Si- NMR spectra obtained for DEMS-based low-*k* films with 300 and 425°C deposition temperatures are displayed in Figure 5-3-4. The main difference in the DEMS-based low-*k* films spectrum with different deposition temperatures is a relatively smaller presence of trimethylsily {SiO-Si-$(CH_3)_3$} group located slightly downfield of ~0ppm for the case of 300°C-deposition temperature. This suggests that low-*k* films with a lower deposition temperature are more likely to produce multimethyl-substituted Si atoms which may not be as thermally stable as the monomethyl-substituted Si species.

The deposition rate of DEMS-based low-*k* films exhibits a decreasing tendency, indicating that this deposition process is mainly controlled by the surface reaction, and the sticking coefficient of the precursor-mediated molecules on the silicon surface decreases with increasing temperature. The deposition rate verse 1/T for DEMS-based low-*k* films is shown in Figure 5-3-5. It is evident from Figure 5-3-5 that the deposition process may be divided into two processing mechanisms and the transition temperature approaches 350°C, agree with our previous inference. The activation energy can be obtained by using Arrehenius equation. For the deposition temperature below 350°C, the deposition rate is strongly dependent on the deposition temperature and the activation energy is about 0.112 eV. On the other hand, when the deposition temperature is above 350°C, the process is less sensitive to the deposition temperature, as indicated by activation energy of 0.048 eV. The phenomenon

reveals that the two different chemical reactions were carrier out when the temperature is crossed 350^{o}C as shown in Figure 5-3-6. For a lower-deposition temperature (<350^{o}C), the higher fraction of the ~OC_2H_5 will be replaced by the CH_3 and then to form the new chemical branch ~Si-CH_3. The reaction energy can be simplified as the sum of breaking (~Si-OC_2H_5) and forming energy (~Si-CH_3 and Si-O network). Furthermore, if there is more reaction energy, beaking ~CH_3 and ~OC_2H_5 can be further decomposed to form ~CH_2 ~ and ~C_2H_4~, respectively, where they can connect to form -H_3C-SiO_2-$(CH_2)_s$-SiO_2-O-SiO_2-CH_3- bonding. This extra energy is the second energy barrier (0.0048 eV) as shown in Figure 5-3-6. As a result, a lower-deposition temperature condition (<350^{o}C) cannot supply sufficient energy to overcome the second energy barrier and produce the compound B.

Figure 5-3-7 and 5-3-8 show the variation of thickness shrinkage and dielectric constant change of DEMS-based low-*k* films with varying deposition temperatures as a function of annealing cycles and annealing temperatures in N_2 ambient, respectively. It can be seen from Figure 5-3-7 that all DEMS-based low-*k* films remain stable even after 7 exposures to the 425^{o}C annealing process, suggesting that these films deposited at all deposition temperatures ranging from 250 to 425^{o}C are suitable as a ILD layer since the maximum fabrication temperature for each layer of the backend process does not exceed 425^{o}C. Noticeably, the dielectric constant slightly decreases after experiencing 425^{o}C thermal process. However, the thickness shrinkage of low-*k* films is significantly increased as the annealing temperature is increased as shown in Figure 5-3-8. In addition, low-*k* films with a lower deposition temperature undergo larger thickness changes. As the annealing temperature exceeds 600^{o}C, the shrinkage of the low-*k* films deposited at a 250^{o}C reaches as high as 10-30%, whereas

films deposited at 425°C experience rather minor changes when exposed to temperature above 600°C.

A similar change in the dielectric constant was also observed when the low-*k* films were exposed to a higher temperature thermal annealing. The dielectric constants of DEMS-based low-*k* films deposited at all the temperature ranges were degraded after 700°C exposure; the dielectric constant increases to 3.380 and 4.87 from 3.07 and 2.78 for 425 and 250°C deposition temperature, respectively. It can be concluded that the low-*k* films deposited at higher temperatures have better thermal resistance. Conceivably, the deterioration of the *k* value is partial removal of the CH_3 groups, converting the film to a SiO_2 structure. According to the study of Shapiro et al. [73], they indicate that Si-CH_3 and Si-CH_n-Si bonds do not decompose until the annealing temperature rises up to 700°C whereas Si-H bonds would decompose as the temperature reaches 400°C. It implies that the low-*k* films contain less Si-H bonds and more Si-CH_n-Si bonds have sufficiently resistant against heating. As a result, low-*k* films with a higher deposition temperature have superior thermal stability compared to those with at lower deposition temperature due to more Si-CH_n-Si bonds in the higher-deposition temperature films. Additionally, it deserves to be mentioned that the dielectric constant of the low-*k* film slightly decreases after 400-500°C thermal processes. A possible cause of this may be the desorption of less thermally stable groups that contribute negatively to the dielectric constant, or that adsorbed moisture in the film helps to convert Si-CH_n-Si

groups to Si-CH_3 bond. As a result, the post annealing process with 400-500^oC is one possible route to further reduce the dielectric constant of the low-*k* film.

Although DEM-based low-*k* films in this study are not prone to moisture uptake at ambient conditions, exposing the as-deposited low-*k* films to a moisture stress test for 168 h. indicate a distinct difference between the low-*k* films deposited at varying temperatures. For films deposited at temperatures < 350^oC, a minor Si-OH peak in 3500 cm^{-1} appear in the FTIR spectra. Despite the incorporation of CH_3 groups into the Si-O network cause the low-*k* films to be hydrophobic, moisture uptake in low-*k* films deposited at a lower temperature during moisture stress test may be due to its porous structure. It is assumed that the films deposited at lower temperatures are more porous, moisture uptake may be exacerbated by the large surface area of the nano-porous structure.

Hardness and Young's modulus tests are used to estimate the mechanical strength of a film, a crucial property for integration with the chemical mechanical polishing (CMP) processes and multi-layer in Cu dual-damascene architecture. Figure 5-3-9 shows the effect of deposition temperatures on the hardness and Young's modulus of the as-deposited low-*k* films using DEMS as a precursor. The hardness and Young's Modulus become larger at a higher deposition temperature due to CH_n bridging network, more Si-O bonding, and higher film density. At a 250^oC deposition temperature condition, the dynamic hardness and Young's Modulus of the low-*k* films are about 1.56 Gpa and 8.86 GPa, respectively, slightly higher

than other reports [126, 130, 138]. To ensure the performance of multi-ILD layer structure through CMP process, consisting of a dielectric stack: 500 Å SiCN/8 KÅ DEMS-based low-*k* film/CMP oxide buffing (20 seconds) was deposited on the bare-Si wafer repeatedly for a total of 8 layers. An optical microscopy (OM) check was also conducted after completing CMP process of each layer. No peeling was observed even using a lower-deposition temperature (lower mechanical strength) film, suggesting that DEMS-based low-*k* films possess not only good mechanical strength but also excellent adhesion ability to other interconnect materials. Figure 5-3-10 shows the TEM cross-section image of an 8-layer dielectric stack, where DEMS-based low-*k* films were deposited at 250°C. This structure was exposed to seven hating/cooling in total, each 30 min. at 425°C and a pressure cooker test at 2 atm water pressure for 168 h. Even under these very stressful conditions, there were no visible signs of cracking or film delamination observed, indicating good film stability.

For interconnect fabrication processing, thermal treatment is an indispensable step and it may enhance the diffusion of metal (Cu) ion into the adjacent dielectric layer. The inability of a material to withstand these process conditions may result in electrical or reliability issues. Consequently, the effect of deposition temperature of the low-*k* films on the properties and integrate ability of Cu has to be comprehensively evaluated. Figure 5-3-11 shows the Cu sheet resistance with a function of the deposition temperature of the low-*k* films on the

blanket wafers and on the real test structures. From Figure 5-3-11, as the sheet resistance of Cu film show no correlation with the deposition temperature of the low-*k* films, it can be concluded that the resistivity and the texture of Cu are not influenced by the deposition temperature of the low-*k* films.

The Secondary Ion Mass Spectrometry (SIMS) analyses shown in Figure 5-3-12 were used to assess the migration of Cu into the structures described above for DEMS films deposited at varying temperatures. A 250 Å –thick TaN layer and a 2000 Å Cu seed layer were deposited on a silicon substrate; Cu layer was then deposited by electroplating. A 500 Å -thick SiCN dielectric was deposited using PE-CVD method at 400°C followed by Cu deposition. A 1500 Å-thick DEMS-based low-*k* films was capped subsequently. The Cu counts in the SiCN films and bulk low-*k* films for a 425°C low-*k* film deposition condition is slightly higher than that for a 350°C low-*k* film deposition condition. This implies that a higher deposition temperature may drive more Cu ion into barrier film (SiCN) and low-*k* films, which may pose a potential reliability issue.

The electrical performance and reliability of DEMS-based low-*k* films with varying deposition temperatures was quantified on a Cu dual-damascene test structure with a four-layer metallization. The via resistance (Rc; 0.19 μm size) values as a function of the deposition temperatures of DEMS-based low-*k* films were characterized using a 2000 via chain as shown in Figure 5-3-13. The yield of via-Rc was not degraded by sequential

processes and thermal cycles. However, the Rc value increased with each ILD layer and thermal cycles, it is assumed that the cause of these changes may arise from moisture uptake in the film during the fabrication of the next ILD layer. Furthermore, this trend of increase becomes obvious with the increase of the deposition temperature of the low-*k* films. The Rc value for DEMS-based low-*k* films with a 250^{o}C deposition temperature is increased by as much as 10-15% for each thermal process. The same increase trend of the metal line-to-line capacitance in first-level metal layer is observed. After completing the next ILD layer, the line-to-line capacitance is increased by an amount that depends upon the deposition temperature of DEMS-based low-*k* films. The maximum increase is also occurred on the films deposited at 250^{o}C. Low-*k* films deposited at lower temperatures have been shown to be more susceptible to moisture absorption and thermal stresses during fabrication would easily degrade the film's properties. On the other hand, the sheet resistance of Cu line with 0.16 μm width/0.16 μm spacing on the pattern wafers is independent of the deposition temperature of DEMS-based low-*k* films as shown in Figure 5-3-11, similar to the results obtained from the blanket wafers. Figure 5-3-14 illustrates the metal line-to-line leakage current on the first-level interconnects of the test device. Although the Cu/barrier surface dominates the leakage current in Cu dual-damascene structure, the quality of the interconnect insulator may have an impact on the leakage current. It is clear from Figure 5-3-14 that there is a minimum in the leakage current profiles with increasing deposition temperature, whereby

films deposited at 350^{o}C provide the lowest leakage current. This is assumed to be the result of a balance between the improved low-*k* film quality and higher Cu drift into the low-*k* film as the deposition temperature is increased.

5-3-4 Summary

The effect of deposition temperatures on the characteristics of the low-*k* films deposited by PE-CVD using DEMS as a precursor was investigated. FTIR, XPS and ^{29}Si NMR show that the low-*k* films deposited at different temperatures differ in composition and local bonding structure. The films deposited at higher temperatures show a lower amount of C and a preference for monomethylated Si atoms relative to lower deposition temperatures and the higher cross-linking bonding due to CH_n bridging network, resulting in higher hardness strength and thermally stability.

The electrical result of DEMS-based low-*k* films deposited at higher temperatures in ILD test structures was provided good electrical performance, consistent with the result from the blanket wafers. This indicates that the low-*k* film deposition temperature is crucial to be considered as this low-*k* material is implemented in IC manufacturing.

5-4 Oxidation Effect on Low-Dielectric materials

5-4-1 Motivation

To mitigate the signal propagation delay, crosstalk, and dynamic power consumption due to resistance and parasitic capacitance, new materials of metal lines and inter-metal-dielectric (IMD) layers are being developed to replace conventional aluminum and SiO_2, respectively, to improve the performance of decreasing the device sizes [61, 99, 100]. This requires the introduction of low resistivity conductors such as copper and insulators with lower dielectric constant (*k*). Therefore, the ongoing effort has been invested to develop reliable low-*k* materials to implement copper metallization. Recently, one of the low-*k* candidates is the material comprised mainly of Si, C, O, H, and/or F prepared by plasma enhanced chemical vapor deposition (PE-CVD) method. These include F-doped oxide, or fluorinated silicate glass (FSG, Si_xOF_y); and C-doped oxides, or organosilicate glass (OSG, SiCO:H) [147]. The former, FSG (*k* = 3.4~3.7), with a slightly lower dielectric constant than conventional undoped silicate glass (*k* = 3.9~4.1) [148-150], has been successfully demonstrated its benefits as a feasible low-*k* material [117, 118, 151-153] into IMD application with suitable fluorine concentration (< 5 %) [154, 155]. The latter, the OSG film, has become one of the main candidates for potential applications in 130 nm technology node due to its lower dielectric constant (*k* = 3.0 ~ 2.1) [119, 156, 157] with good thermal and mechanical stability.

Many precursors have been studied for the deposition of PE-CVD SiCOH films, such as trimethylsilane, tetramethylsilane, tetramethylcyclotetrasiloxan, dimethyldimethoxysilane, and Hexamethyldisiloxane [122, 158]. However, from the point of view of process integration, this new low-*k* material, which has low density and high porosity, has not demonstrated sufficient mechanical properties, such as high hardness and elastic modulus that are required to withstand the mechanical stress imposed by the chemical-mechanical polishing process. Additionally, it needs to possess high resistance to stress migration and dry etching, without raising the dielectric constant.

In this study, DEMS was selected as a precursor for the deposition of SiCOH film. It has been suggested that the precursor provides the best balance between the electrical and mechanical properties [145, 146]. The SiCOH films were deposited at various oxygen flows, and the optical refractive index, bonding configuration, mechanical properties, and electrical strength of the films were investigated in this study. The structural alteration mechanism that leads to the improved mechanical properties and lower dielectric constant are proposed and discussed in this contribution.

5-4-2 Experimental Procedures

The deposition of the SiCOH films was performed in a PE-CVD system with the operating rf of 13.56 MHz. The thin films were deposited on *p*-type 200 mm silicon wafers with (100) orientation Diethoxymethylsilane (DEMS, Air Products and Chemical, Inc.) was carried in vapor phase by inert helium (He) gas to the reaction chamber. The flow rate of He gas and DEMS flow were controlled at 300 sccm and 1500 mg min^{-1} (equal to 250 sccm), respectively. The DEMS precursor gas was mixed with oxygen (O_2) in the deposition process. The pressure and RF power were maintained at 533 Pa and 500 W, respectively, throughout the deposition process. The deposition temperature and O_2/DEMS flow rate ratio were varied between 350°C and 425°C and 0~1, respectively, where O_2 flow rate was varied from 0 to 250 sccm.

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The thickness and refractive index (at 633 nm wavelength) of the as-deposited films were analyzed for by reflectometer and/or ellipsometer using the Nano-Spec® 9100. Forty nine-point measurements were performed on each wafer to acquire the mean value. Chemical bonding and composition of the film were investigated using Fourier transform infrared spectroscopy (FT-IR) [Bio-Rad Win-IR PRO], and photoelectron spectroscopy (XPS),

respectively. FT-IR was performed at a resolution of 4 cm^{-1}, each spectrum being the average signal over 64 scans with the background corrected to a silicon reference. An MTS Nano-Indentation XP system was utilized to measure the nano-hardness and modulus of the deposited SiCOH films. The sample thickness for nano-hardness measurement was approximately 1 μm. The penetration depth was about 100 nm at ~ 0.3 mN down force, and each hardness entry is the average over 5 measurements. In electrical characterization, the dielectric constant and leakage current of the SiCOH films were measured by capacitance-voltage measurements with a SSM Inc. Hg probe 5100 CV system at 1 MHz. The errors of the capacitance and the mercury electrode area are less than 1%.

5-4-3 Results and Discussions

Figure 5-4-1 shows the deposition rate of SiCOH films deposited at different temperatures (350^{o}C and 425^{o}C) as a function of the O_2/DEMS flow rate ratio. The deposition rate is increased with O_2/DEMS flow rate ratio and decreased with the deposition temperature. In the PE-CVD process, the deposition rate depends on the activated reactant concentration on the substrate surface. The increase of the oxygen flow rate in the deposition process induces the increase in reactivity of DEMS, and a higher proportion of plasma-generated species having sufficient bonding energy has been incorporated into the film. In addition, as O_2/DEMS flow rate ratio is increased beyond 0.4, the effect of oxygen content on the growth rate of SiCOH films becomes significantly obvious. Moreover, it is found that the growth rate is increased by a factor of 4 times as the O_2/DEMS flow rate ratio up to 1.0. The change in deposition rate at different deposition temperatures can be explained by the changes in desorption of the reactant with different temperatures. The deposition rate of the SiCOH films exhibits a decreasing tendency with temperature, indicating that this deposition process is surface reaction control, and the sticking coefficient of the

precursor-mediated molecules on the silicon surface is decreased with increasing the temperature. Figure 5-4-2 exhibits the refractive index of the SiCOH films deposited at various temperatures and oxygen flows**.** The refractive index of SiCOH films is averaged over 49 measured points per wafer which exhibits a decreasing trend with the O_2/DEMS flow rate ratio regardless of the deposition temperature. The results suggest that the properties of the deposited films, such as composition, density, and bonding configuration, have been significantly changed by the addition of oxygen. It is well known that the refractive index is closely related to the density of materials, being lower at lower density [142]. A lower density is attributed to the higher porosity within the film. Therefore, the difference of the refractive index with O_2/DEMS flow rate for SiCOH films in this study is attributed to the variation of film density which is caused by Si-O-Si caged structure variation obtained from FTIR measurements.

To further investigate the variation in growth rate and refractive index, the bonding states of the SiCOH composite films were analyzed by IR absorption spectra over the range of 400 – 4000 cm^{-1}. Figure 5-4-3 shows the FT-IR raw spectra for a series of SiCOH film of 300 nm thickness deposited at 425^oC. The Si-O stretching cage-structure peak near 1132 cm^{-1}, Si-O network stretching network peak is near 1040 cm^{-1}, Si-O bending cage-like peak near 863 cm^{-1}, and the Si-O bending network peak is near 830 cm^{-1}. In addition, the Si-CH_3 stretching and bending peaks are near 1270 cm^{-1} and 802 cm^{-1}, respectively. The weakly absorption methylene bridged silicon stretch is located at 1360 cm^{-1}. CH_x peak is near 2975 cm^{-1}, and the weakly absorbing Si-H bands are located at 2240 and 2170 cm^{-1} due to (Si-O_3)-H and R-(Si-O_2)-H, respectively.

It is observed from Figure 5-4-3 that there is little change in the Si–O stretching mode while the Si-O stretching cage-like mode is increased as the O_2/DEMS flow rate ratio is

increased. The network structure reduces the density of the SiCOH film. Influences of process parameters on absorption of Si-O-Si stretching mode in the films are shown in Figure 4. It can be found that the absorption of Si-O-Si stretching mode shifts to a higher wave number with increasing the O_2/DEMS flow rate ratio, and to slightly a lower wave number with decreasing the deposition temperature. The increasing wavenumnber of the Si-O absorption is due to a changing bond angle of the Si-O netrwork, approaching to that of SiO_2. As a consequence, the Si-O-Si bonds are weakened and become less rigid and more stretchable, resulting in a higher stretching frequency as shown in Figure 5-4-4. In this case, higher deposition temperature increases the frequency of the stretching Si-O-Si bonds in the structure of SiCOH films. This implies that the electronic defects are reduced and bond angle are adjusted at high deposition temperature so that the Si-O-Si bond strength is restored to certain degree, and the effect of oxygen is enhanced.

As further investigated in 950-1250 cm^{-1} wavenumber, it reveals that the Si-O-Si stretching peak is divided into two peaks, the main peak at around 1070 cm^{-1} (Si-O network), and the shoulder peak at around 1130 cm^{-1}. Si-O (cage) is typically the main cause for the shoulder at higher wavenumbers, but has C-O groups and other species that are obscured by the strong Si-O absorbance. It becomes increasingly difficult to differentiate the two peaks at higher O_2 ratio due to the blue-shift and the overlap of shoulder peak with the main peak. Pai *et al.* [142] suggested that the shoulder peak is due to in-phase and out-of-phase movements of the Si-O-Si bond. Grill *et al.* [122] and Chou *et al.* [152] proposed that the shoulder peak is related to the porosity of an oxide with caged Si-O bonds and the reflection of enhanced porosity in the films. The addition of oxygen results in microvoids that account for the appearance of the shoulder peak.

The peak intensity of CH_x-group (around 1270 cm^{-1} and 2900 cm^{-1}) shows no significant change or trend with increasing O_2/DEMS flow rate ratio (Figure 5-4-5). However,

the addition of oxygen in the deposition process slightly increases the organic contribution (CH_x-group), which decreases electrical and ionic polarization of the deposited films. Therefore, the dielectric constant of the deposited film is slightly decreased with the addition of oxygen in the deposition process.

In the FT-IR analysis of 2100-2300 cm^{-1}, there are two obvious peaks observed in 2170 cm^{-1} and 2240 cm^{-1}, corresponding to R-(Si-O_2)-H and (Si-O_3)-H bonds. As shown in Figure 5-4-5, there is a significant reduction in the Si-H content with increasing oxygen. It is worth mentioning that the hydrogen reduction is attributed to the reduction of R-(Si-O_2)-H group. Additionally, the shape of the absorbance indicates a shift to more networked as oxygen is added to the deposition process. On the other hand, as comparing the Si-CH_3 absorbance, there is a shift and narrowing of the absorbance with adding and increasing the amounts of oxygen. It is inferred that DEMS contributes more Si-$(CH_3)_2$ and Si-$(CH_3)_3$ groups when there is no oxygen in the deposition. As oxygen is added, there is a preference for more Si-(CH_3), or mono-methylsilane groups. This well agrees very well with the ^{29}Si NMR data which shows the same effect when oxygen is added. The amount of methyl groups attached to Si does not change with the addition of oxygen. This indicates that the addition of oxygen does not directly affect the methyl group via oxidation, but it prevents the production of Si-$(CH_3)_2$ and Si-$(CH_3)_3$, essentially converting to mono-methylsilane groups. A particular change is the loss of the absorbance at 1360 cm^{-1}, indicating that the influence of addition of oxygen is the reduction of Si-CH_2-Si groups. As a result, when oxygen is added to participate in the deposition process, there are two main outcomes to balance the overall effect on the mechanical properties of the films. One is the loss of Si-H (no contribution to network) and the other is the loss of Si-CH_2-Si (positive contribution to network).

The effects of O_2/DEMS flow rate ratio and deposition temperature on the relative carbon content incorporated into the SiCOH film is shown in Figure 5-4-5. The relative

bonding concentration of carbon incorporated in SiCOH films is calculated by the following equation normalized to the peak Area of the Si-O-Si stretch mode:

$$\text{Relative [C] content (\%)} = \{A_C/(A_C + A_{Si\text{-}O})\}\times 100\% \quad \textbf{(5-4-1)}$$

where $A_{Si\text{-}O}$, and A_C are the peak height of the stretching vibration mode of Si-O-Si at 1060 cm^{-1}, and $Si\text{-}CH_3$ at 1270 cm^{-1}, respectively. The carbon content is increased with decreasing the deposited temperature and increasing the oxygen flow. The carbon content is reached saturation as O_2/DEMS flow rate ratio is up to 0.4. On the other hand, from the results of elemental analysis by XPS shown in Table 5-4-1, it exhibits a slightly decrease in the carbon element with increasing the O_2/DEMS flow rate ratio. This result suggests that the increase in O_2/DEMS flow rate ratio in the SiCOH films is accompanied with the increase of $Si\text{-}(CH_3)$ or mono-methylsilane groups and the decrease of $Si\text{-}CH_2\text{-}Si$ groups in the SiCOH film.

Mechanical hardness and modulus of elasticity of the resulting SiCOH films are plotted as a function of O_2/DEMS flow rate ratio at 350°C and 425°C deposition temperature shown in Figure 5-4-6. The hardness variation with O_2/DEMS flow rate ratio is attributed to the porosity of this film due to the existence of Si-O-Si caged-structure by oxygen incorporation. At the O_2/DEMS flow rate ratio of 0.2-0.3, the film is demonstrated the lowest hardness (1.79 Gpa). Due to the reduction of $Si\text{-}CH_2\text{-}Si$ group, positive contribution to network, the hardness of the film is slightly increased as the O_2/DEMS flow rate ratio is above 0.4. It is worth noting that the hardness (1.7 G ~ 2.2 GPa) of the SiCOH films at 425°C is higher than that deposited at 350°C (1.1~ 1.8 GPa) due to the abundance of Si-O-Si bonds at higher temperatures. This helps the SiCOH films restore part of the bond integrity and tetradral structure of a perfect SiO_2, leading to the improved mechanical properties. Additionally, it is found that the SiCOH film deposited from the DEMS precursor have higher hardness than OSG (~ 1.5 GPa) deposited by methylsilane precursors.

Dielectric constant is a frequency dependent, intrinsic material property. Figure 5-4-7

shows the dielectric constant (relative permittivity) measured at 1 MHz of the thin films investigated in this study. As shown in Figure 5-4-7, when oxygen is incorporated into the deposition chamber, the dielectric constant is decreased and reaches a minimum value at the oxygen flow rate of 100 sccm. The reduction of the dielectric constant of the SiCOH film caused by the electronic contribution is attributed to a decreased density of the network due to higher Si-O cage structure while the organic content of the film remains unchanged. This reflects the decreased refractive index of the deposited film. When the oxygen flow rate is reached 100 sccm, the dielectric constant shows a minimum value. While the oxygen flow rate exceeds 100 sccm, the dielectric constant is increased slightly with the increase of the oxygen flow rate. It is deduced that the dominant factor in the overall dielectric constant is turned into the ionic contribution because Si-O bond is more polarized than Si-C bond [152]. Additionally, an extra benefit is observed as the oxygen is added in the deposition process. Since the non-uniformity in dielectric constant causes the large variation in device performance, depending on the location on the wafers, more uniform dielectric constant across the wafer is essential. As oxygen is incorporated into the reaction, the variation of dielectric constant at the center and edge location of 8-inch Si-wafer is about 0.1-0.2, lower than 0.4 without oxygen addition. It may be caused by the uniform plasma density across the wafer as O_2 is incorporated into the reaction processes. The within-wafer uniformity of thickness and refractive index also reveals the same results.

The leakage currents on the electric field for SiCOH films deposited at varying oxygen flows rate and deposition temperature were evaluated. As shown in Figure 5-4-8, there is an increasing trend of the leakage current with raising the O_2/DEMS flow rate ratio. The leakage currents are in the range of 10^{-8}-10^{-9} A/cm^2 at 1 MV/cm, depending on the O_2 flow rate. This value is slightly lower than that of other PE-CVD low-*k* films [119, 158]. The reason of of increased leakage current by adding O_2 is not clarified yet. However, it is speculated to be the

increase of the microvoid structure. As for temperature effect, lower deposition temperature results in more stretchable Si-O-Si bonds, more CH_x groups, and more porosity present in the films. The leakage current of the SiCOH film is, therefore, decreased at a lower deposition temperature.

5-4-4 Summary

The composition, bonding configuration, mechanical, and electrical properties of SiCOH films using diethoxymethylsiliane (DEMS) and oxygen (O_2) as a precursor by PE-CVD method have been investigated. The refractive index of SiCOH increases with increasing deposition temperature but decreases with increasing oxygen adding to the deposition recipe. The addition of oxygen dramatically enhanced the plasma deposition rate of DEMS. The as-deposited films also show lower dielectric constant and decreased mechanical hardness and modulus. The effect is reduced at higher temperatures. The results can be accounted by the changes in composition and bonding configuration, as determined from FT-IR and elemental analyses.

5-5 Heat, Moisture and Chemical Resistance on Low Dielectric Constant (Low-k) film using Diethoxymethylsilane (DEMS) prepared by plasma enhanced chemical vapor deposition

5-5-1 Motivation

As minimum device features shrink below 180 nm, the increase in propagation delay, the resistance and capacitance delay (RC) of the interconnect has become a limiting factor in

ultra-large scale Integration (ULSI) device performance. Since RC delay is a product of the resistance in the metal interconnect (R) and the capacitance between the metal line (C), incorporating copper (Cu) wiring and low-*k* dielectric to replace the conventional AlCu/SiO_2 into interconnect technology can effectively reduce the RC delay [61, 99, 121].

Various low dielectric constant materials have been proposed to decrease the time delay caused by capacitance. Recently, organosilicate glass (OSG), deposited by PE-CVD method using various organo-precursors, such as methylsilane (MS), Tetramethylsilanetetrasiloxane (TOMCATS) and Diethoxymethylsilane (DEMS), is the most promising low-*k* dielectric candidate [65, 121, 137, 141]. Among these precursors, DEMS precursor is a strong candidate based on the excellent film properties. Diethoxymethylsilan (DEMS ; H-Si(CH_3) (OC_2H_5)$_2$)-based low-*k* films not only have a lower dielectric constant (*k*=2.8-3.0) but also have a greater hardness (higher cross link) as it contains an O:Si ratio of 2:1 in the precursor produced optimum films [136].

However, during the interconnect fabrication process, thermal cycle and photoresist stripping are the indispensable steps. Therefore, the physical (thickness and refractive index) and electrical properties (dielectric constant and leakage current) of the low-*k* interconnect dielectric are needed to be resistance against heat, moisture and chemical stress in order to prevent the degradation during the interconnect fabrication process. Furthermore, to ensure the high reliability performance of the high-speed ULSI, the moisture resistance is essential to avert moisture penetrating from the outside the package[66, 138, 160].

In this work, the stability of the low-*k* films deposited using a DEMS precursor against heat, moisture and chemical stresses is clarified. The low-*k* films prepared using DEMS or DEMS/O_2 reactant gas are submitted to reliability tests to distinguish the stability divergence

for the effect of the addition of O_2. Furthermore, the electrical measurements and material analyses have also been used to evaluate the low-*k* film before and after the reliability tests.

5-5-3 Experimental Procedures

Material prepared- All thin film deposition was performed on an Applied Materials Producer system with a 200 mm Producer chamber. The thin films were deposited on *p*-type (100) silicon substrates by radio frequency (13.56 MHz) PE-CVD with Diethoxymethylsilan (DEMS, CVD precursor) carried to the reaction chamber in the vapor phase by inert helium (He) gas. The chamber pressure and RF power were maintained at 6 Torr and 700 W, respectively, throughout the deposition process. The deposition temperature and He flow were kept 400^{o}C, and 150 sccm, respectively. The DEMS flow rate was fixed at 1500 mgm and oxygen (O_2) flow was varied from 0 to 250 sccm (herein the O_2/DEMS ratio was 0~0.175).

Reliability Test- To determine the thermal stability, the films were annealed for 1h in a nitrogen ambient at temperatures ranging from 400 to 800^{o}C. Moreover, to mimic the thermal stresses encountered during Cu interconnects fabrication process; thermal annealing at 425^{o}C in nitrogen ambient for 1 h was performed 7 times. For the humidity test, a pressure cooker test (PCT) was carried out at 120 ^{o}C, 100% relative humidity, and 2 atmosphere pressure for 168 h. To test the impact of O_2 plasma on the film properties, the as-deposited DEMS-based films were exposed to O_2 plasma environment in a cathode-coupled rf asher. The pressure and RF power were 10 mTorr and 200 W, respectively, and the process time was set at 60 s.

Analysis Method- The low-*k* films were analyzed for thickness and refractive index (RI,

at 633 nm) by reflectometer (SCI FilmTek) and/or ellipsometer (Nano-Spec®9100) before and after stressing. The thickness change is defined herein as

$$Thickness\ change(\%) = \frac{THK_{stressing} - THK_{As.dep.}}{THK_{As.dep.}} X100\%$$

where $THK_{stressing}$ and $THK_{As.dep.}$ represent the measured thickness after stressing and as-deposition.

Transmission FT-IR spectra were measured the chemical bonding of the film using Bio-Rad spectrometer at 4 cm^{-1} resolution. All spectra are an average of 32 scans and background corrected to a silicon reference. The dielectric constant (*k*) and leakage current density were measured by an SSM mercury probe cyclic voltammeter (CV) system (SSM 495) at 1 MHz frequency. The *k* value was obtained from the average of 9 sites measurement.

5-5-3 Results and Discussions

The dependence of the stress behavior of the as-deposited DEMS-based low-*k* films as a function of O_2/DEM ratios is shown in Figure 5-5-1. The intrinsic stress of the DEMS-based low-*k* films becomes more tensile as the O_2 flow rate is increased. Furthermore, thermal stability had been evaluated by stress/temperature analysis. Figure 5-5-2 shows the stress hysterisis curves of the low-*k* films with polymerization of DEMS and oxidation of DEMS and O_2. It reveals that the stress shift between the first thermal cycle and the second cycle was suppressed for the low-*k* films prepared by DEMS and O_2. Minimal change in stress is observed for low-*k* films deposited using DEMS and O_2. The shift magnitude is 2.0E07 dyne/cm^2, significantly smaller than that with pure DEMS deposition (3.0E09 dyne/cm^2).

This result implies that the low-*k* films deposited using DEMS and O_2 have better thermal stability.

In the Cu integration processes, there are at least 7-8 layers interconnect dielectric deposition with the deposition temperature of around 400^{o}C. The dependence of the heating cycles on the degradation of the thickness and dielectric constant of DEMS-based low-*k* films with various DEMS/O_2 ratios are compared in Figure 5-5-3 and 5-5-4, respectively. For DEMS-based low-*k* films, the thickness remains constant after performing 425^{o}C annealing cycling independence of DEMS/O_2 ratios shown in Figure 5-5-3. This implies that low-*k* film deposited using DEMS precursor has a higher bonding strength when subjected to the heating tests related to other OSG films prepared by other precursors [107, 130, 131]. On the other hand, it can be seen from Figure 5-5-5 that the change of the dielectric constant of low-*k* films with DEMS/O_2 was found to behave differently to that with DEMS only. The dielectric constant of the low-*k* films deposited only using DEMS gradually increase with increasing the 425^{o}C heating cycles. In contrast, as O_2 was incorporated into the reaction, the dielectric constant of DEMS-based low-*k* films almost retains the same value, even after the seven cycles of the 425 ^{o}C heating test. To further investigate the heating resistance of DEMS-based low-*k* films, different heating temperatures, ranging from 400 to 800 ^{o}C, were performed. The influence of the heating temperatures on the change of thickness and the dielectric constant of DEMS-based low-*k* films for different DEMS/O_2 ratios are shown in Figure 5-5-5 and 5-5-6,

respectively. The behavior is similar to other OSG low-*k* films using other precursors [130, 131], the dielectric constant of the low-*k* films deposited with DEMS or DEMS/O_2 maintain a stable value (*k*=2.8-3.2) at temperatures up to 600^{o}C. Moreover, the dielectric constant of low-*k* films deposited only using DEMS degrade to 3.6 as the heating temperature is increased to 700^{o}C and sharply increases to 5.0 as the temperature approaches 800^{o}C. On the other hand, the dielectric constant of low-*k* films deposited using DEMS/O_2 does not degrade until the annealing temperature is increased to 800^{o}C. This indicates that DEMS-based low-*k* films with O_2 as an oxidant gas have a superior thermal resistance to that deposited only using DEMS precursor. This result seems to imply that low-*k* films deposited using DEMS and DEMS/O_2 have different bonding structures, which exhibits a different thermal resistance. To further investigate the difference in the bonding structure for these low-*k* films, FTIR and X-ray Photoemission spectroscopy (XPS) analyses were conducted depicted in pervious paragraph. Low-*k* film deposited using only DEMS gas has more –CH_3 terminal bonds and more C-$Si_{4-X}H_x$ (x<2) bonds to form a cross-linking structure. In contrast, the deposited low-*k* films contain less C-$Si_{4-X}H_x$ (x<2) bonds and mono-mthylsilane group to form a micro-void structure as O_2 gas was added to the reaction. The speculated schematics of the low-*k* film chemical bonding structures deposited using (I) DEMS, (II) DEMS/O_2 are shown in Figure 5-5-7. Furthermore, it is worth to note that the dielectric constant of DEMS-based low-*k* films deposited using DEMS/O_2 further decrease after annealing with temperature below 600^{o}C.

The decreasing dielectric constant could be attributed to the desorption of the small amount water in the film and rearrangement of the amorphous structure during annealing. It was observed from FTIR spectra that no significant change in the concentration of C-H bonds and Si-CH_3 bond is thermally stable up to 600^{o}C. We believe that the decreasing dielectric constant of low-*k* films deposited by DEMS/O_2 was a result of the formation of open ring structures in the films caused by the loss of water and CH_x organic materials during annealing at 400-600^{o}C. Since the thermal resistance of Si-CH_x-Si bonds is lower than Si-CH_3, the Si-CH_x-Si bonds were converted to CH_x organic materials and desorped during 400-600^{o}C annealing. This is positive to reduction the dielectric constant, but is negative to the thickness stability. As the annealing temperature is increased to 700^{o}C, the Si–CH_3 absorbance peak dramatically decreases and there is an increase in the oxide character of the film, and a loss of methyl groups after the annealing process as shown in Figure 5-5-8. Interestingly, the enhancement in Si-O characteristics is less for the low-*k* films deposited using DEMS/O_2 film, which also showed much smaller increases in the dielectric constant. This suggests that the Si-CH_3 bonding did not decompose until the thermal temperature above 700^{o}C. In addition, low-*k* film deposited only using DEMS, where Si is bonded with multi-methyl group (-CH_3) bonding would degrade easily during the higher temperature annealing.

The change in the dielectric constant of DEMS-based low-*k* films under the moisture stress test in terms of O_2/DEMS ratios is shown in Figure 5-5-9. It indicates a slightly

increase in the refractive index and the dielectric constant after a 168 h PCT for two different deposition conditions. Compared with low-*k* films deposited using 3MS as precursor [73], low-*k* films deposited using DEMS as precursor shows a better moisture resistance, implying that this film has a surface hydrophobic property as a result of more $–CH_3$ terminal bonds. Additionally, the dielectric constant of low-*k* film deposited only using DEMS gas increases to 2.93 from 2.86, which is slightly lower than that prepared by DEMS/O_2 with a dielectric constant of 2.96. More surface hydrophobic -CH_3 bonds in low-*k* films prepared using DEMS gas, hindering the moisture penetrate into the film, causes this divergence. More interesting to note, the stress of low-*k* film tends to decline to neutral value after the moisture test. Additionally, Thermal Desorption Spectrum (TDS) analysis indicated that the H_2O peak was observed at about 250^oC and the desorption amount of H_2O was greater for the low-*k* films prepared using DEMS/O_2 reaction. These imply that the deposited low-*k* film still contains moisture in terms of physical absorption and low-*k* film produced only using DEMS gas have better moisture resistance, consistence with the previous observation.

In the interconnect integration fabrication, the ILD layer etching and photo-resist stripping processes are indispensable steps. Figure 5-5-10 shows the etching rate of DEMS-based low-*k* film as a function of O_2/DEMS ratios, performed using Ar/C_5F_8/N_2 gas. The etching rate of DEMS-based low-*k* films slightly increases with an increasing O_2/DEMS ratio. The higher etching rate for DEMS-based low-*k* films with a higher O_2 flow rate is

suspected to porosity structure in the low-*k* film; that is, the film is less dense (refractive index is lower for DEMS-based low-*k* films with a higher O_2 flow rate). On the other hand, the dielectric constant of post-etching DEMS-based low-*k* films almost remains the stable value as the as-deposited films independent of the O_2 flow rate. This indicates that low-*k* film deposited using DEMS and O_2 gas can efficiently withstand the treatment of the etching chemical gas.

In conventional photo-resist stripping step process, O_2 plasma ashing is commonly implemented because of its better efficiency in removing the polymer. However, all porous low-*k* films would suffer a degradation of the dielectric constant after exposing O_2 plasma ashing process[17]. Therefore, the effect of O_2 plasma ashing on low-*k* films prepared by DEMS or DEMS/O_2 was investigated in this study. Figure 5-5-11 shows the change of thickness and the dielectric constant of DEMS-based low-*k* film as a function of O_2/DEMs ratios. The thickness reduction can be negligible since the maximum thickness reduction is about 2.5% for films deposited only using DEMS reactant. Additionally, the thickness reduction is less 1% for low-*k* films deposited using DEMS/O_2 reactant. A plausible explanation is that terminated methyl groups in DEMS-based low-*k* films are oxidized in the O_2 plasma condition, in line with the following Eq. (5-5-1)~(5-5-3):

$$\text{-Si-CH}_3 + \text{H}_3\text{C-Si-} + \text{O} \rightarrow \text{-Si-OH} + \text{OH-Si-} + \text{CO} + \text{H}_2\text{O} \quad \textbf{(5-5-1)}$$

$$\text{-Si-OH} + \text{OH-Si-} \rightarrow \text{-Si-O-Si-} + \text{H}_2\text{O} \quad \textbf{(5-5-2)}$$

$$-Si-CH_n-C-Si- + O \rightarrow -Si-O-Si- + CO + H_2O \quad \textbf{(5-5-3)}$$

The forming -Si-O-Si- bonds are almost as dense as -Si-C-Si- as the bond length of Si-O is similar to that of Si-C bonds. As a result, the thickness change under O_2 oxidation can be negligible, which might account for the lower reduction in the DEMS/O_2 reaction because the low-*k* films deposited using DEMS/O_2 contains more Si-C-Si bonds.

Exception of the above oxidation, O_2 plasma treatment has also been found to resulting in dangling bonds arising from the enhanced breaking of Si-H bonds by oxygen radicals, and damage through the following reaction, resulting in increased dielectric constant.

$$-Si-H + O \rightarrow -Si-OH \quad \textbf{(5-5-4)}$$

In contrast to the thickness reduction, the degradation in the dielectric constant of low-*k* films deposited using DEMS/O_2 gas become serious as O_2 flow rate is increased. On the other hand, low- *k* films deposited using DEMS gas show a lower change in the dielectric constant.

To solve the dielectric constant degradation issue for the deposited low-*k* films, the dielectric constant of DEMS-based low-*k* films with post O_2 plasma treatment was measured after dry etch method, as shown in Figure 5-5-12. The purpose of dry etch is to remove the dense layer, which is oxidized on the top of low-*k* film during the O_2 plasma ashing process. As can be seen, after the dry etch, the dielectric constant of low-*k* film deposited using DEMS or DEMS/O_2 reduced to about 3.3, which is close to the original as-deposition value. It clearly shows that the low-*k* film inside is not degraded during the O_2 ashing process. SEM

also displays the distinct two-layers inside the low-*k* film after the O_2 plasma ashing. The depth of the oxidation film increases with increasing O_2 exposure time. This dense surface can be removed during sputter etching prior to the metal deposition in the practical fabrication process. As a result, control of the O_2 plasma time and pre-sputter etching is a feasible method for recovering the dielectric constant. Another approach to alleviate dielectric constant degradation is using NH_3 or N_2 plasma treatment on the as-deposited low-*k* films. This N_2 plasma treatment would induce the N atom doping in low-*k* films and replace the Si-H bonds to form a thin Si-N layer on the film surface. The dielectric constant of low-*k* films prepared by DEMS/O_2 is slightly increased from 2.78 to 2.86 after N_2 plasma treatment. The new forming layer can effectively impede the attack on the dielectric constant of low-*k* film during the O_2 plasma ashing process. Figure 5-5-13 shows the leakage current density at 2 MV/cm and dielectric constant of the N_2 plasma treated low-*k* films before and after being exposed to the O_2 plasma treatment. The leakage current density remains at a stable value of about 1.40E-8 A/cm^2 at 2 MV/cm, which is slightly lower than the as-deposited low-*k* film (1.65E-8 A/cm^2 at 2 MV/cm) dut to the formation of Si-N bonds. In addition, the dielectric constant of N_2 plasma-treated low-*k* films deposited with 0.05 ratios of DEMS/O_2 maintains the stable value when compared to film without N_2 plasma treatment. The results indicate this functional group produced by N_2 plasma treatment ensures that the low-*k* films have a superior electrical performance to against O_2 plasma ashing damage.

5-5-4 Summary

The resistance to heat, moisture stress and chemical test for organo-silicate glass (OSG) low-*k* film deposited using DEMS and various O_2 flow was investigated. Low dielectric constant organo-silica-glass (OSG) film deposited using DEMS and O_2 is shown to be the most reliable. The dielectric constants are stable even after a heating test at 700^{o}C and a pressure cooler test for 168 h, and are superior to other PE-CVD low-*k* films deposited by other precursors. This excellent stability ensures the low-*k* film deposited using DEMS is suitable for application as multilevel interconnects, showing long-term reliability after fabrication. However, the O_2 plasma ashing process leads to a dielectric degradation in deposited low-*k* film during photoresist removal processing. A N_2 plasma treatment is proposed as a method of preventing the damage from an O_2 plasma attack on the low-*k* film deposited using DEMS/O_2 gas

Table 5-1-1. Physical properties data for He and Ar Carrier gas.

Carrier gas	Ionization Energy (eV)			Molecular Weight (a.m.u)	Lennard-Jones Collision diameter(Å)	Mass diffusivity (cm^2/s)	Thermal conductivity (cal/cm-s-K)
	First	Second	Third				
He	24.59	54.42		4	2.551	13.43	4.68×10^{-4}
Ar	15.76	27.63	40.74	40	3.542	3.15	9.03×10^{-4}

* Ionization energy denotes the Ionization energy of the *n*th electron.

Table 5-2-2. Percentage of element from XPS Quantification (%).

Carrier gas	Take-off 0°			Take-off 60°		
	O	C	Si	O	C	Si
He	34.7	30.9	34.4	34.3	33.1	32.7
Ar	33.1	31.8	35.1	33.4	34	32.6
STD	33.6	31.6	34.8	33.1	33.2	33.8

Table 5-3-3. Related Binding energy and Percentage for Si^{2p} peak.

Si(2p)	Si^{4+}-O_4	Si^{4+}-O_3	Si^{4+}-O_2	Si^{4+}-O_1	Si^{4+}-O_0
Binding Energy(eV)	103.4	102.2	101.1	100.2	99.1
He	2%	23%	49%	21%	5%
Ar	2%	24%	47%	21%	6%
STD	2%	24%	48%	21%	6%

Gas Phase Reaction:

Reaction gas : **Intermediates :**

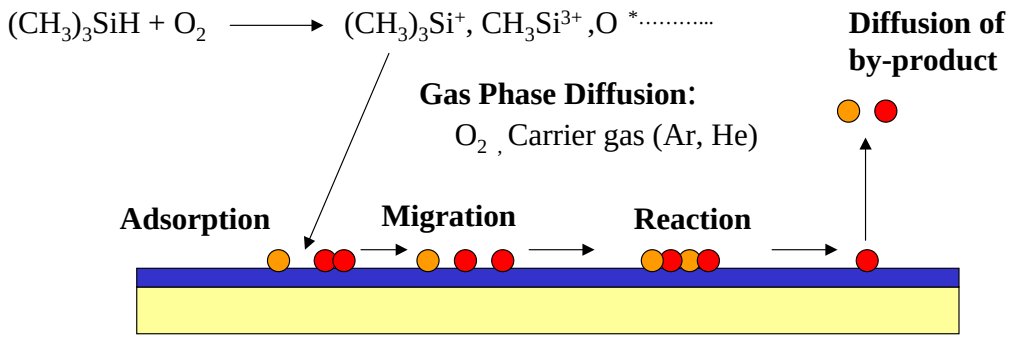


Figure 5-1-1. A series of reaction process steps of the low-*k* film formation using 3MS and O_2.

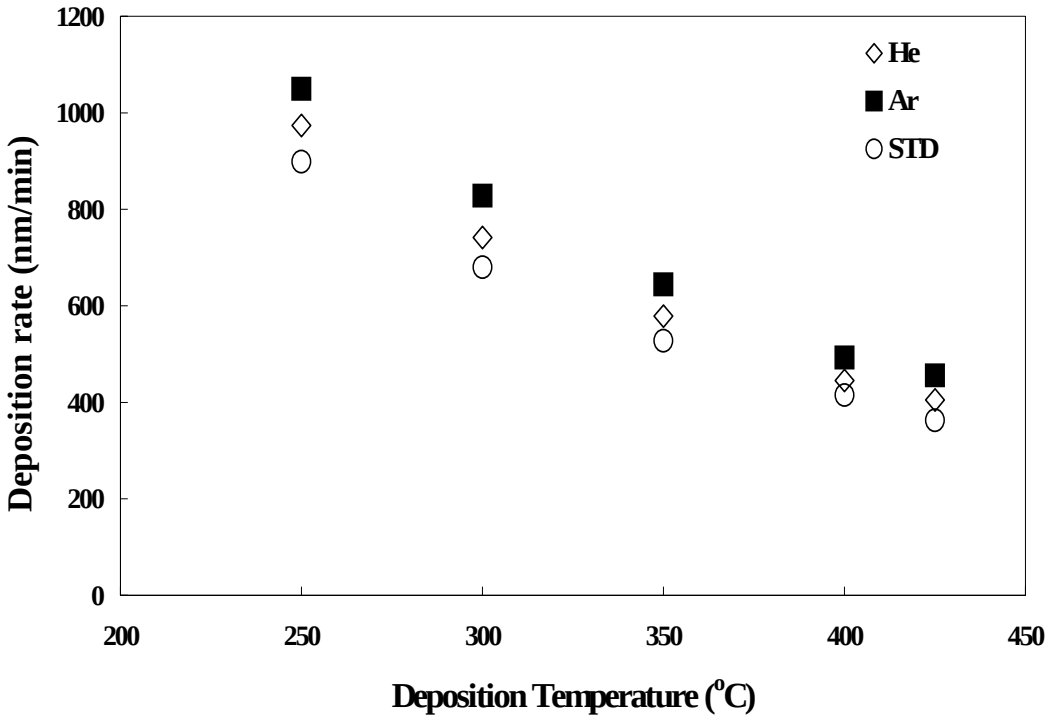


Figure 5-1-2. The effects of the deposition temperature on the deposition rate of the low-*k* film processes.

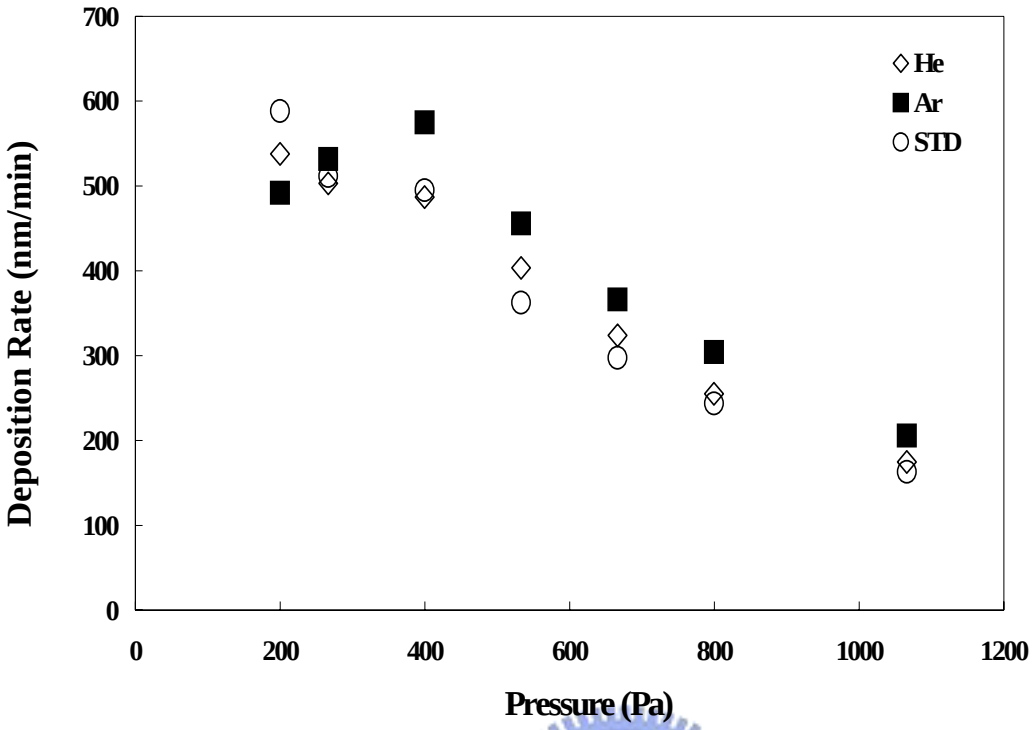


Figure 5-1-3. The effects of the deposition pressure on the deposition rate of the low-*k* film processes.

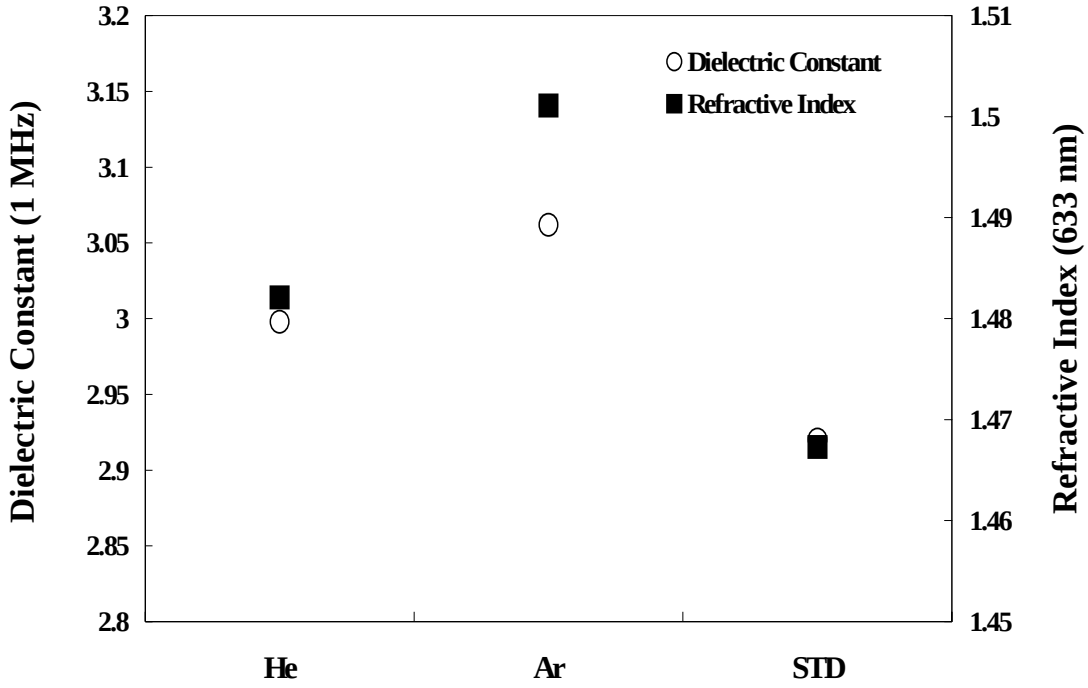
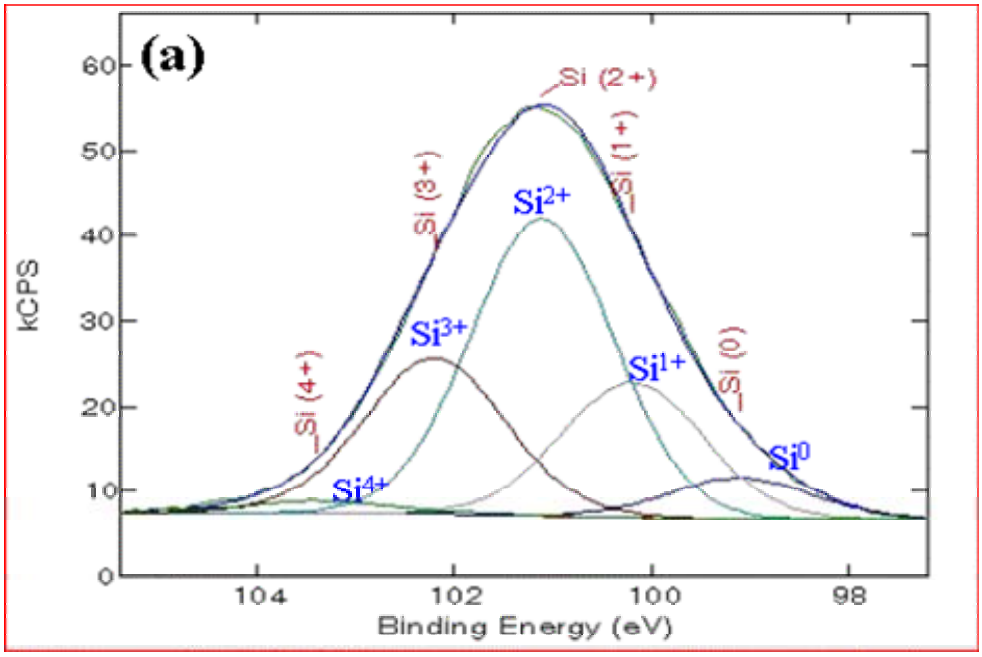
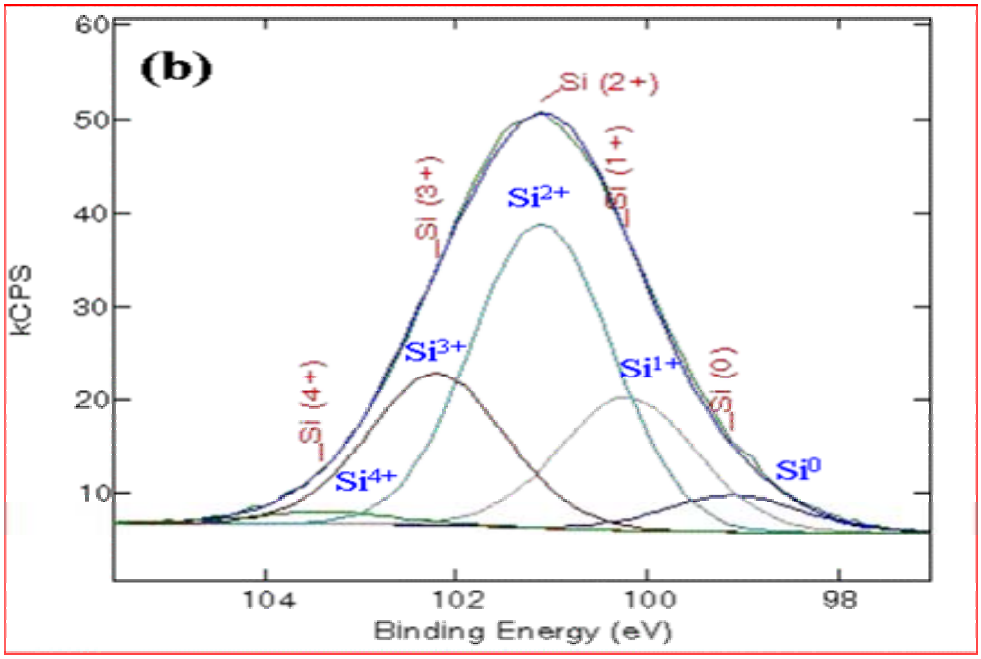


Figure 5-1-4. The effects of carrier gas on the dielectric constant and refractive index of the low-*k* films.


(a)
kCPS
Binding Energy (eV)
Si (2+)
Si (3+)
Si (1+)
Si (4+)
Si (0)
Si2+
Si3+
Si1+
Si4+
Si0


(b)
kCPS
Binding Energy (eV)
Si (2+)
Si (3+)
Si (1+)
Si (4+)
Si (0)
Si2+
Si3+
Si1+
Si4+
Si0

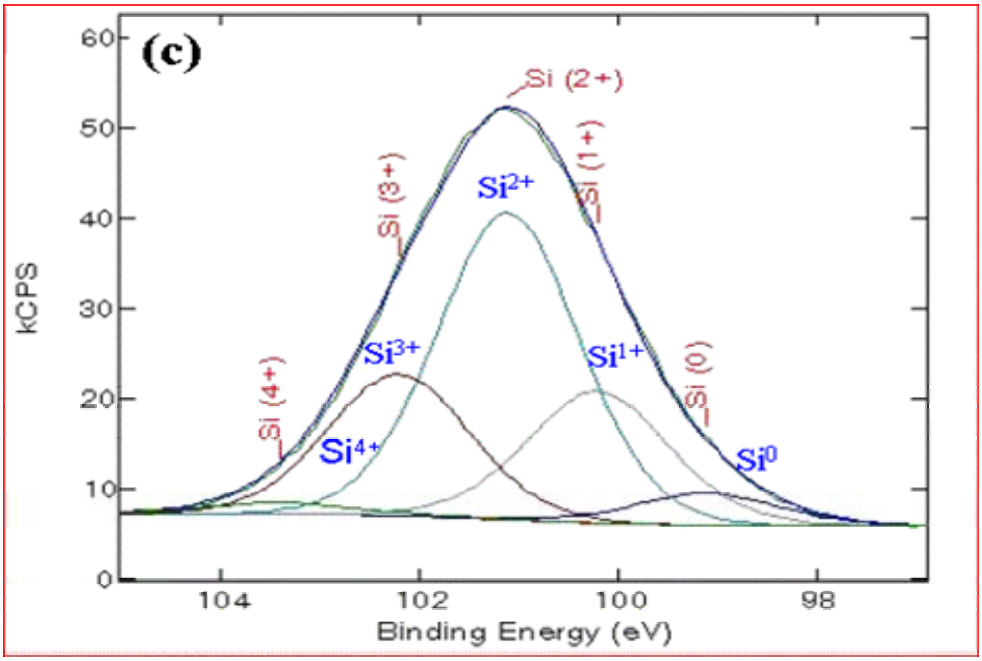


Figure 5-1-5. Binding Energy of Si^{2p} spectrum for the low-*k* films using (a) STD (without carrier gas); (b) He carrier gas; (c) Ar carrier gas.

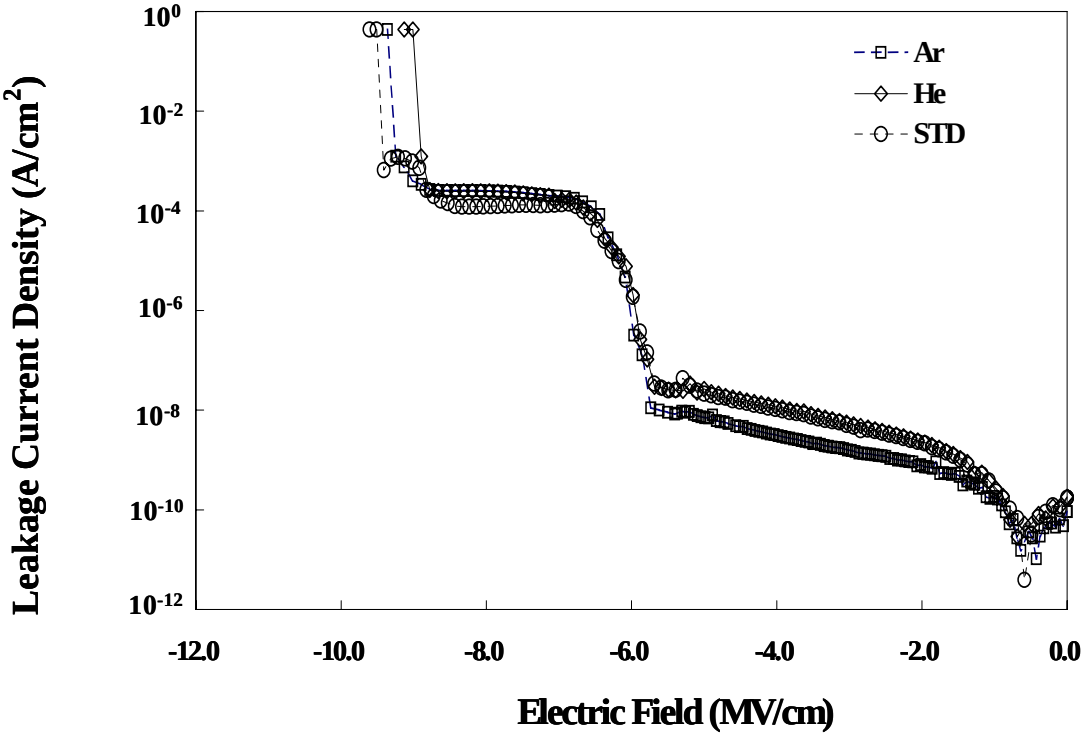


Figure 5-1-6. The leakage current density of the low-*k* films deposited using different carrier gases.

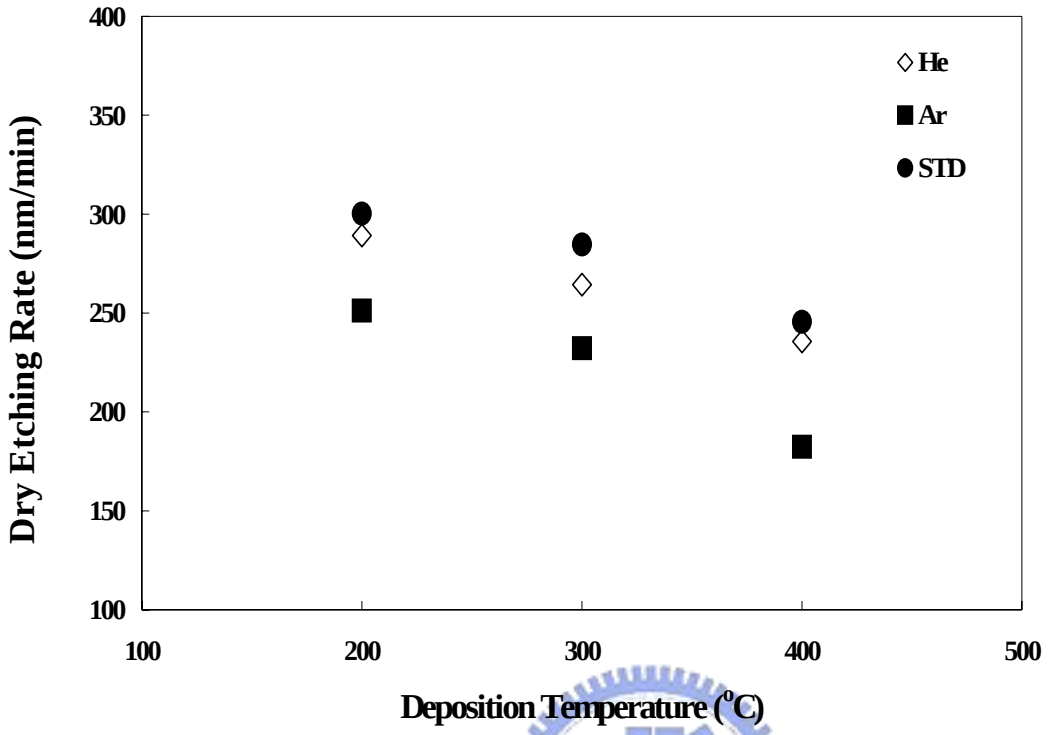


Figure 5-1-7. The dry etching rate of the low-*k* films as a function of deposition temperature with different carrier gases.

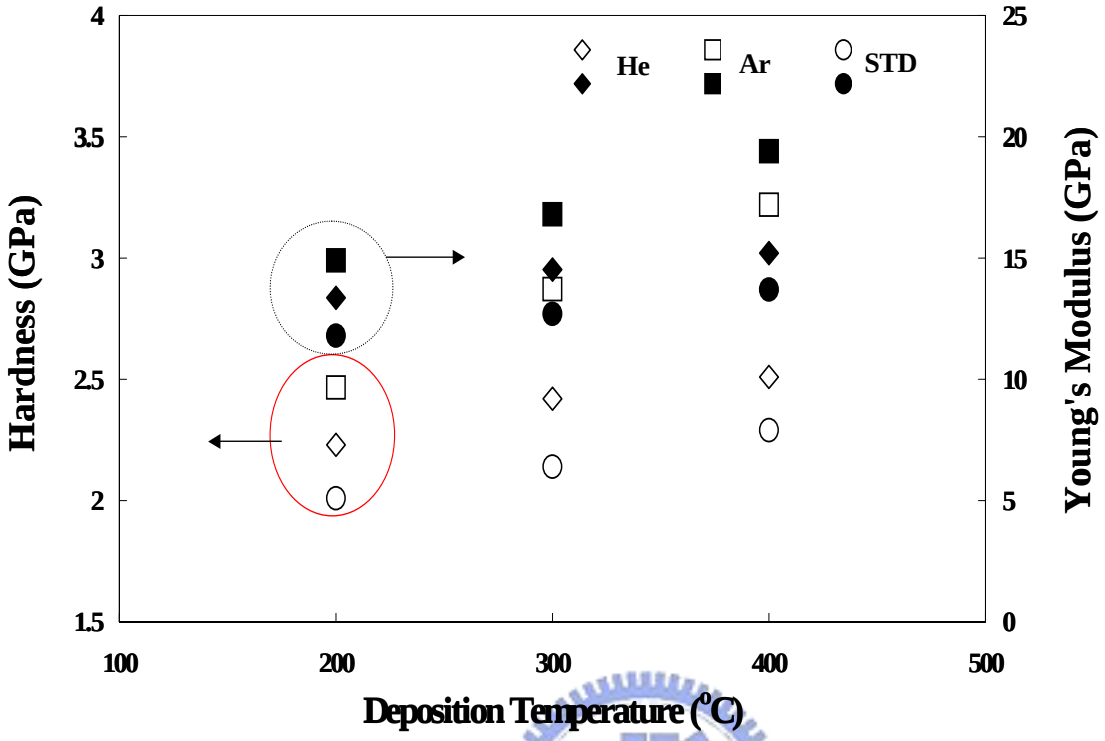


Figure 5-1-8. The Hardness and Young's modulus of the low-*k* films with different carrier gases.

Table 5-2-1. Process conditions of the 3MS- and DEMS-based low-*k* films.

Process Conditions	3MS	DEMS
Pressure (torr)	4	6
Power(W)	600	600
Temperature(^{o}C)	400	400
Spacing(miles)	320	320
3MS(DEMS)/O2	5.2	1.8
He(sccm)	N/A	150

Table 5-2-2. RBS and XPS results of the 3MS- and DEMS-based low-k films.

RBS	%Si	% H	% C	% O
3MS	20~22	36~42	17~21	18~22
DEM	19~21	33~38	9~13	32~36
XPS				
3MS	33~35	N/A	30~34	32~34
DEM	32~34	N/A	20~24	44~46

Table 5-2-3. Characteristics of the 3MS- and DEMS-based low-*k* films.

Film Properties	**3MS**	**DEMS**
Deposition Rate(nm/min.)	415.2	514.2
Refractive Index(633nm)	1.4673	1.414
Density(g/cc)	1.35	1.49
Stress(dyne/cm^2)	2.79E+08	7.33E+08
Etch Rate (nm/min)	2764	2676
Dilectric constant	2.92	2.78
K_e	1.15296929	0.999396
K_{ion} +K_{ori}	1.76703071	1.780604
Hardness (Gpa)	1.78	2.24
Leakage Current (2MV/cm)	2.24E-07	2.45E-09
Breakdown Voltage (V)	5.12	5.35

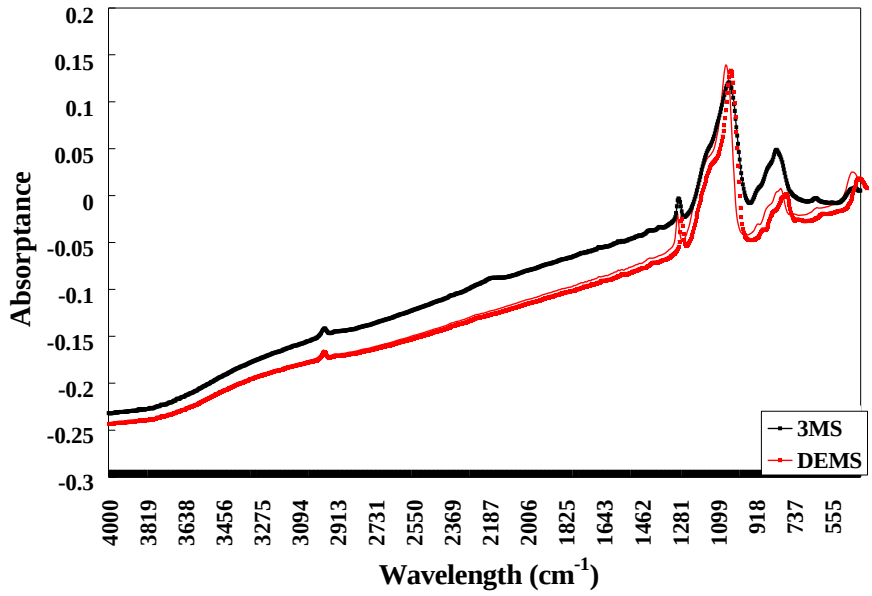
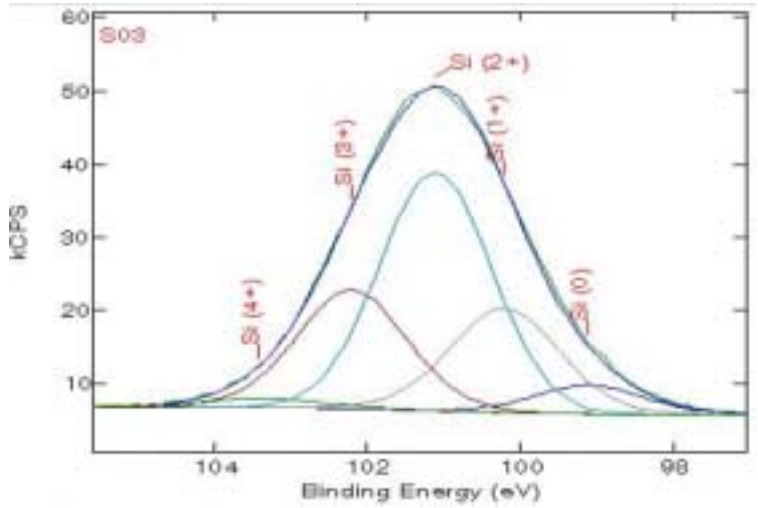
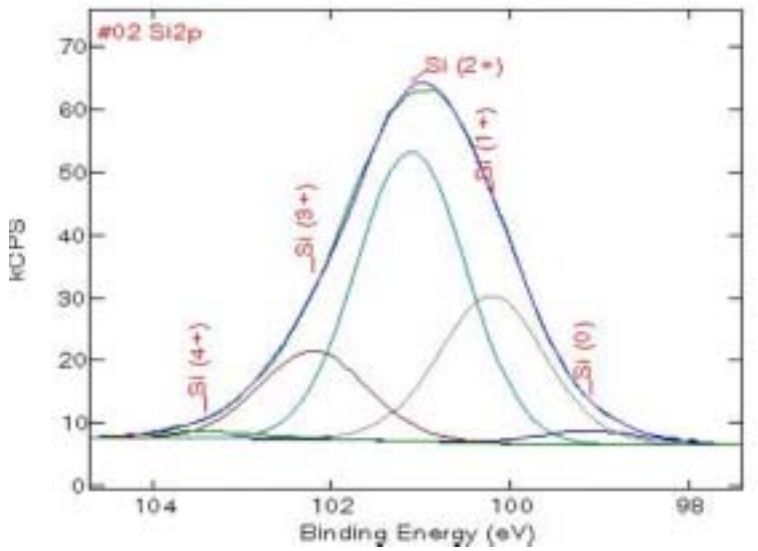


Figure 5-2-1. FTIR spectra of the 3MS- and DEMS-based low-*k* films.

(a)



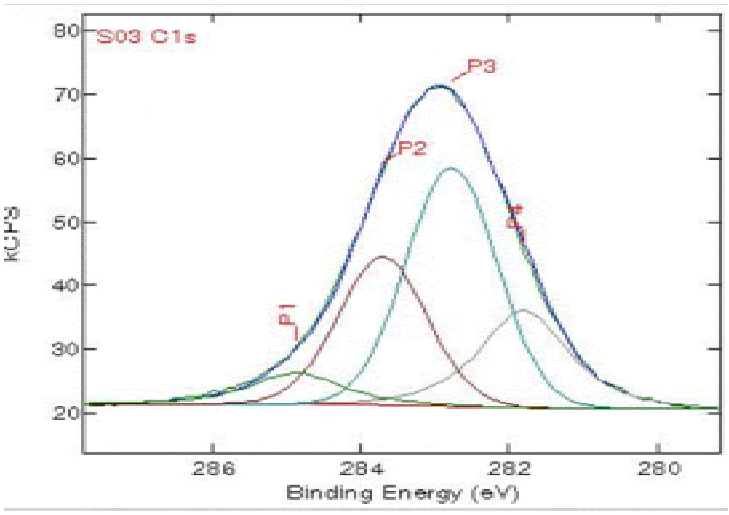
(b)



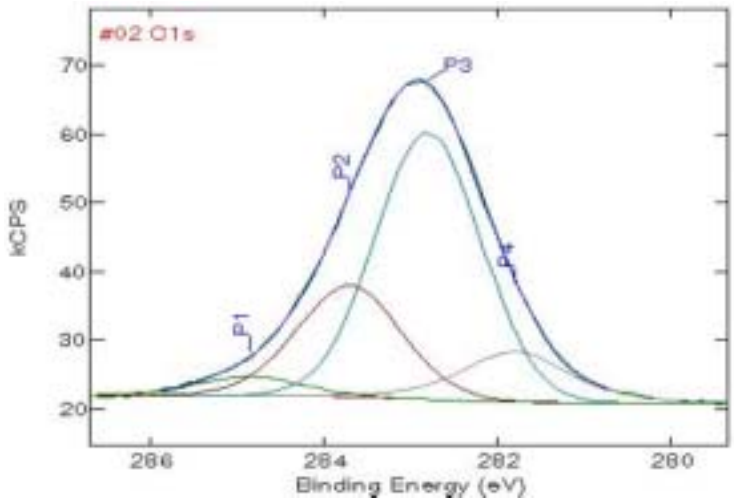
Si 2p	Si^{4+}	Si^{3+}	Si^{2+}	Si^{1+}	Si^{0}
eV	103.4	102.2	101.1	100.2	99.1
3MS	2%	24%	48%	21%	6%
DEMS	1.2%	16.1%	53.5%	26.9%	2.3%

Figure 5-2-2. XPS Si(2p) spectra of low-k films deposited by (a) 3MS and (b) DEMS.

(a)



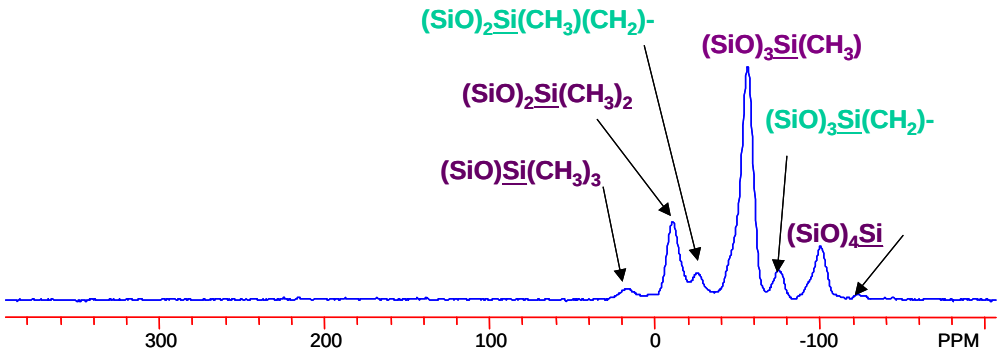
(b)



C 1s	O_2-C-C-(Si, H)$_2$	O-C-C-(Si, H)$_3$	Si-CH_3	$CSi_{4-x}H_x$
eV	285.2	284.1	283.4	282.4
3MS	7%	28%	46%	20%
DEMS	4.1%	24.7%	59.6%	11.7%

Figure 5-2-3. XPS C(1s) spectra of low-k films deposited by (a) 3MS and (b) DEMS.

(a)



(b)

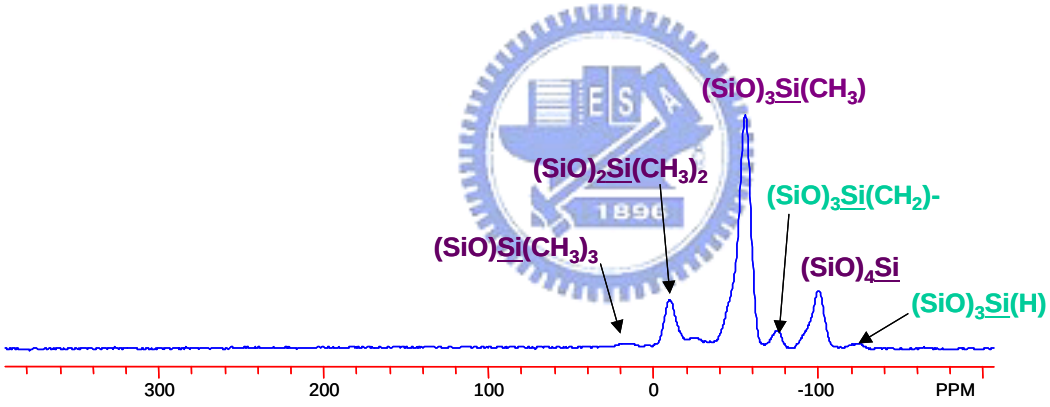


Figure 5-2-4. ^{29}Si NMR spectra of low-k films deposited by (a) 3MS and (b) DEMS.

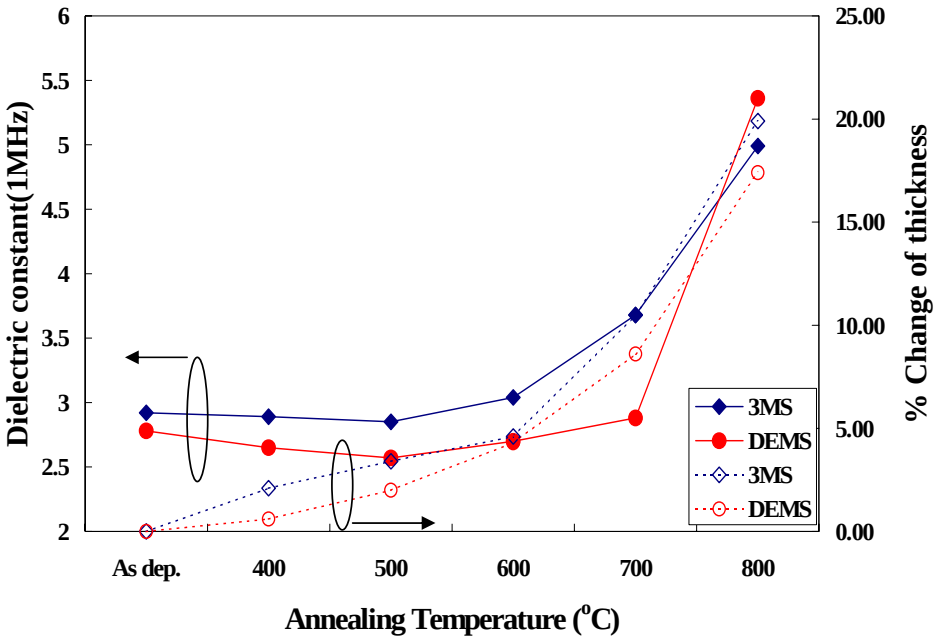


Figure 5-2-5. Effect of heating test temperature on the change of dielectric constant and thickness of the 3MS- and DEMS-based low-k films.

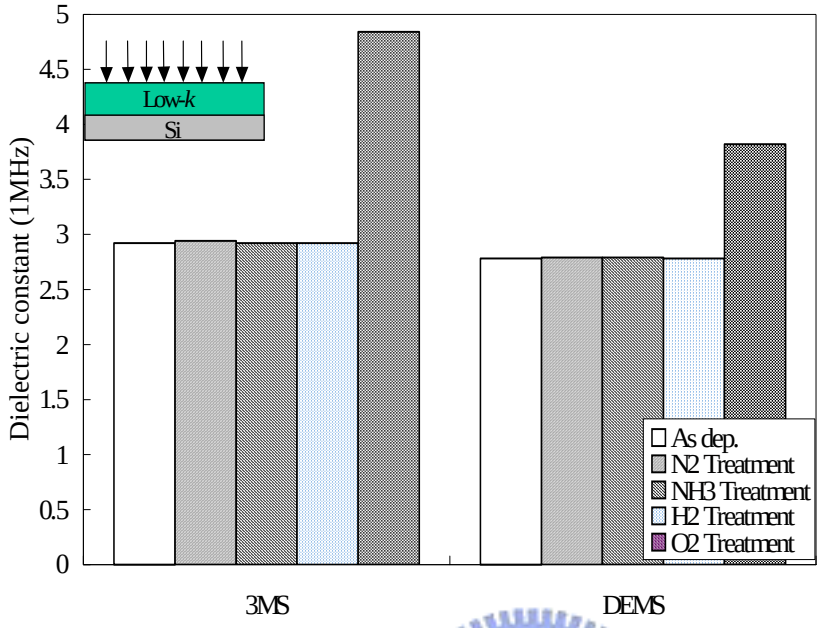


Figure 5-2-6. Effect of varying plasma treatments on the change of dielectric constant of the 3MS- and DEMS-based low-k films.

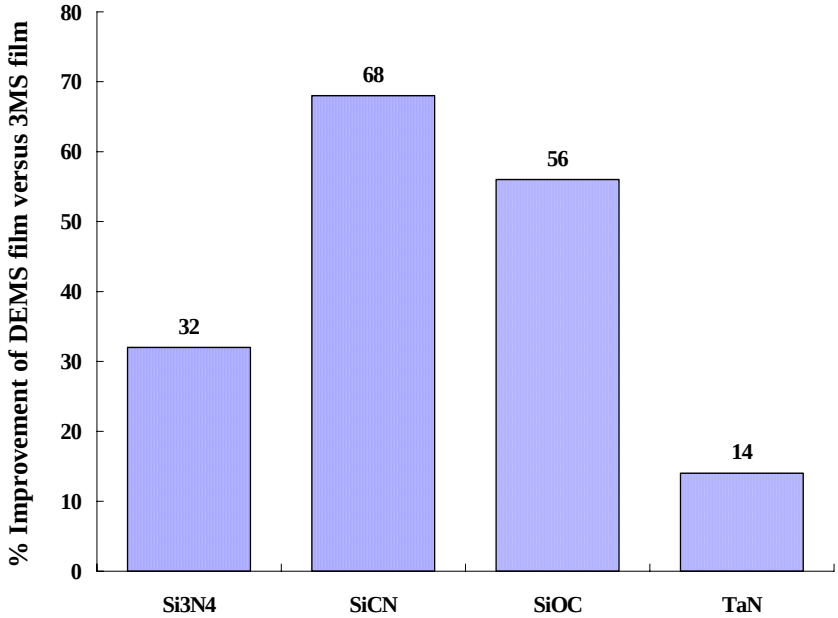


Figure 5-2-7. Relative adhesive strength between the 3MS- and DEMS-based low-k films.

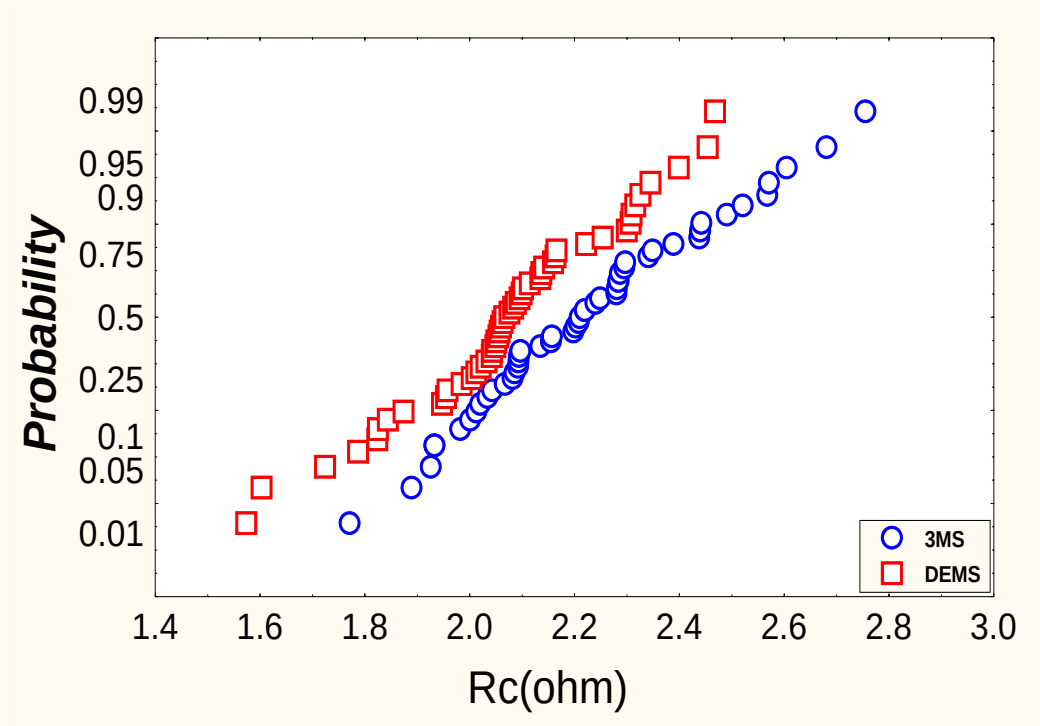


Figure 5-2-8. 0.18-μm via resistance of the 3MS- and DEMS-based low-*k* films.

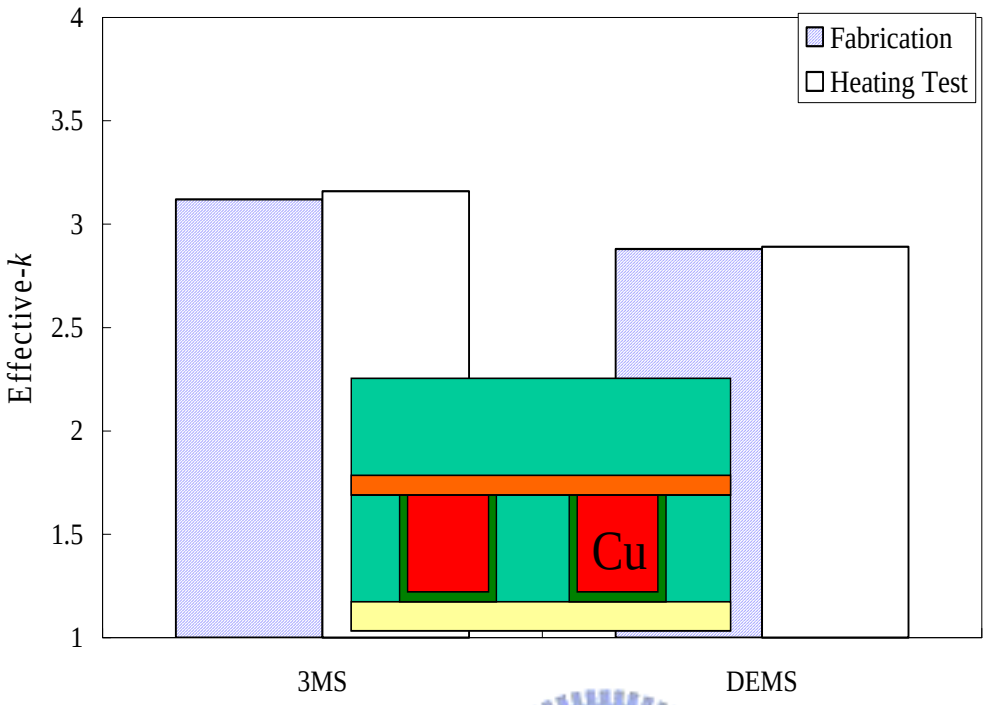


Figure 5-2-9. Effect of heating test temperature on the change of Effective k values of the 3MS- and DEMS-based low-*k* films.

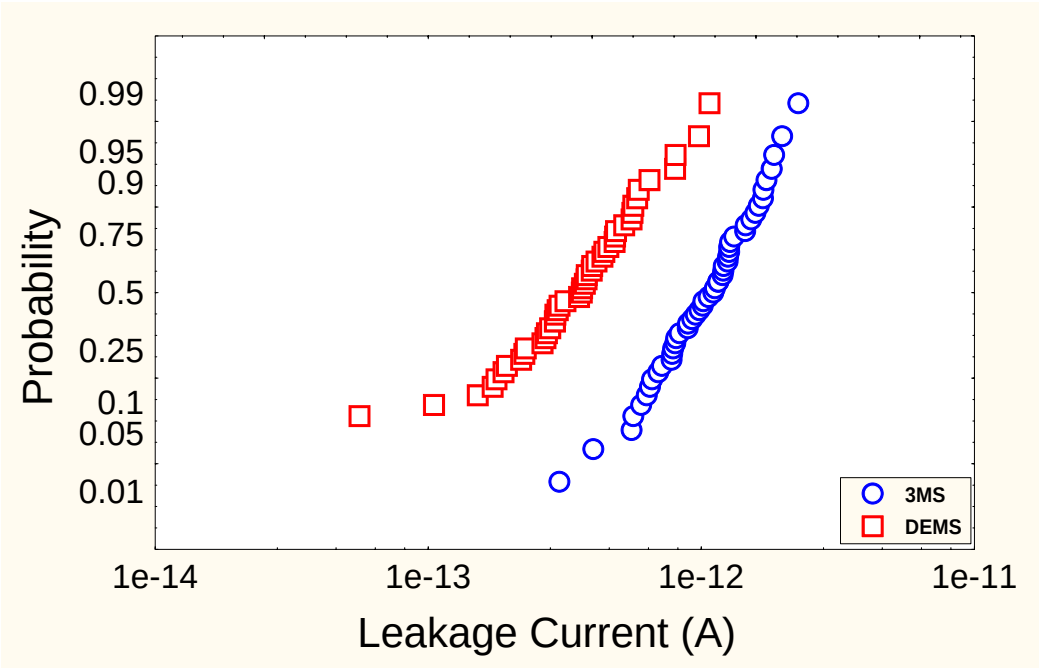


Figure 5-2-10. Metal line-to-line leakage current of the 3MS- and DEMS-based low-*k* films.

Table 5-3-1. RBS result for the low-*k* films prepared DEMS as a function of the deposition temperature.

RBS	% Si	% H	% C	% O
250^{o}C	19~21	49~53	16~18	16~18
350^{o}C	20~22	40~43	12~15	25~28
425^{o}C	19~21	33~36	9~13	32~36

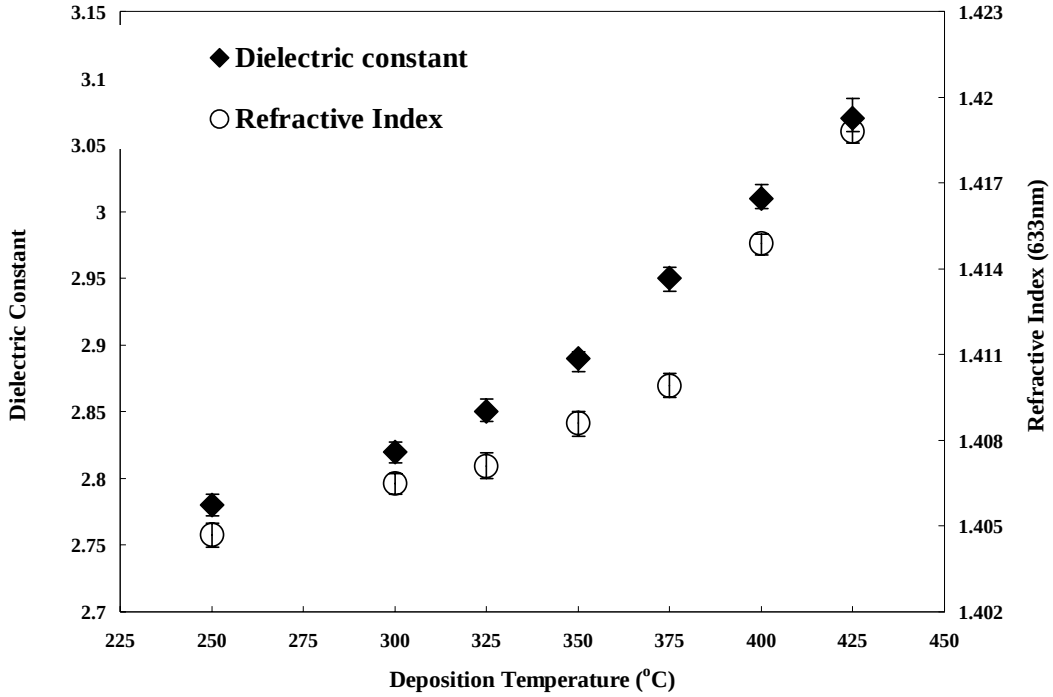


Figure 5-3-1. Refractive index and dielectric constant of DEMS-based low-*k* films as a function of the deposition temperature.

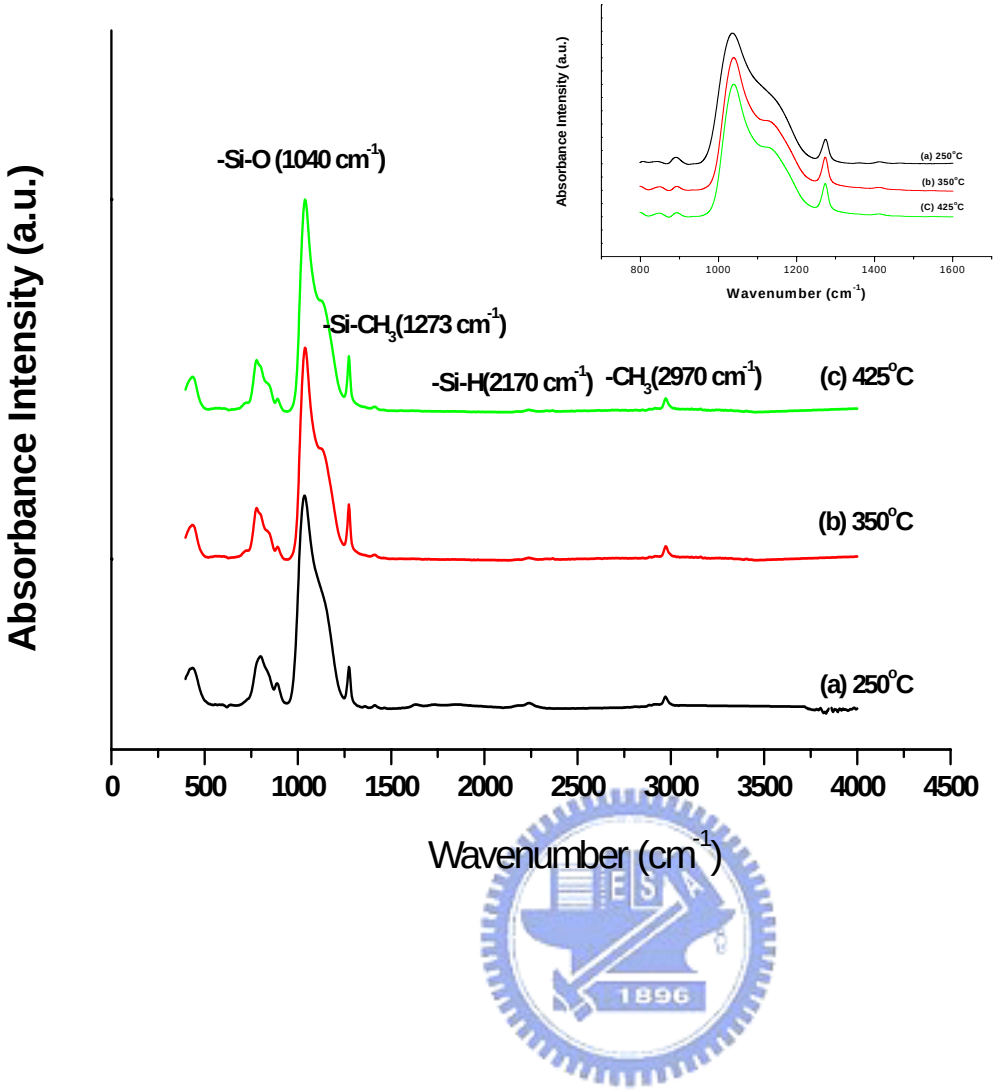


Figure 5-3-2. FTIR spectra of DEMS-based low-*k* films at different deposition temperatures.

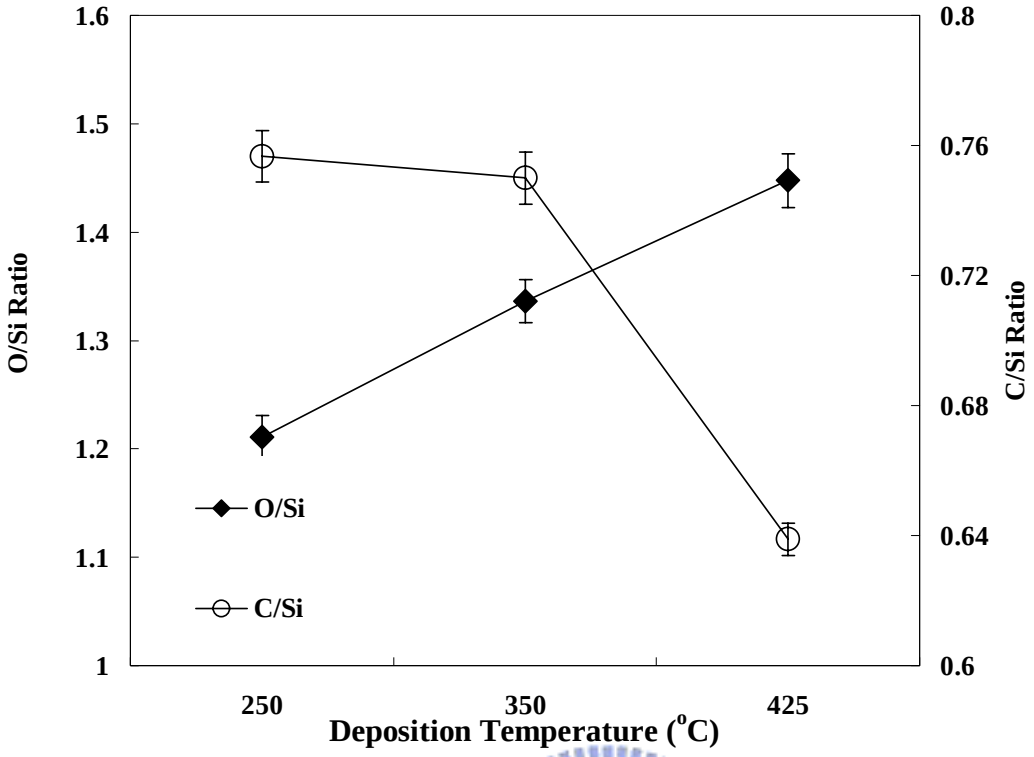
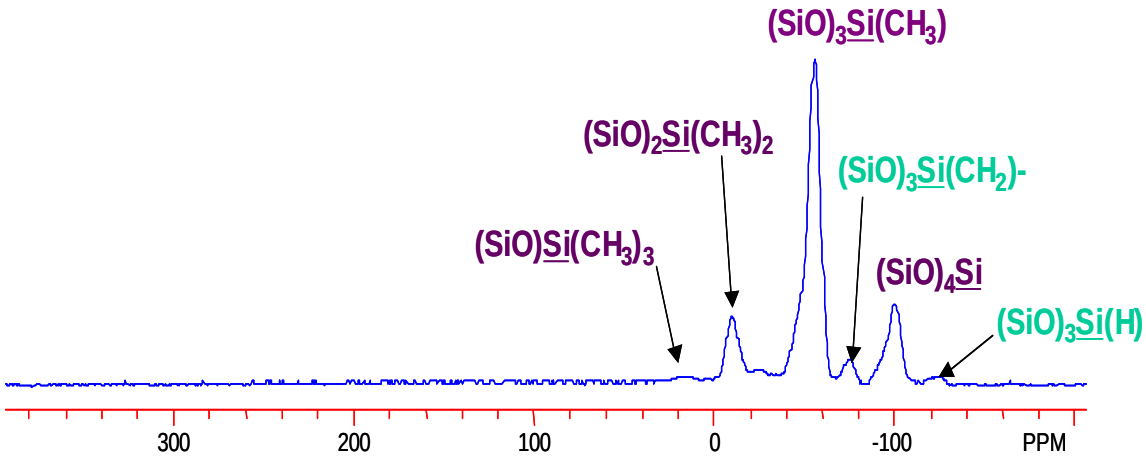


Figure 5-3-3. XPS results of the O/Si and C/Si ratio as a function of the deposition temperature.

(a)



(b)

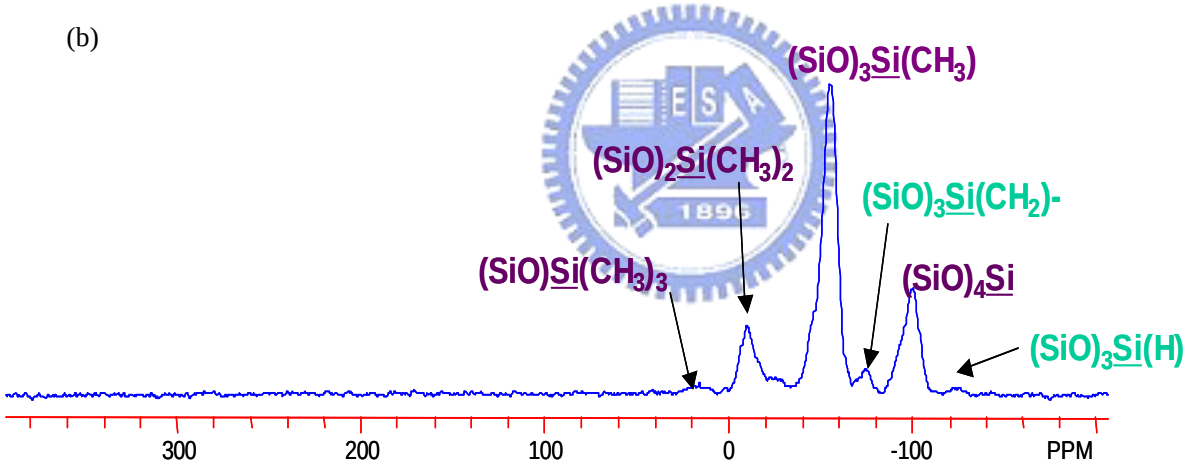


Figure 5-3-4. [29] Si NMR spectra for DEMS-based low-*k* films (a) 425°C Deposition temperature; (b) 300°C Deposition temperature.

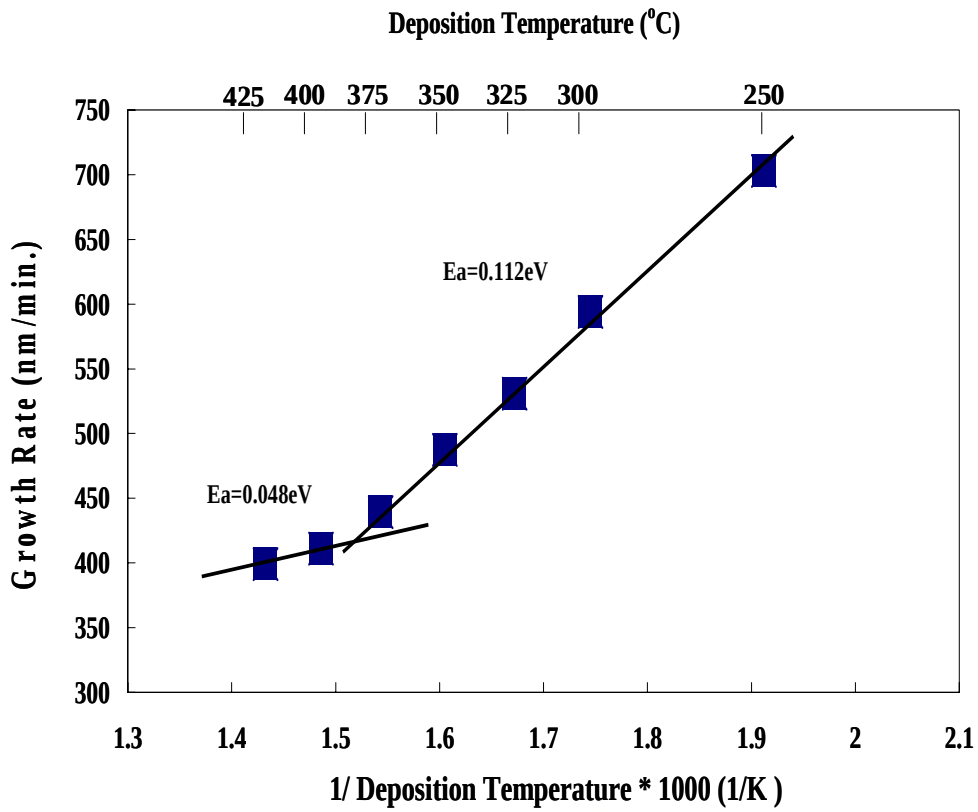


Figure 5-3-5. Deposition rate of DEMS-based low-*k* films as a function of the deposition temperature.

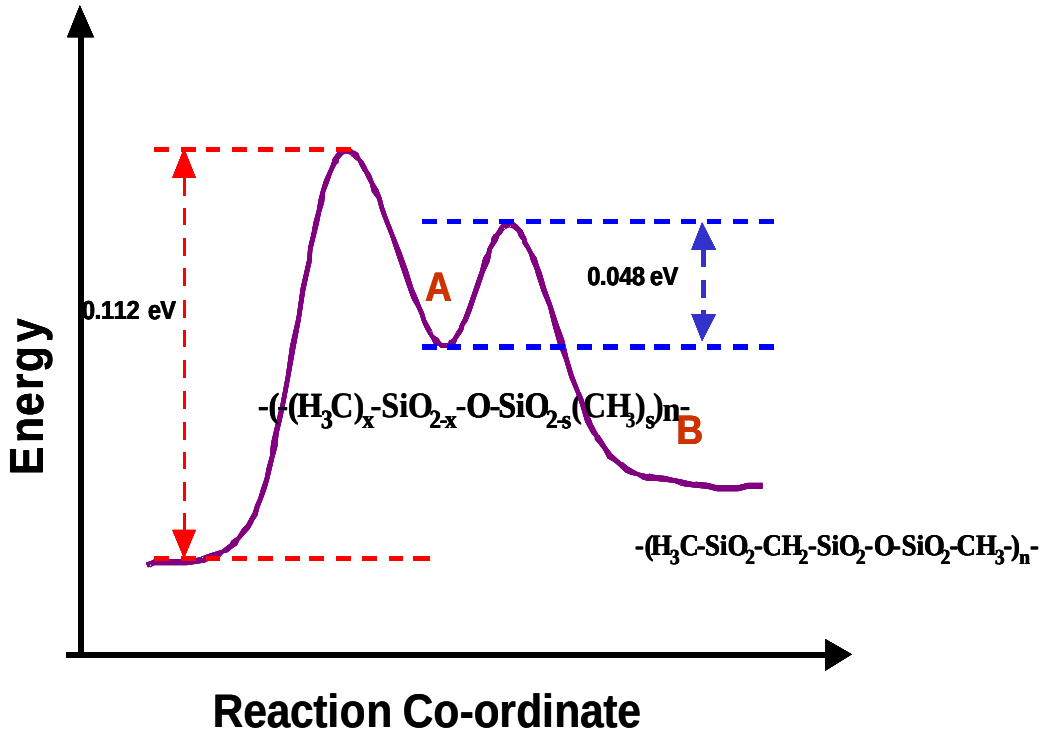


Figure 5-3-6. Activated energy of DEMS-based low-*k* films.

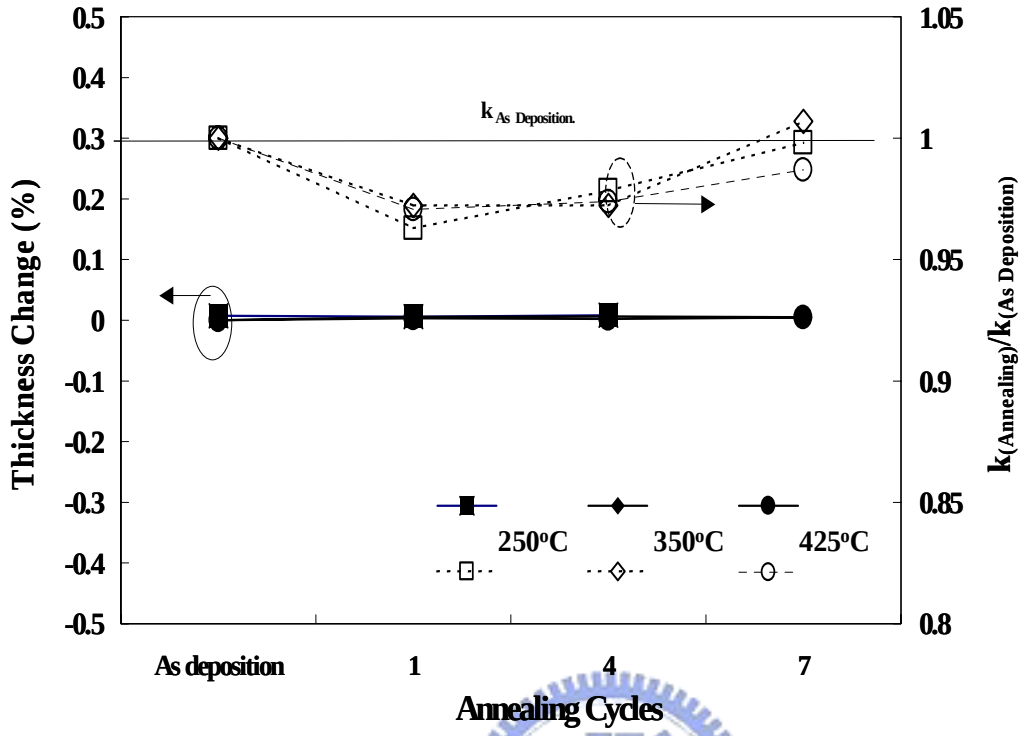


Figure 5-3-7. Effect of annealing cycles on the change of dielectric constant and thickness of DEMS-based low-*k* films with varying deposition temperatures.

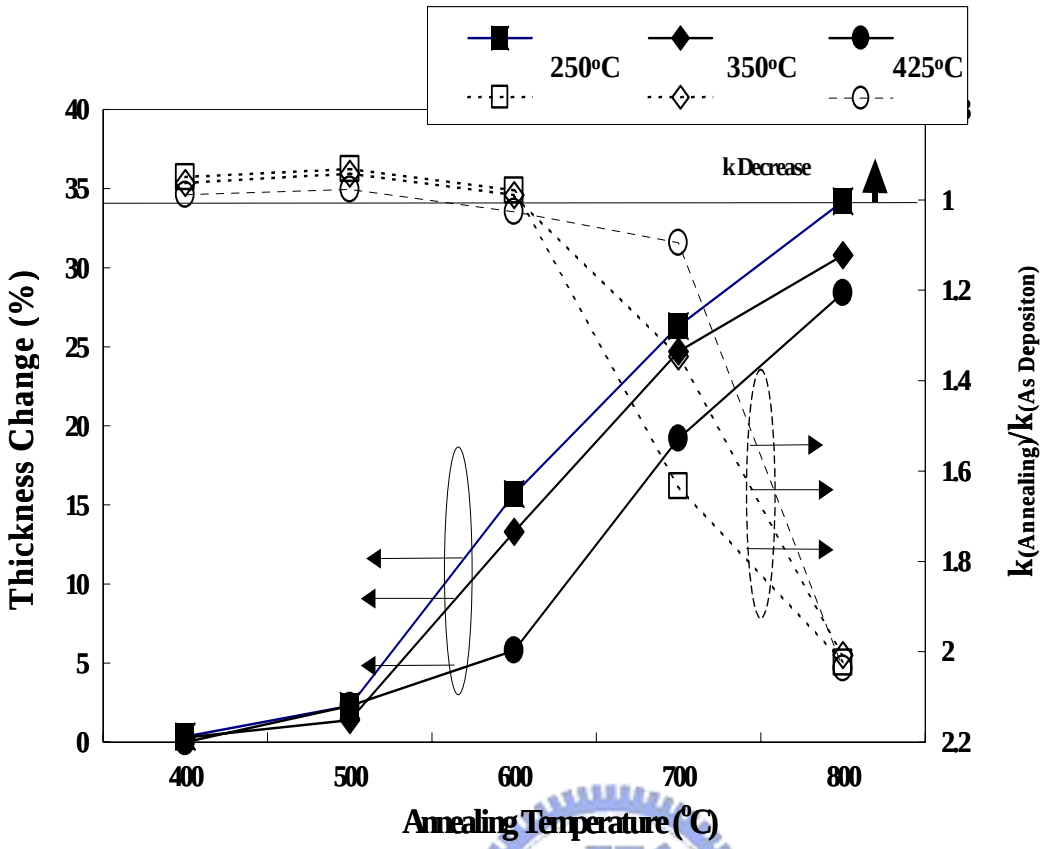


Figure 5-3-8. Effect of annealing temperatures on the change of dielectric constant and thickness of DEMS-based low-*k* films with varying deposition temperatures.

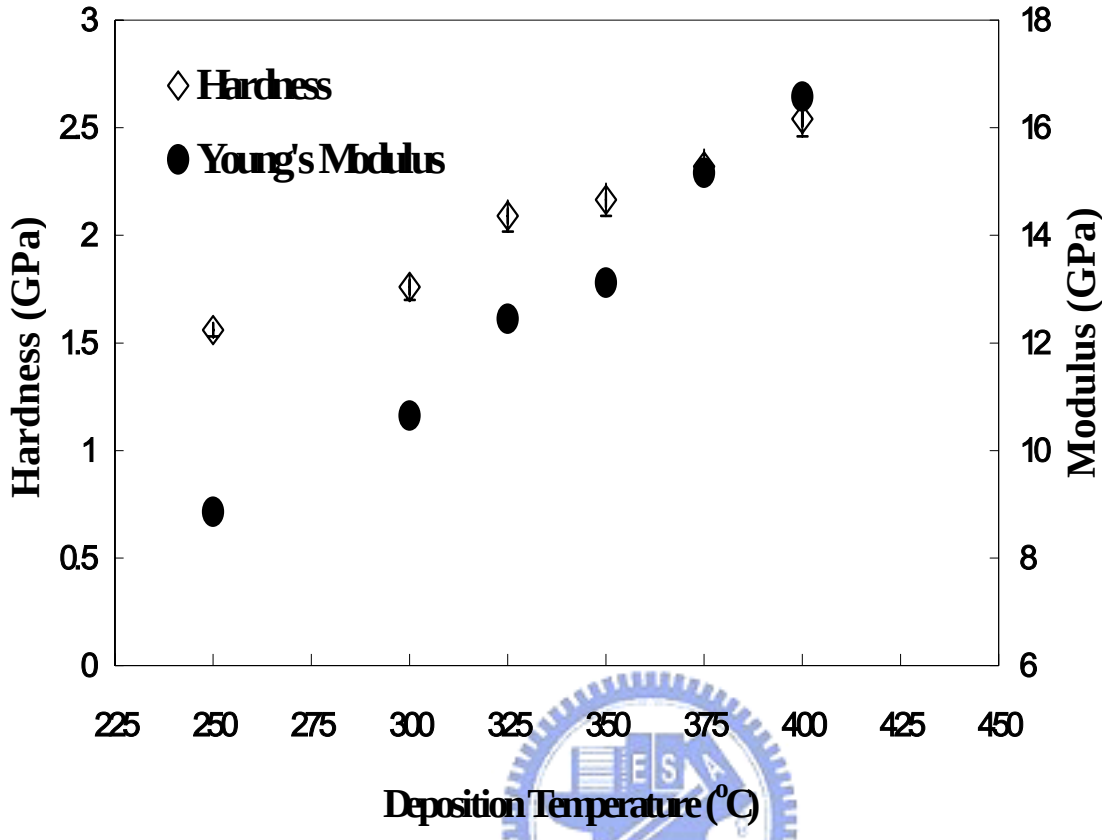


Figure 5-3-9. Hardness and Young's Modulus of DEMS-based low-*k* films as a function of the deposition temperature.

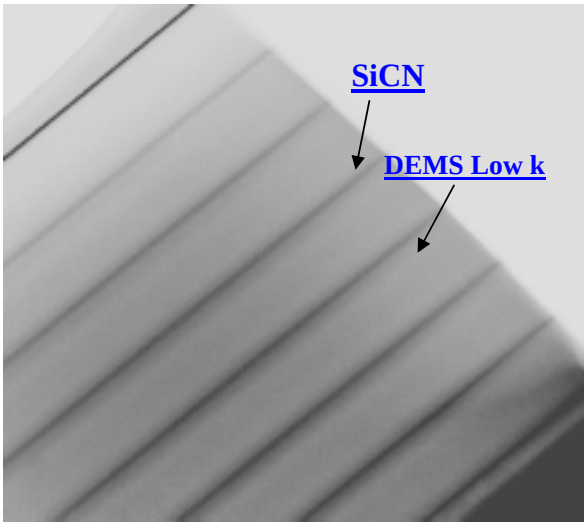


Figure 5-3-10. TEM image for 8-level dielectric Stack of 250^{o}C DEMS-based low-*k* film/SiCN Stack.

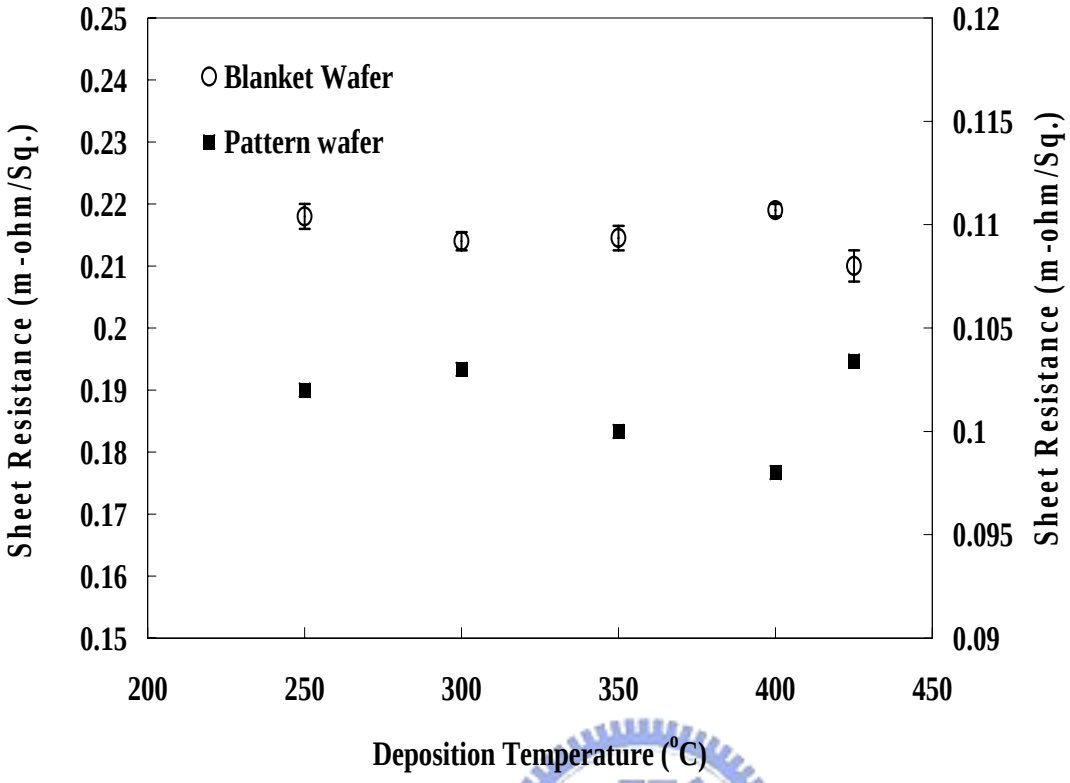


Figure 5-3-11. Cu sheet resistance on the blanket wafer and the pattern wafer as a function of DEMS-based low-*k* film deposition temperature.

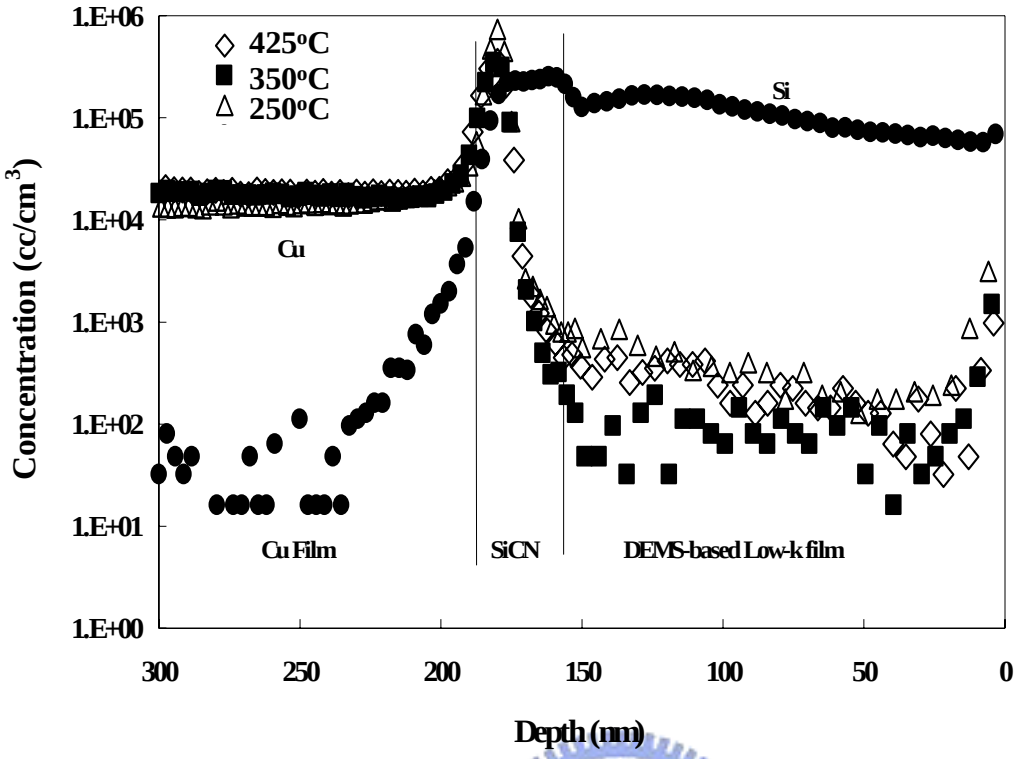


Figure 5-3-12. Secondary Ion Mass Spectroscopy profile of the Cu counts for a film stack of Cu/SiCN/DEMS.

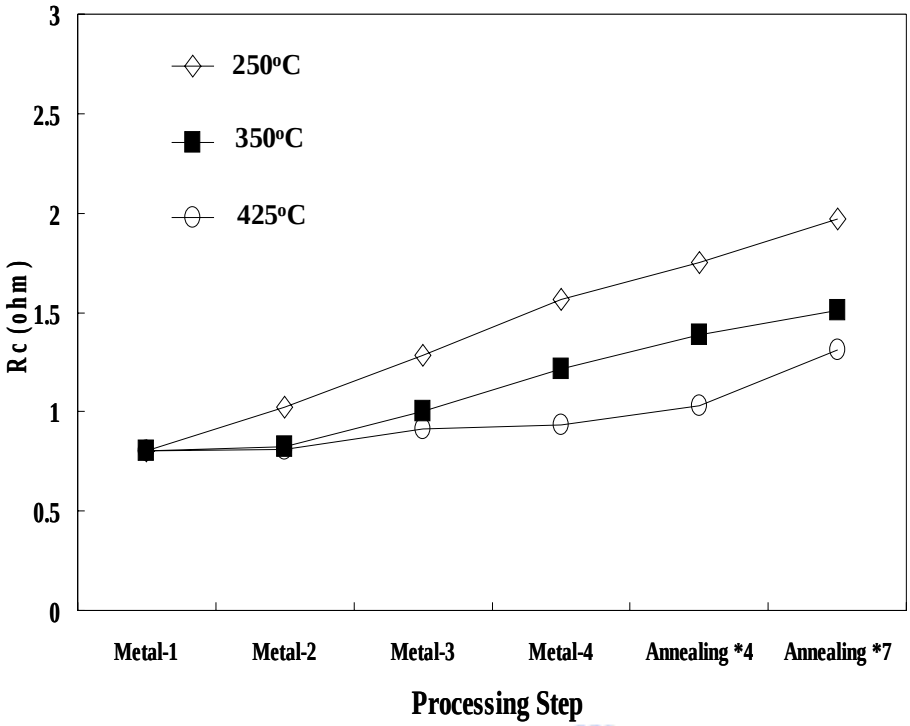


Figure 5-3-13. Effect of thermal process on the via resistance with 0.19 μm diameter for DEMS-based low-*k* films with varying deposition temperatures.

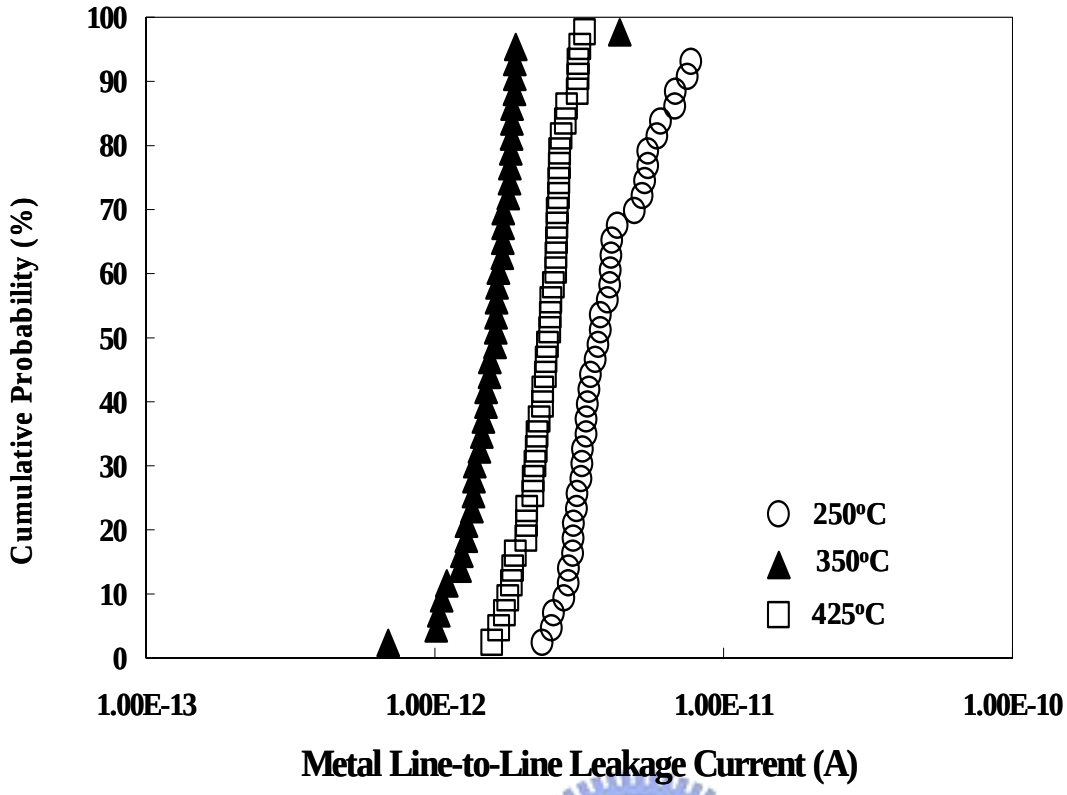


Figure 5-3-14. Metal line-to-line leakage current as a function of the DEMS-based low-*k* film deposition temperature.

Table 5-4-1. XPS result for the SiCOH films as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

O_2/DEMS	Temp	O	C	Si
0	425°C	42.8	24	33.2
0.4	425°C	45.1	21.9	33
1	425°C	46.7	20.6	32.7
0	350°C	41.2	26.4	32.4
0.4	350°C	43.9	23.6	32.6
1	350°C	44.8	22.2	33

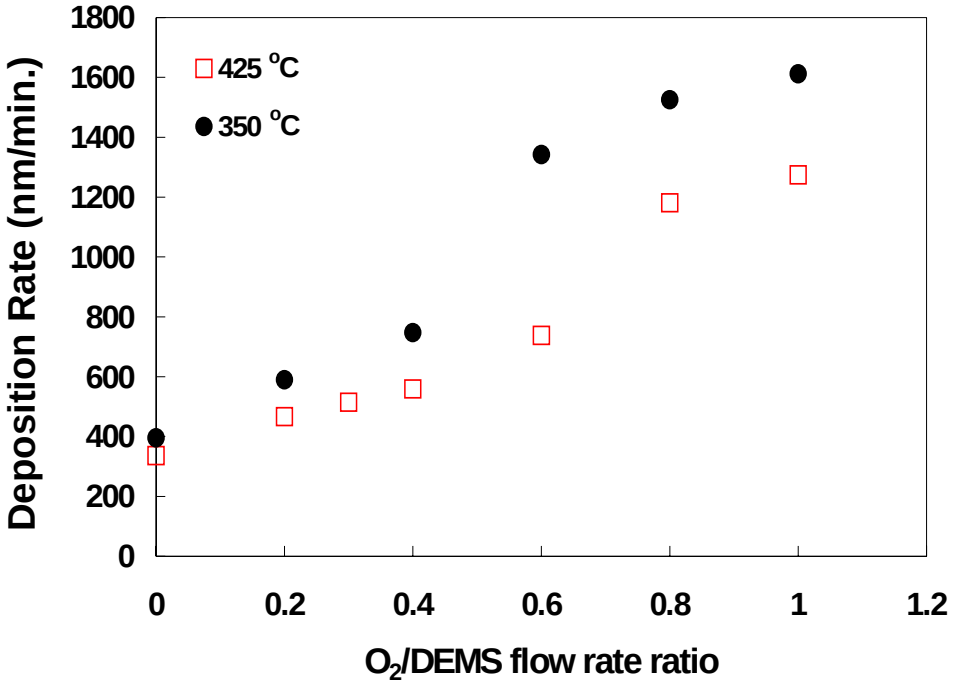


Figure 5-4-1. Deposition rate as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

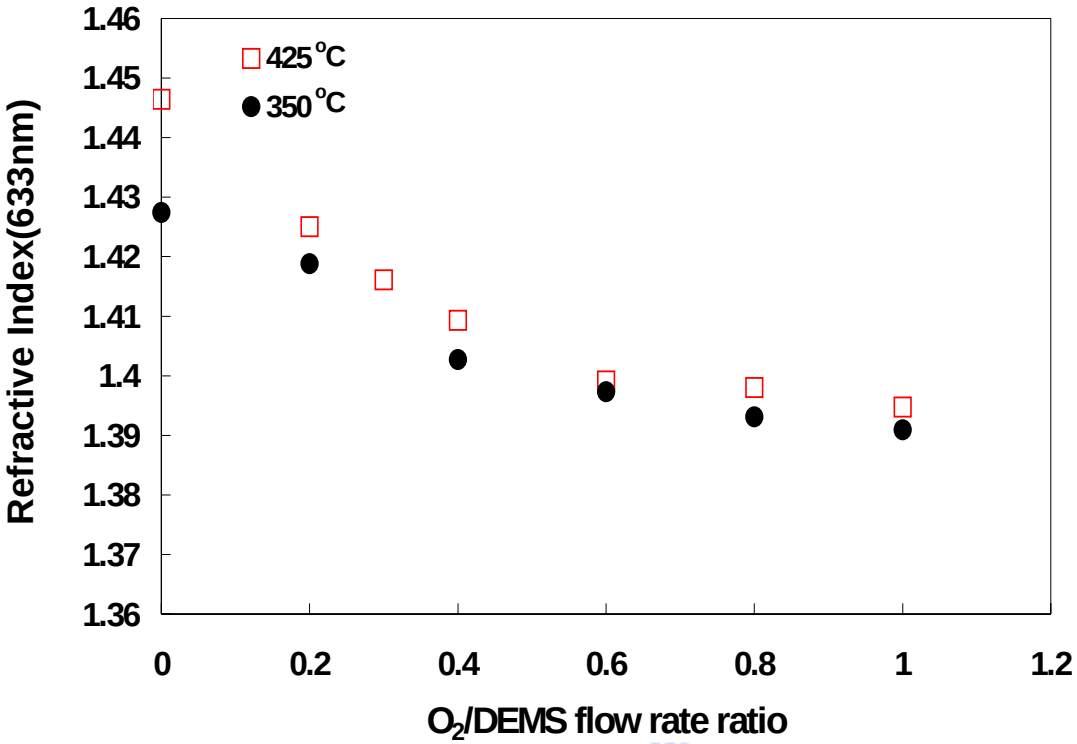


Figure 5-4-2. Refractive index (633nm) as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

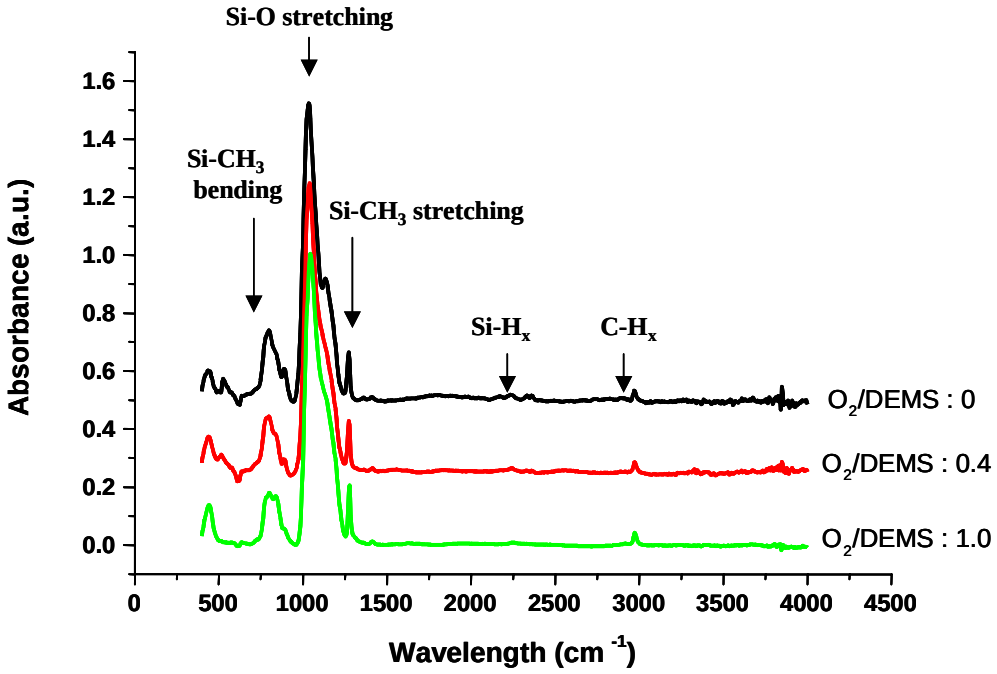


Figure 5-4-3. FTIR spectra of the SiOCH films with varying O_2/DEMS ratio.

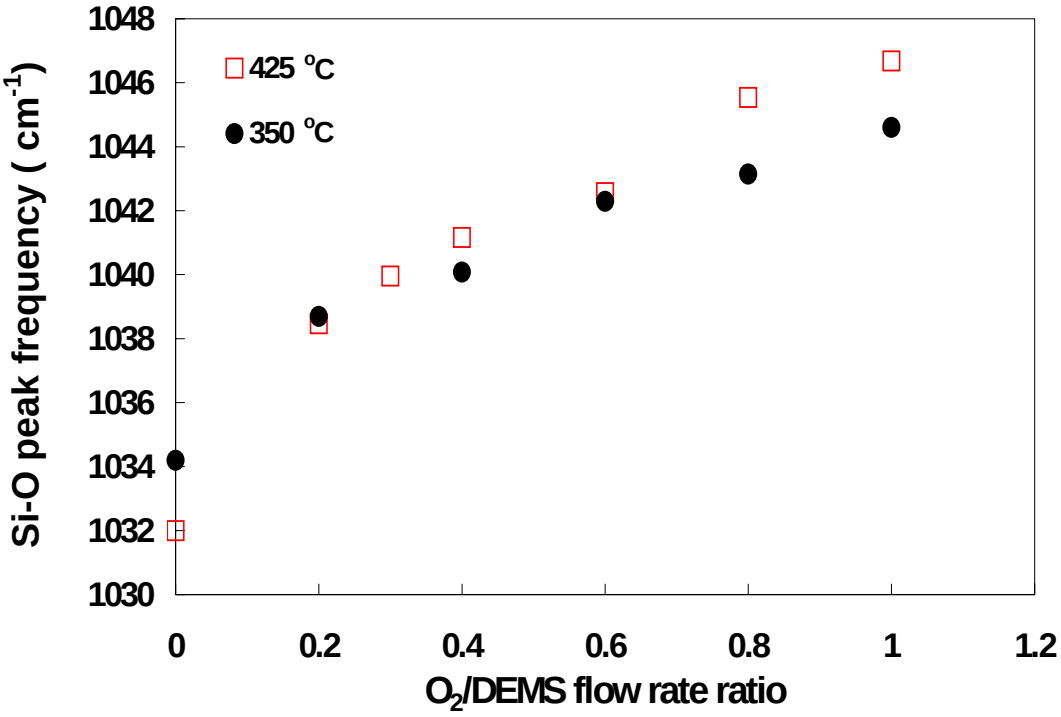


Figure 5-4-4. Si-O peak frequency as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

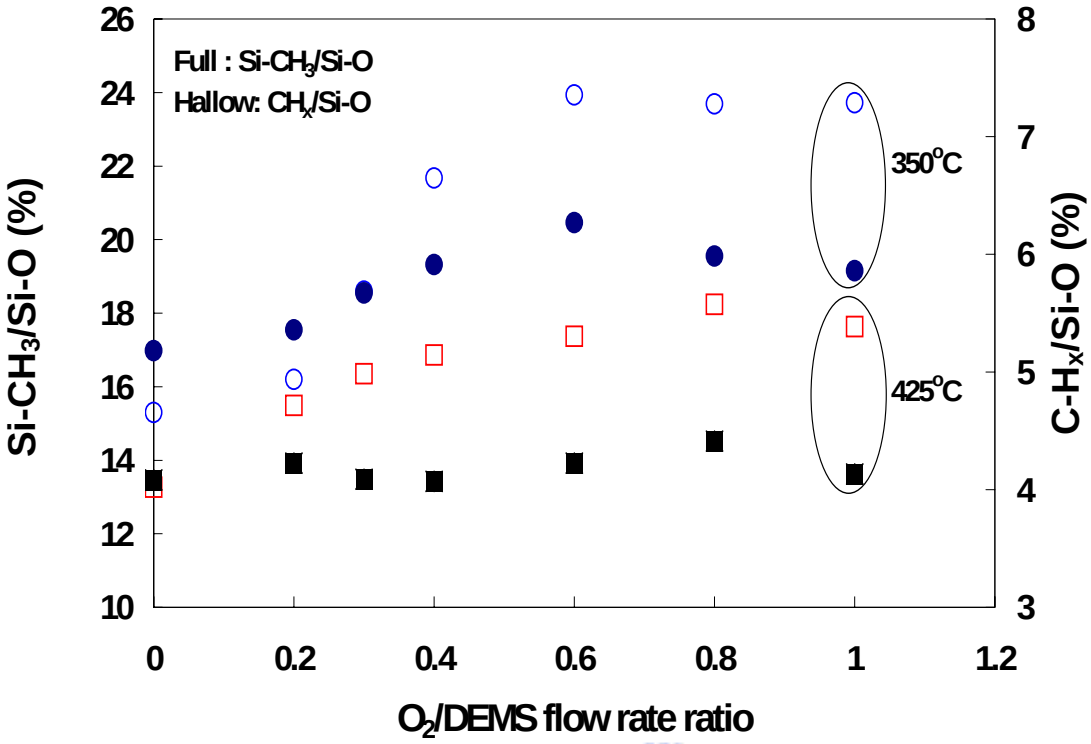


Figure 5-4-5. Si-CH_3/Si-O and C-H_x/Si-O peak ratio in the SiOCH films as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

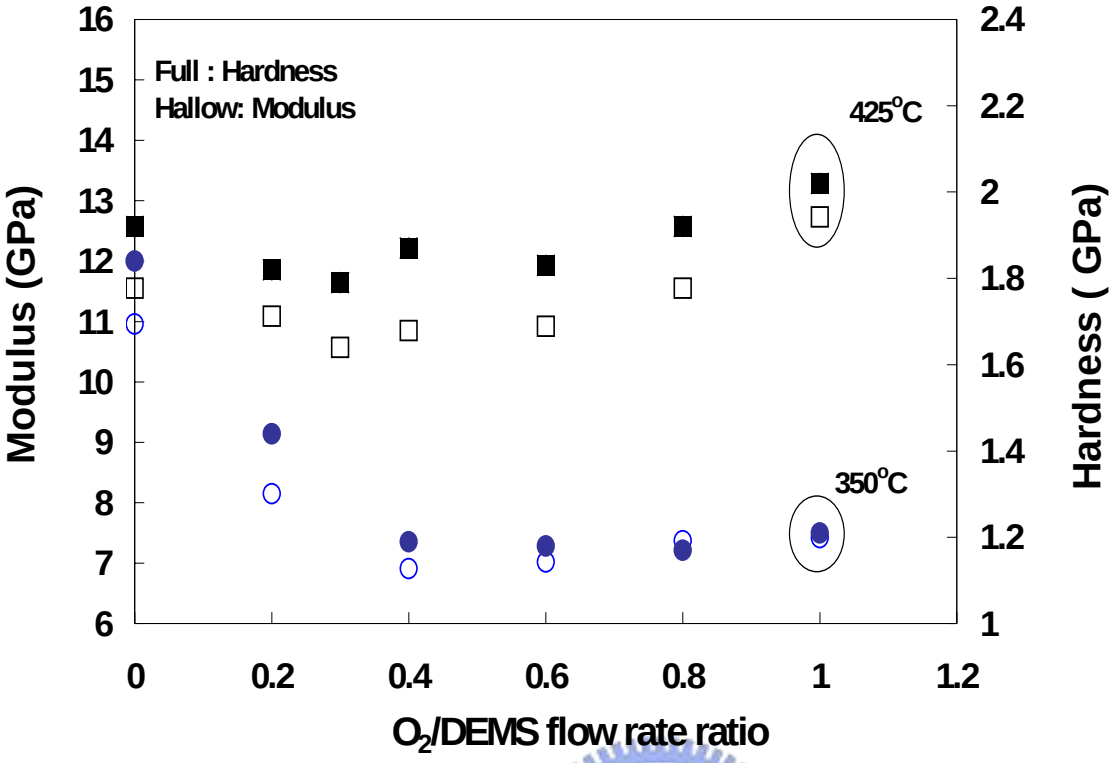


Figure 5-4-6. Hardness and Modulus of the SiOCH films as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

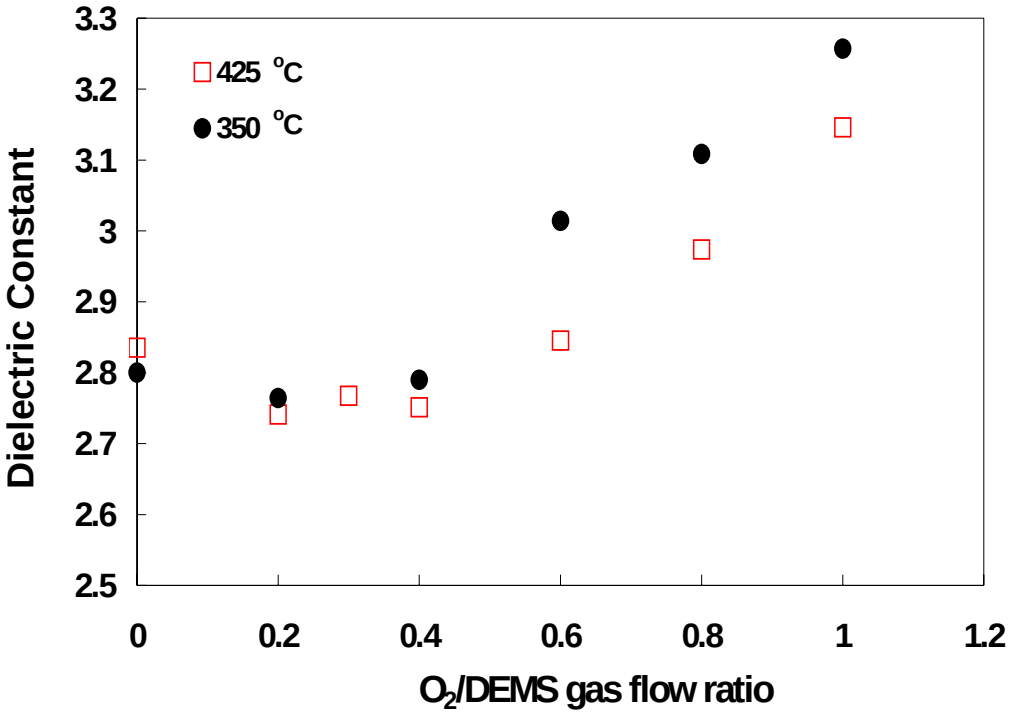


Figure 5-4-7. Dielectric constant of the SiOCH films as a function of O_2/DEMS ratio at 350°C and 425°C deposition temperature.

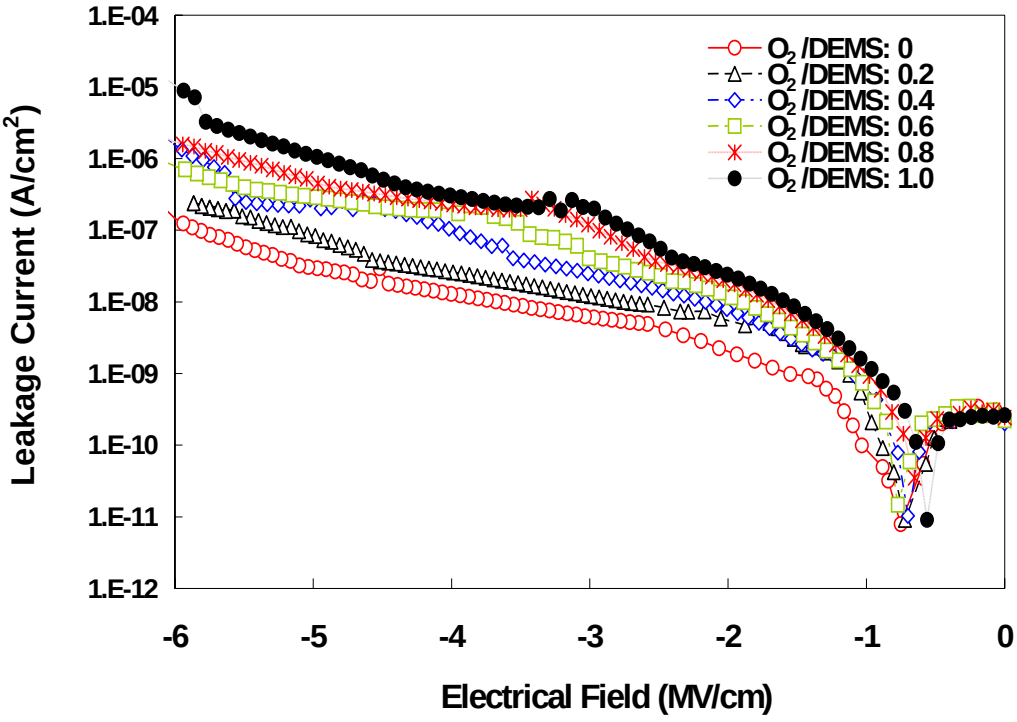


Figure 5-4-8. Leakage current of the SiOCH films as a function of O_2/DEMS ratio at 425^{o}C deposition temperature.

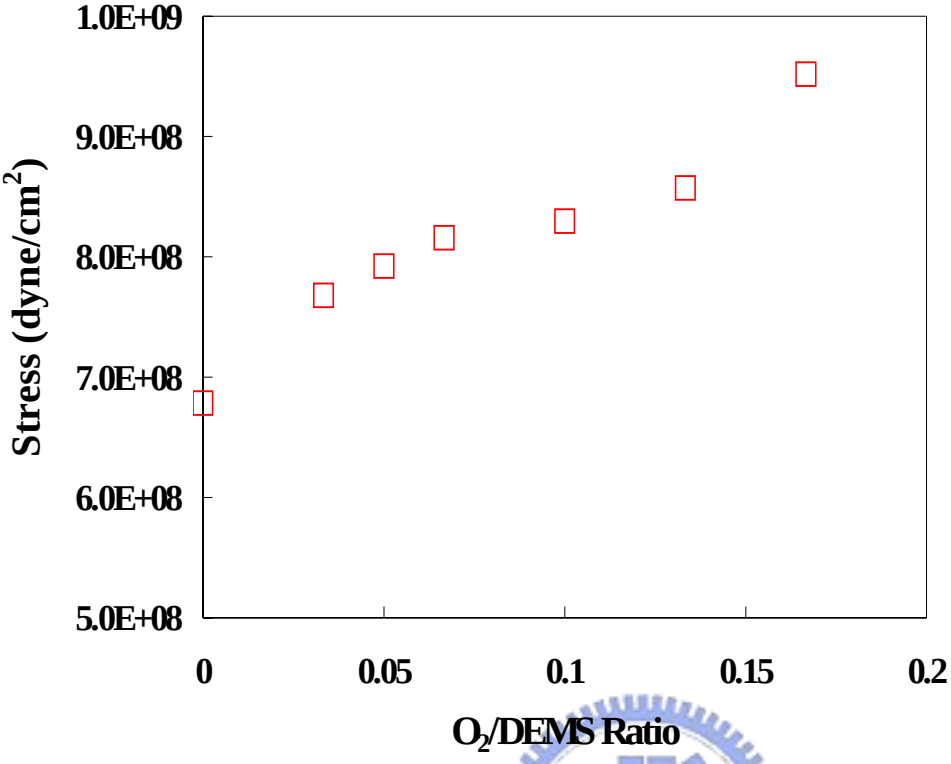
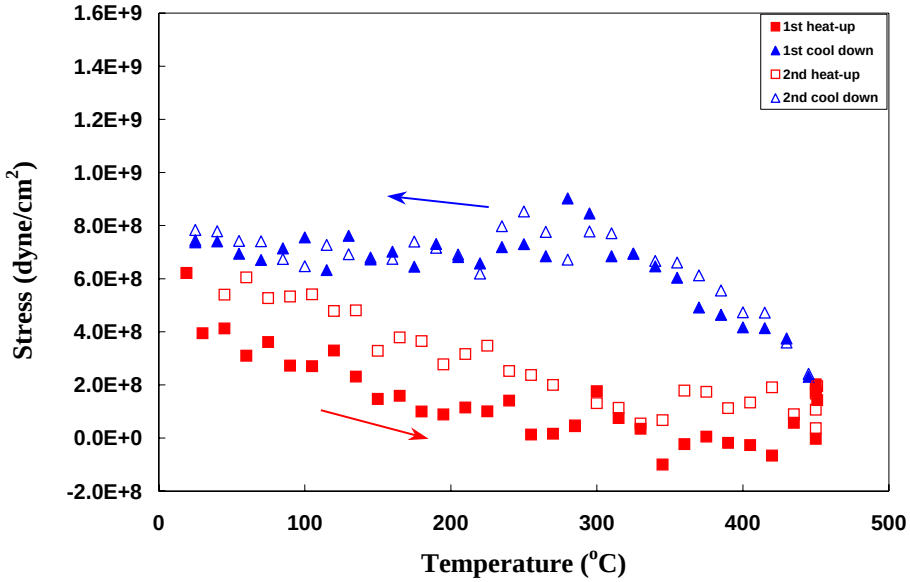
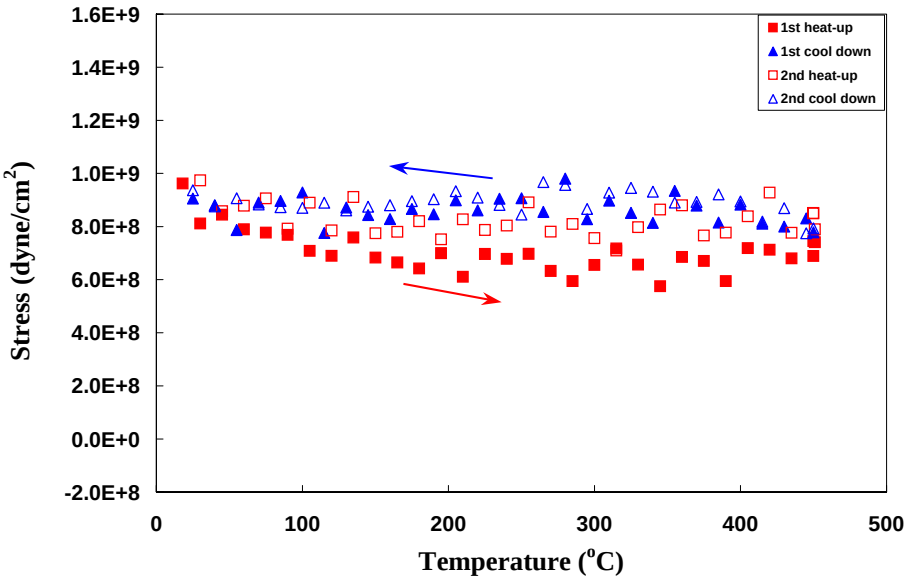


Figure 5-5-1. The effect of the ratio of O_2/DEMS on the stress of the *low-k* film.

(A) DEMS



(B) **O2/DEMS=0.05**



(C) **O2/DEMS=0.175**

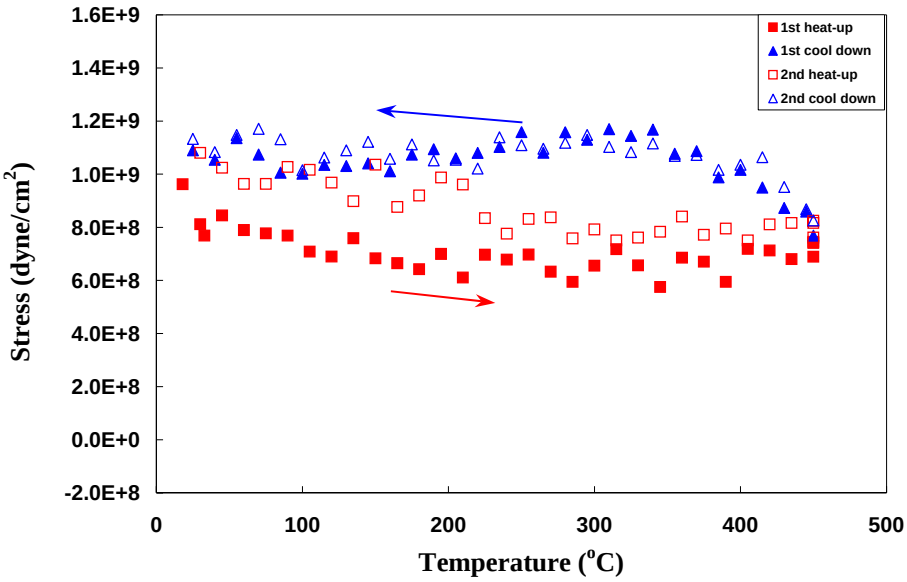


Figure 5-5-2. The stress hysterisis of DEMS *low-k* film with different O_2 flow rates; (a) 0sccm, (B) 150sccm, and (C) 300sccm.

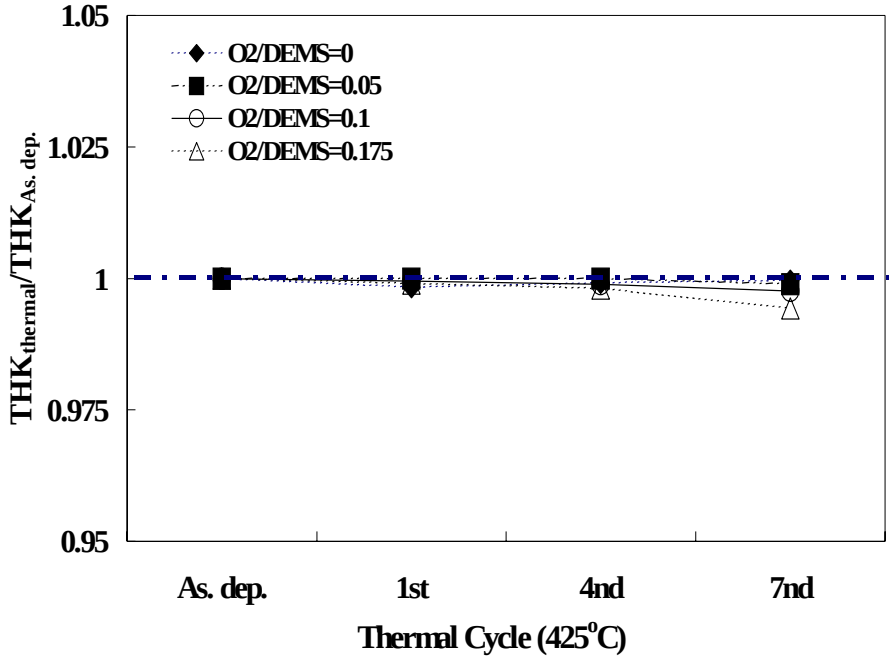


Figure 5-5-3. The thickness change of the *low-k* film after 7 times 425°C thermal cycle.

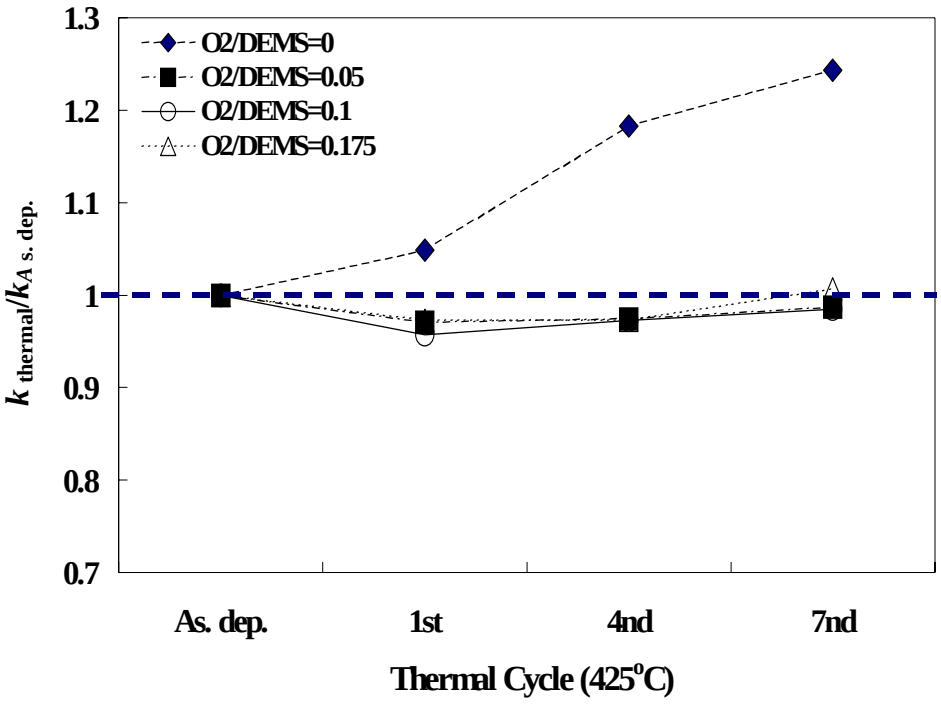


Figure 5-5-4. The dielectric constant (1MHz) change of the *low-k* film after 7 times 425°C thermal cycle.

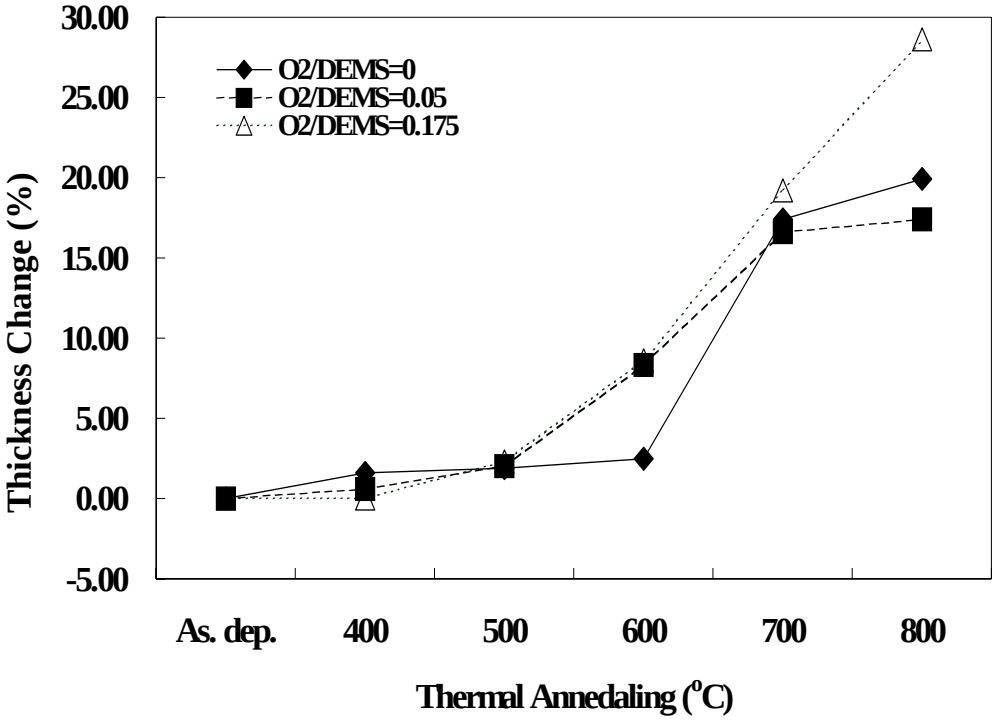


Figure 5-5-5. The thickness change of the *low-k* film after thermal tests with temperature ranging from 400 to 800 °C.

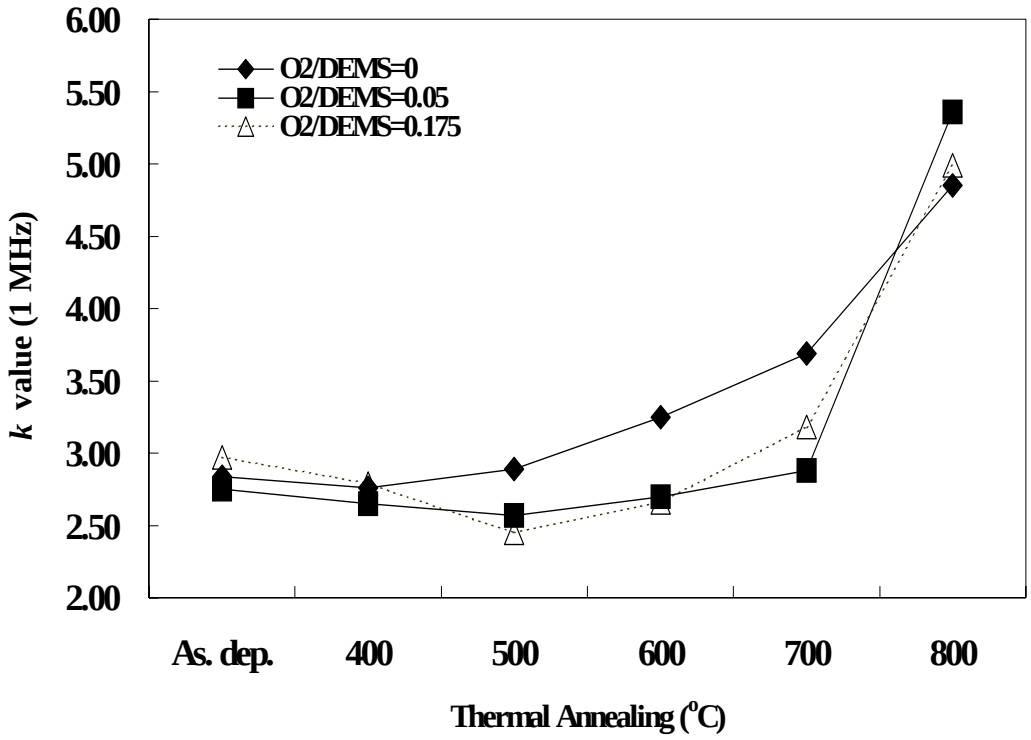
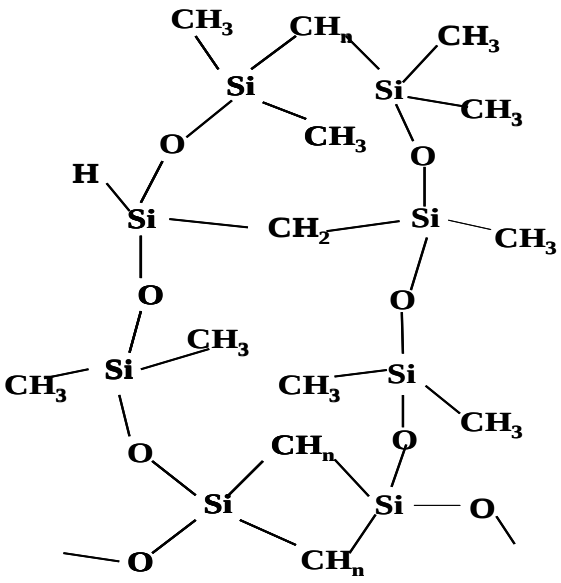


Figure 5-5- 6. The dielectric constant (1MHz) change of the *low-k* film after thermal tests with temperature ranging from 400 to 800 °C.

(a) DEMS low-*k*



(b) DEMS +O_2 low-*k*

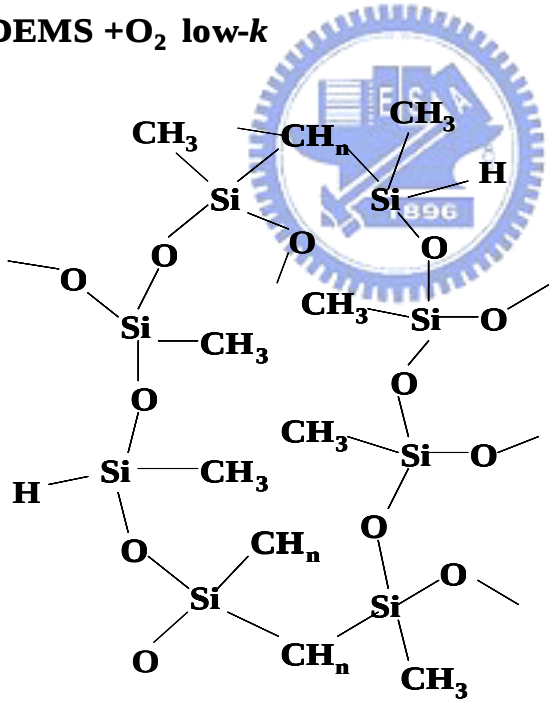


Figure 5-5-7. Schematics of the chemical bonding structure (a) DEMS; (b) DEMS+O_2.

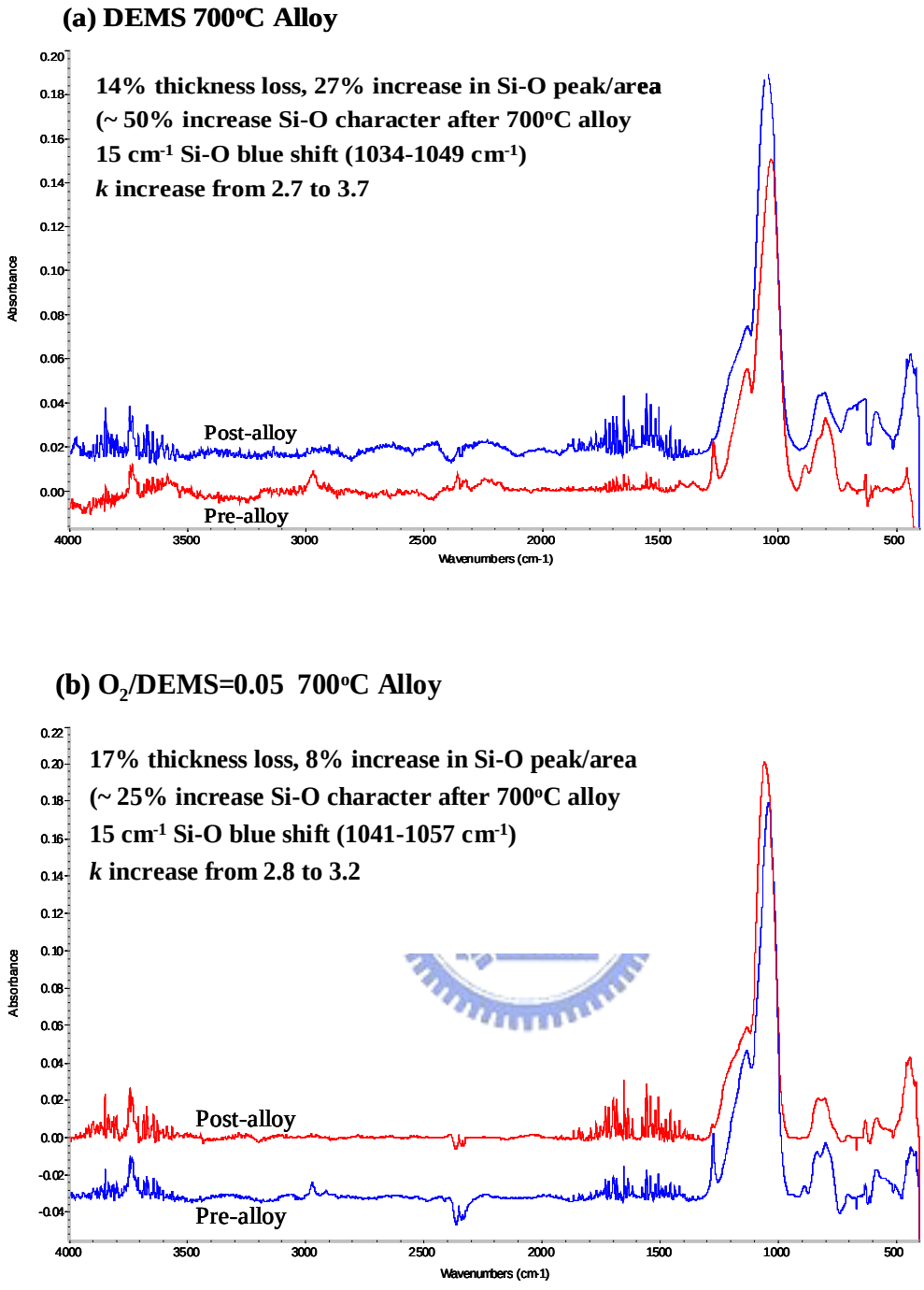


Figure 5-5-8. FTIR spectrum change of the *low-k* film after 700°C thermal test (a) DEMS; (b) DEMS+O_2.

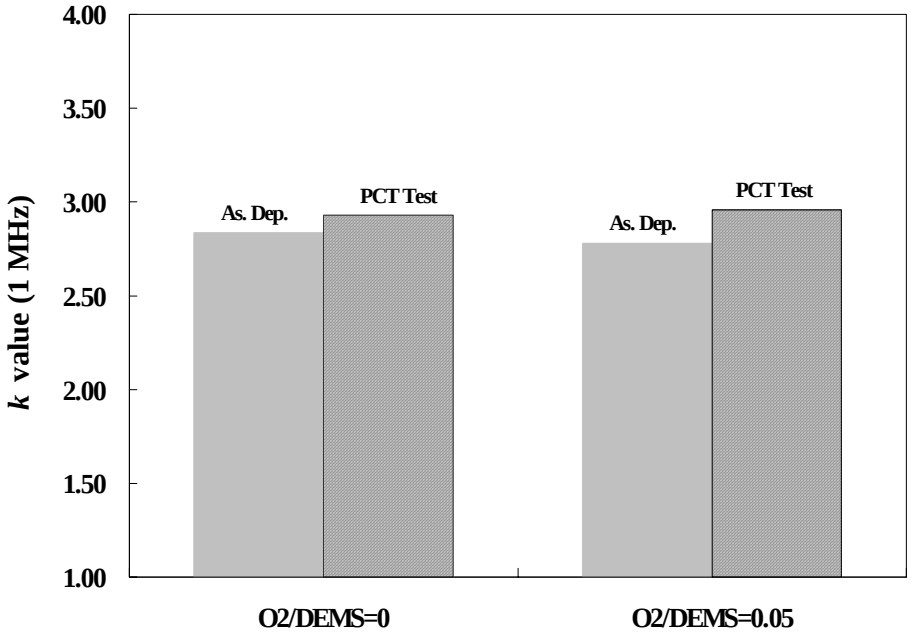


Figure 5-5-9. The dielectric constant (1MHz) change of the *low-k* film after 168 hours PCT test.

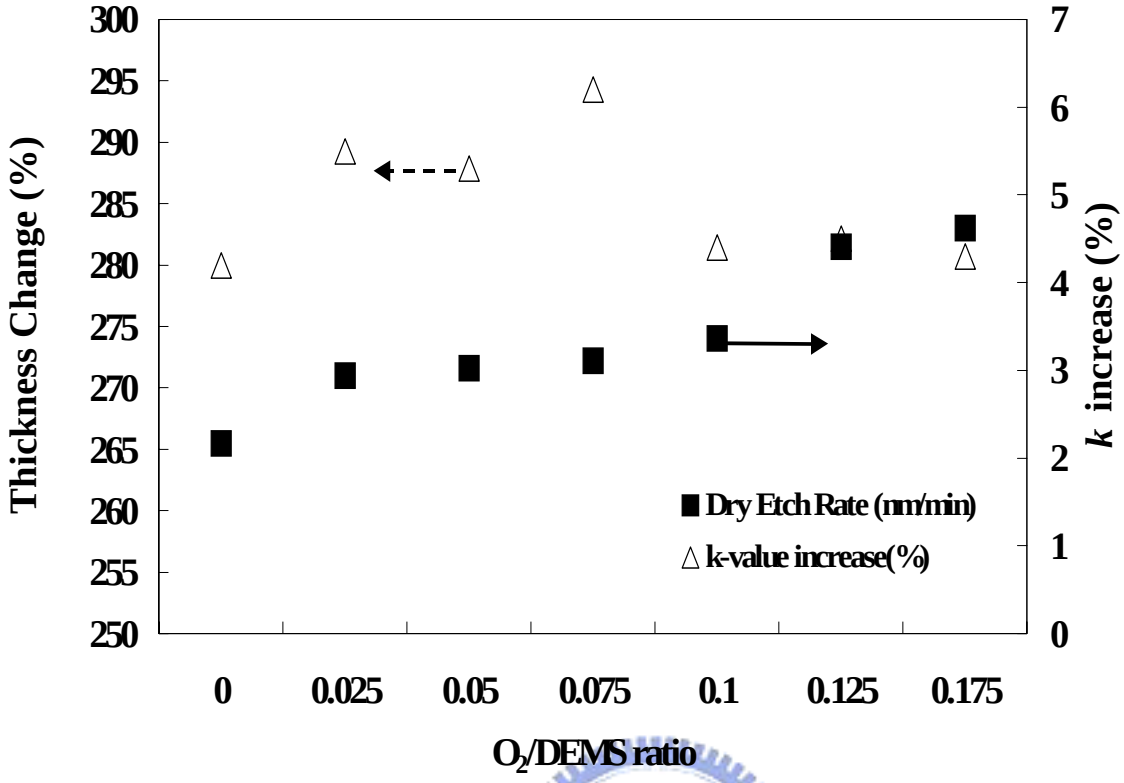


Figure 5-5-10. The dry etch rate and dielectric constant (1MHz) change of the *low-k* film as a function of the ratio of O_2/DEMS.

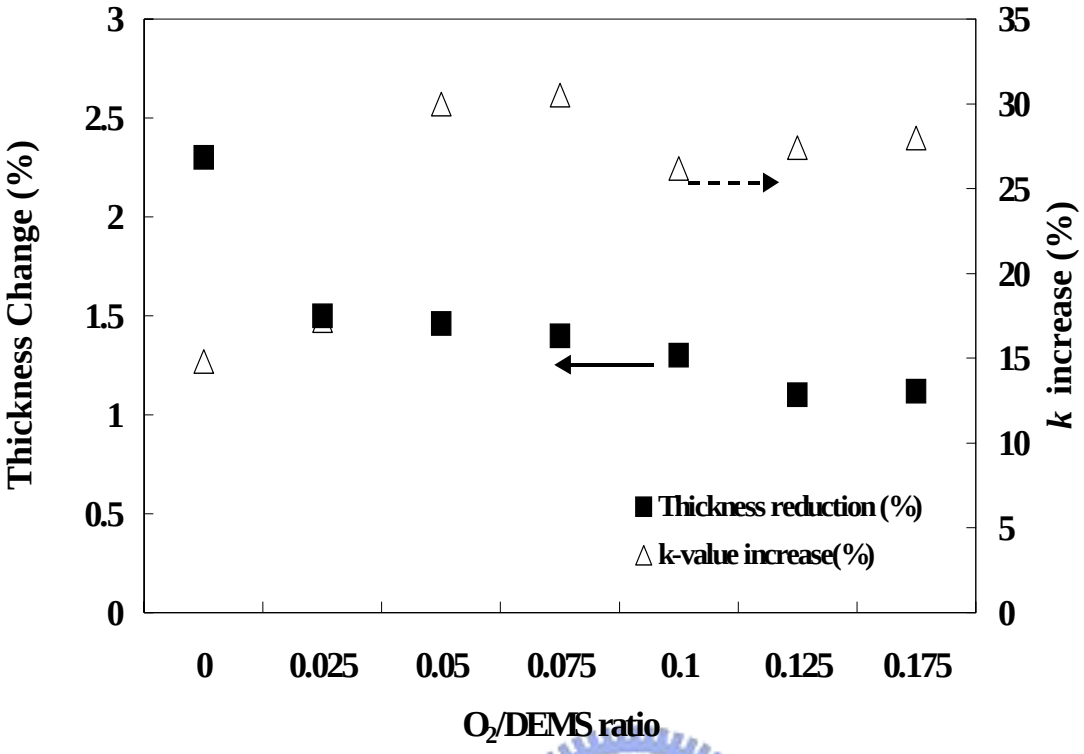


Figure 5-5-11. The thickness and dielectric constant (1MHz) change of the *low-k* film after O_2 plasma ashing as a function of the ratio of O_2/DEMS.

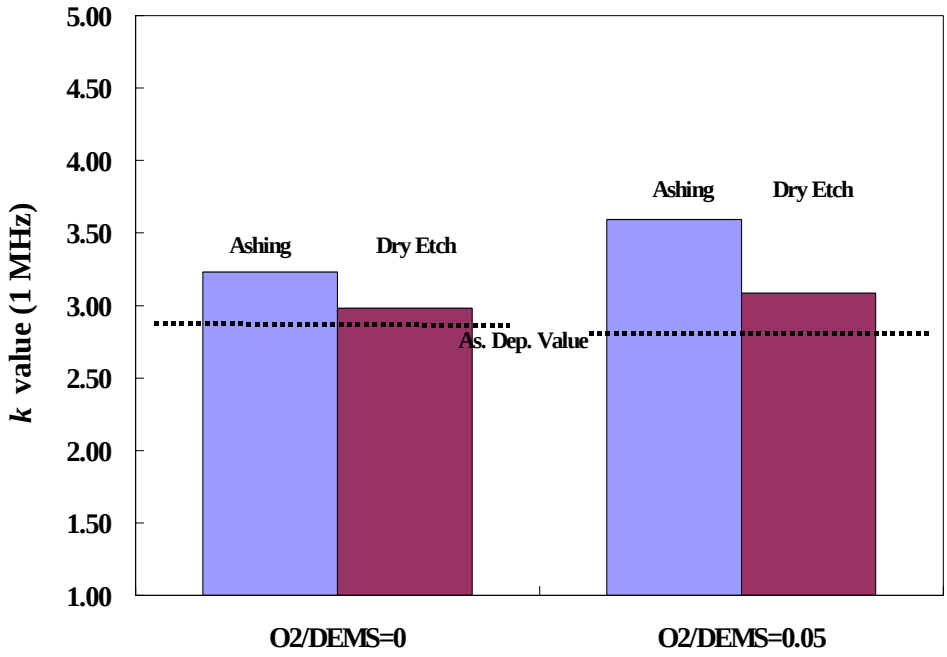


Figure 5-5-12. The dielectric constant (1MHz) change of the *low-k* film by remove the surface layer.

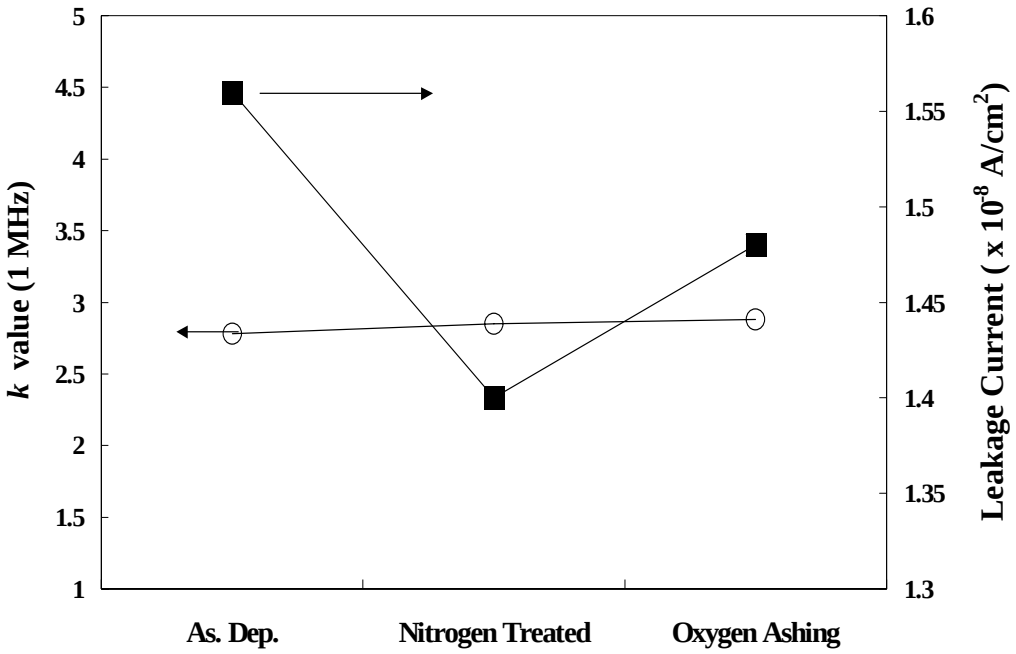


Figure 5-5-13. The dielectric constant (1MHz) and leakage current oat 2MV/cm change of the nitrogen treated *low-k* film after O_2 plasma ashing.

Chapter 6

Characterization of Fluorine-incorporation Siloxane-Based Low-Dielectric-Constant Material

6-1 Organoflurosilicate Glass (OFSG)- A Dense Low-Dielectric-Constant Material

6-1-1 Motivation

A major challenge in the fabrication of integrated circuits with critical geometries below 130 nm has been the development interlayer dielectrics (ILDs) with low dielectric constant (k) values that possess sufficient mechanical strength, thermal stability, and adhesive strength required for integration. Currently, fluorosilicate glass (FSG; k = 3.6) is used in advanced devices. It is well known that the Si-F species is very effective at reducing the dielectric constant due to the low polarizability of the Si-F bond [164]. The introduction of approximately 5 atomic percent fluorine to a silicate network, in the form of Si-F, lowers the k by about 10%. However, because of stability issues a further reduction in k via addition of more fluorine is not a viable solution for the next generation ILD materials. This limitation led to development of organosilicate glasses (OSG) [165, 166] for next generation ILD in which k is lowered by introducing bulky, non-polar organic species to the Si-O network. The significant reduction in k that this affords comes at the cost of significantly diminished mechanical strength. The presence of organic groups within the ILD material may also

impact the thermal and oxidative stability of the film. Because of these issues the pace for implementing new low dielectric constant materials is much slower than anticipated just a few years ago.

The primary need for ILD materials is to provide the requisite materials properties for integration at the lowest possible *k* values. Striking a balance between lowering *k* and maximizing mechanical strength requires optimizing the type and amount of species introduced to a silicate material. Herein we describe organofluorosilicate glass (OFSG), a new material that captures the synergy of Si-F and organic groups. Through the addition of SiF_4 to trimethylsilane-based OSG recipes (3MS-OSG), the more weakly bound and chemically susceptible organic species are effectively replaced with Si-F groups. This minimizes disruptions to the silicate network, providing a denser material with improved mechanical, electrical, and thermal properties at similar dielectric constants to analogous OSG materials.

6-1-2 Experimental Procedures

All films were deposited on 200 mm Si wafers in an Applied Materials DxZ chamber from mixtures of trimethylsilane (3MS, Dow Corning® Z3MS™ CVD precursor), tetrafluorosilane (SiF_4), and oxygen (O_2). Design of experiment methodologies were used to define parameter space for stable plasma and uniform deposition conditions, as well as for optimizing the electrical and mechanical properties for the material. Film thickness and refractive index were measured by reflectometry and ellipsometry. Dielectric constant measurements were performed by mercury probe on low resistivity wafers (< 0.02 ohm-cm). Sample modulus/hardness were assessed by nanoindentation using a MTS model SA-2 on films > 750 nm thickness following manufacturers protocol (multi-sample average, modulus /

hardness quoted at 50/100 nm depth, respectively). Rutherford Backscattering/Hydrogen Forward Scattering (RBS/HFS) were used to determine film composition. Film composition and bonding structure were assessed by X-ray Photoelectron Spectroscopy (XPS) after 30 seconds of argon ion sputtering to remove the surface layer, transmission FT-IR on high resistivity wafers (> 20 ohm-cm), Carbon-13 and Silicon-29 Nuclear Magnetic Resonance (NMR), and Dynamic Secondary Ion Mass Spectrometry. X-ray Reflectivity (XRR) measurements were used to determine film density. Thermogravimetric Analysis (TGA) was used to quantify weight loss by exposing samples under nitrogen atmosphere (100 sccm dynamic flow) to a thermal ramp at 10°C/min to 425°C where the sample was held isothermal for a minimum of 4 h. The adhesive/cohesive strength of materials to various interfaces was assessed by stud pull testing using manufacturers standard protocol.

6-1-3 Results and Discussions

A. OFSG Properties

For the particular materials properties targeted for OFSG, the optimum balance between dielectric constant and hardness is achieved from gaseous mixtures of 3MS:SiF_4:O_2 in the approximate ratio 10:5:3, while the 3MS:O_2 ratio used for 3MS-OSG films was ~ 6:1. Material properties for OFSG were not strongly dependent upon SiF_4 flow in the region surrounding the optimized ratios. The properties of optimized OFSG and 3MS-OSG films are compared in Figure 6-1-1. Superior mechanical and electrical properties are found for OFSG relative to 3MS-OSG, with essentially no difference in throughput as determined by relative deposition and etch rates. Leakage currents for OFSG are almost an order of magnitude lower

than 3MS-OSG (~3E-8 A/cm^2 versus ~ 2E-7 A/cm^2 at 2 MV/cm, respectively). Breakdown voltage for OFSG was also slightly superior to 3MS-OSG (> 6 MV/cm versus ~ 5.5 MV/cm, respectively).

Adhesive strength of 3MS-OSG and OFSG to various commercial barrier layer materials performed by stud pull analysis are compared in Figure 6-1-2. All data shown are for samples that were processed through a surrogate Cu-alloy routine: 7 cycles for 30 min. dwell at 400 ºC in N_2 ambient. All samples possess ILD as the top layer and silicon as the base substrate. For all cases tested the adhesion of OFSG is superior to 3MS-OSG. The most common failure mode for OFSG test samples is at the epoxy-stud interface, registering as high as 70 MPa for OFSG/SiN and OFSG/SiOC. In these cases stud pull analysis provides only a measure of the minimum adhesive and cohesive strengths of film. The most common failure mode for 3MS-OSG is between the ILD and barrier; adhesion of 3MS-OSG to SiOC and SiCN fails catastrophically at the ILD/barrier interface as indicated by the significantly larger adhesive strength of OFSG. In general we observed that the types of barrier material and process conditions used to deposit the ILD materials directly impact the adhesive strength and failure location. Various plasma pretreatments of barrier surface (e.g., oxidative plasma) prior to depositing 3MS-OSG films improves adhesion in most cases, approaching that measured for OFSG. Similar pretreatments have little beneficial effect on adhesive strength of OFSG. We speculate that the OFSG deposition process eliminates interfacial

issues that the analogous 3MS-OSG depositions apparently do not.

Film residual stress resulting from interfacial stresses can play a critical role in adhesive behavior of layered materials. This is of particular importance in IC manufacturing when multi-layered systems are exposed to thermal cycling from the copper alloying process. OFSG affords significantly reduced residual stress, measuring ~ 20 MPa (tensile) relative to ~ 50 MPa (tensile) for 3MS-OSG. Stress hysteresis measurements shown in Figure 6-1-3 for OFSG and 3MS-OSG indicate fairly stable profiles for both materials through the first and second scan from ambient to 400°C; a stress hysteresis of 0.6 MPa was measured for OFSG relative to 1.5 MPa for 3MS-OSG. The change in stress from ambient to 400°C, however, was substantially reduced for OFSG, changing by ~ 25 MPa over the entire scan reaching a non-stressed state relative to the silicon wafer at elevated temperatures. Comparatively, 3MS-OSG stress- temperature profiles indicate a large change in residual stress of ~ 100 MPa (~50 MPa tensile at ambient temperatures to ~50 MPa compressive at 400 °C). Both higher residual stress and the large temperature dependence of stress for 3MS-OSG appear to contribute to its reduced adhesive strength.

B. Composition and Structure

Compositional analyses by X-ray photoelectron spectroscopy and Rutherford backscattering/hydrogen forward scattering are shown in Table 6-1-1. A fluorine concentration of approximately 2-3 atomic percent is typical for optimized OFSG. As silicon

and oxygen concentrations are very similar to 3MS-OSG, it appears that the addition of fluorine primarily affects the carbon content of OFSG films. The C:H ratio for both materials being approximately 0.6 suggests that a distribution of carbon types exist in these films, including terminal methyl groups as well as network forming methylene, methyne, and fully networked carbon. Analysis of OFSG by ^{13}C-NMR indicates a dominant peak assigned to Si-CH_3 at ~ 0 ppm with slight asymmetry on its downfield shoulder likely arising from networked carbon groups (eg. Si-CH_2-, Si-CH-). Neither ^{13}C-NMR nor XPS provide evidence for C-F bonds within OFSG. The structural similarities between OFSG and 3MS-OSG are displayed in the ^{29}Si NMR spectra for these films in Figure 6-1-4. The main differences in the OFSG spectrum compared to 3MS-OSG are a relatively smaller presence of trimethylsilyl group located slightly downfield of 0 ppm and the potential presence of a band at ~ 125ppm upfield most likely due to Si-F [168].

The FT-IR spectra shown in Figure 6-1-5 for representative OFSG and 3MS-OSG films reflect the structural similarities of the films. A blue-shift of the Si-O absorption from 1030 to 1045 cm^{-1} suggests the presence of Si-F bonds in the OFSG, however Si-C absorptions in the range below 950 cm^{-1} masks quantitative determination. The shift in Si-O absorption is related to a change in the bond angle for Si-O species adjacent to Si-F [168]. Evidence of slightly reduced C-H and Si-CH_3 absorptions in the FT-IR correlates with reduced carbon content determined by XPS and RBS/HFS. A reduction in residual Si-H

incorporated from the trimethylsilane precursor is apparent in OFSG relative to 3MS-OSG. We believe that the presence of fluorine radicals or trifluorosilyl species generated by the plasma may act as hydrogen scavengers. Spectra for both OFSG and 3MS-OSG provide evidence for networked carbon groups (e.g., methylene bridges) as noted by a weak absorption at 1360 cm^{-1}. In addition, both indicate evidence for multi-methyl substituted Si (e.g., trimethylsilyl) from absorptions centered ~1270 cm^{-1}. Monomethylsilyl substituents in 3MS-OSG have a narrow absorption centered at 1275 cm^{-1}, while trimethylsilyl groups show absorptions near 1260 cm^{-1}. The non-Gaussian nature of the features suggest multiple absorptions, and corroborates NMR evidence for multi-methyl substituted silicon atoms in both OFSG and 3MS-OSG.

X-ray reflectivity measurements indicate an approximate 10% increase in density of OFSG relative to 3MS-OSG. This increased density is mostly likely the result of Si-F bonds occupying approximately 50% less volume than $Si-CH_3$ groups and a reduction in trimethylsilyl substituents [166]. Increases in density typically will cause a concomitant increase in dielectric constant because polarizable atoms are substituted for void space. However, the Pauling estimates for the polarizabilities of fluorine and carbon show that fluorine is significantly less polarizable [169]. The reduction in free volume is balanced by decreased polarizability, thus retaining the low-dielectric properties while significantly increasing the mechanical strength of the material.

C. Thermal Stability

Both OFSG and 3MS-OSG have excellent thermal resistance up to 600°C, as indicated by less than 5% reduction in thickness and no significant change in refractive index (1.405 +/- 0.010 for 3MS-OSG versus 1.446 +/- 0.010 for OFSG) after prolonged exposure. Thermal gravimetric analysis, at isothermal conditions (inert, 425°C), indicates that both 3MS-OSG and OFSG materials experience weight loss of less than 0.1 wt%/h. Introduction of air to the test chamber while still at 425°C results in instantaneous weight loss of approximately 2% for 3MS-OSG materials and no measurable change in weight is seen for OFSG, indicating superior thermo-oxidative stability for OFSG.

Dynamic SIMS profiles for 500 nm 3MS-OSG/1000 nm OFSG layered samples are shown in Figure 6-1-6 for pre and post-anneal conditions (425°C, air, 30 mins.). The spectra indicate little change in the distribution and concentration of fluorine within OFSG. This suggests the fluorine incorporated within OFSG is very stable to thermally-induced migration. Recent experimental evidence indicates OFSG possesses a greater stability than FSG to thermally induced fluorine migration [168]. It is believed that the low fluorine content and reduction in Si-H species contributes significantly to the stability of this material [169]. Also noticeable in Figure 6-1-6 is a significant reduction in the carbon content of the post-annealed 3MS-OSG layer. Dielectric measurements of OFSG and 3MS-OSG samples after air exposure at 425°C indicate an increase of up to 0.5 in *k* value for 3MS-OSG with no measurable increase for OFSG. It is proposed that the addition of SiF_4 to the deposition enables the removal and replacement of less thermally stable organic species with Si-F bonds.

6-1-4 Summary

A new low *k* interlayer dielectric material, organofluorosilicate glass, has been developed and characterized. The addition of silicon tetrafluoride to a trimethylsilane-based

organosilicate glass deposition process provides chemical and structural changes to the deposited film that result in improved mechanical strength at comparable dielectric constants to their non-fluorinated analogs. The presence of SiF_4 in the plasma affects the replacement of more labile organic species with 2-3 atomic percent inorganic fluorine, providing enhanced material stability. The chemical and structural changes also result in enhanced adhesive strength and reduced residual stress and stress hysteresis. Materials properties displayed by OFSG suggest its candidacy for advanced ILD applications.

6-2 Moisture Resistance and Thermal Stability of Fluorine-incorporation Siloxane-Based Low-Dielectric-Constant Material

6-2-1 Motivation

Low parasitic capacitance multilevel interconnects using low dielectric constant interlayer dielectrics are essential for high-speed ultra large-scale integrated circuits (ULSIs). Organo-silica-glass (OSG, k=2.8~3.3) deposited by PE-CVD technology has received more attention recently due to their potential to fit into existing processing schemes. It is the reduced mechanical strength of OSG materials as a result of replacement of oxygen from the silicate network with organic groups such as Si-CH_3 bonds that is a main issue for integrated circuit fabrication. Here we study the heat and moisture resistance of a newly developed low-k material, organofluoroisilicate glass (OFSG), within fluorine is incorporated into the structure as Si-F only. The resulting material is endowed with higher mechanical strength and improved adhesion [170,171], providing enhanced resistance to cracking of multi-layer

structures-and film peeling due to chemical-mechanical planarization.

To ensure high process yield, device performance and reliability over its lifetime, the electrical properties (dielectric constant, and breakdown voltage, leakage current) of interlayer/intermetal dielectric materials need to be resistant to thermal and moisture stresses. The heat resistance is necessary since wafers are exposed to temperatures over 400^{o}C during fabrication of upper-level interconnects. Since thermal treatment is required after completion of each level of the interconnect structure, the lower level interlayer dielectrics are subjected to many hours of heating. Additionally, moisture resistance is necessary for long-term reliability after packaging. In real operating conditions, the ILDs are subjected to moisture penetrating from the outside the environment. The effect of this moisture penetration is commonly evaluated by accelerated humidity tests.

The effects of heat and moisture exposure on OSG and OFSG films is investigated in this paper. The effect of fluorine addition to the silicate network is assessed by physical and reliability properties of these films. The result of the relationships between the dielectric constant stability, surface chemical composition and electric properties are reported and discussed.

6-2-2 Experimental Procedures

The deposition of the OSG and OFSG films were carried out in a Plasma Enhanced

Chemical Vapor Deposition (PE-CVD) system with 13.56 MHz operating rf. The substrates used in this study were B-doped p-type 200 mm silicon wafers with (100) orientation. The deposition temperature was maintained at 350^{o}C; process pressure and rf power were set at 4 torr and 600 Watts, respectively. Except for the addition of SiF_4, both materials were deposited using trimethysilane (Z3MS^{TM}, Air Products and Chemicals, Inc. and oxygen under similar conditions. The optimized process conditions and film properties are shown in Table I. Films with 300-500 nm thick were analyzed for thickness and refractive index (RI, at 248 and 633 nm) by reflectometry (SCI Film Tek 2000) and/or ellipsometer (Nano-Spec 9100). Transmission FT-IR spectra were measured using Bio-Rad spectrometer at 4cm^{-1} resolution. All spectra are an average of 32 scans and were background corrected to a silicon reference. Dielectric constant and leakage current were measured by mercury probe at 1MHz frequency. Atomic composition was determined by x-ray photoelectron spectroscopy (XPS) using a Physical Electronics 5000LS ESCA spectrometer after sputter with Ar^+ beam to remove the top 20Å of film.

Thermal stability of the films was assessed by furnace anneal in nitrogen ambient at temperature ranging from 300 to 700^{o}C. Thermal cycling 7 times for 30 minutes at 425^{o}C in nitrogen ambient was used to mimic stress encountered during copper alloy process. Moisture resistance was determined by exposing films to 120^{o}C and 100% relative humidity at 2 atmosphere pressure for up to 168 h.

6-2-3 Results and Discussions

The results of thermal exposure at 425^{o}C are show in Figure 6-2-1 to 6-2-3. The thickness of the OSG and OFSG films decreases continuously upon 425^{o}C heating tests (Figure 6-2-1). The maximum thickness reduction was found after the first time heating test, decrease slightly for each subsequent cycle, with OSG films showing higher shrinkage than OFSG films. The dielectric constant of OSG and OFSG films were essentially stable after thermal cycling (Figure 6-2-2). The change in RI and stress for OSG and OFSG (Figure 6-2-3) indicates that magnitude of change for RI of OFSG films is actually larger than that for OSG films. While the trend in RI and stress differ in direction the relative change is in good agreement, suggesting a common root cause. A possible explanation is that OFSG films have a more stable bonding structure due to replacement of thermally labile organic groups with Si-F species. The stability of film properties upon thermal cycling suggests that both OSG and OFSG film would retain their desirable properties through the thermal stresses experienced as a result of the copper alloy process. This clearly indicates that the OSG and OFSG films are suited for intermetal dielectrics on semiconductor due to there is at least 7-8 layers interconnect fabrication process and 400^{o}C is a minimal backend process for an interconnect fabrication process.

Figure 6-2-4 and 6-2-5 show the change of thickness, refractive index and dielectric

constant for furnace anneals from 300 to 700^{o}C for 1 h. The *k* value for both of the OSG and OFSG films were stable (*k*=3.2-3.3) up to 600^{o}C, however, exposure to a temperature of 700^{o}C resulted in sharp increase in the *k* value for both films. We infer that specific bonds in OSG and OFSG films, such as Si-CH_3 and Si-F, do not decompose at least up to 600^{o}C. This further exemplifies that both OFSG and OSG films have sufficient thermal resistance to withstand normal interconnect fabrication processes which do not typically exceed 400^{o}C.

Moisture stress test results are shown in Figure 6-2-6. The *k* values of the OSG film degraded slightly after 168hr PCT test, similar to the result of Takeshi, et al [127]. The *k* value of the OFSG films increase significantly to 3.8 only after the 10 h PCT test. Based on this result, attention should be paid to the moisture penetration when using the OFSG as ILD material.

Leakage current tests (Figure 6-2-7) for films pre- and post- PCT test indicate that both OFSG and OSG films increase significantly in current leakage after exposure. Breakdown voltages were also found to decrease from 6.3 MV/cm and 7.0 MV/cm to 5.6 MV/cm and 6.6 MV/cm for OSG and OFSG film, respectively. Interestingly, despite the degradation in *k* and suggested susceptibility to hydrolysis, leakage and breakdown testing indicates that the leakage current of OFSG films after exposure is still lower than that of OSG film even before the PCT test.

The FTIR spectra of the OSG and OFSG films before and after PCT test are displayed in

Figure 6-2-8 and 6-2-9, respectively. The FTIR spectrum of OFSG film shows a very weak, sharp absorbance at 3500 cm^{-1} appearing after PCT, suggestive of Si-OH bonds formation. The decomposition was gradual; the resulting films still contains Si-H bonds, and the films contains a little moisture. This explains the relatively minor changes seen in both materials upon thermal treatment. During the PCT test, however, the Si-H is found to decompose drastically; at the same time, fewer Si-F bonds is also decomposed due to the moisture absorption. Therefore, it results in much moisture absorption (Si-OH and H-OH). The reactions of Si-F, $Si-CH_3$ or Si-H bonds and H_2O can be expressed as the following formulas, respectively:

$$Si-F + H_2O \rightarrow Si-OH + HF \quad \textbf{(6-2-1)}$$

$$Si-OH + H_2O \rightarrow Si-OH + H_2 \quad \textbf{(6-2-2)}$$

$$Si-CH_3 + H_2O \rightarrow Si-OH + CH_4 \quad \textbf{(6-2-3)}$$

$$2Si-OH \rightarrow Si-O-Si + H_2O \quad \textbf{(6-2-4)}$$

During the PCT tests, the greater moisture absorption resulted in drastically decompose and incompletely condense. This result significantly increases both the *k*- value and leakage current, so the films degrade shown in Figure 6-2-5 and 6-2-6.

Comparing with the difference between the OFSG films and OSG films, OFSG films have less Si-H bonding and additional Si-F bonding which appears to be mainly due to Si-H bonds in OSG films replaced by Si-F bonds. The OSG film originally contains Si-CH3 and

Si-O-Si bonds, with lesser contributions from Si-H and Si-CH_2-Si species. According to the results of T. Furusawa ,et al [], the Si-C-Si species is thermally stable to 700^{o}C or higher. The heat resistance of the films is determined by the decomposition of the Si-H and Si-CH_3 bonds; the decomposition temperature of Si-H and Si-CH_3 bonds is about 700^{o}C and the bonds decompose completely at higher temperature, while no decomposition is observed for Si-C-Si, Si-H and Si-CH_3 bonds. The replacement of less thermally stable Si-H bonds by Si-F bonds results in the improved thermal stability and reduced shrinkage relative to OSG. However, the inferior moisture resistance of Si-F bonds results in poorer moisture resistance of OFSG compared to OSG films.

6-2-4 Summary

The resistance of organo-silicate glass (OSG) and fluorine-doping organo-silicate glass (OFSG) films against heat and moisture stress test was investigated. Compared with OSG films, the OFSG films were shown to be having superior thermal stability and electrical properties. The enhanced degradation of the dielectric constant of OFSG films during moisture stress tests was attributed to the hydrolytic instability of Si-F bonds. Consequently, similar to fluorosilicate glass, moisture resistance of the OFSG film will require attention during integration of this material.

6-3 The Fluorine effect on Siloxane-Based Low-Dielectric-Constant Material

6-3-1 Motivation

Improvements in interconnect insulator materials are required for superior circuit speeds, to mitigate the signal propagation delay, crosstalk and dynamic power consumption. A number of new materials have been developed for the semiconductor industry in the past years for their use in ultra-large scale integrated circuits (ULSIs) with critical geometries 130 nm and smaller. Therefore, ongoing effort has been invested to develop reliable lower-*k* materials and for their implementation in copper metallization schemes. The first true generation of low dielectric constant materials, fluorinated silicate glass (FSG, Si_xOF_y), is currently being scaled into volume production. However, FSG does not have low enough *k* value (*k* = 3.4~3.7) to meet the next generation requirements. Furthermore, high fluorine concentration can result in metal corrosion and high moisture sorption. Next generation materials with dielectric constant of 2.7 to 3.2 will likely be organic carbon doped silicates (OSG, SiCO:H). Recently, carbon-doped silicates have shown promise for ultralarge scale integrated circuits (ULSIs) intermetal dielectric applications. Nevertheless, inferior mechanical strength and adhesion to of the OSG to metals (Ta/TaN/TiN) relative to standard SiO_2 has proven to be a limiting factor for their integration into standard fabrication processes such as copper CMP process. Delamination can further cause issues such as metal thinning, dielectric thinning and scratching.

In light of these considerations for these two kinds of low-*k* material, to improve mechanical strength, fluorine incorporated into organo-silicate glass (OFSG) was developed. Even so, the control of fluorine concentration is an essential on depositing this film.

In this work, we will compare the physical and reliability properties of OFSG films with those of OSG films. The result of the relationships between the dielectric constant, surface chemical composition and adhesion are reported.

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6-3-2 Experimental Procedures

The deposition of the OSG and OFSG films were carried out in an Enhanced Plasma PE-CVD system with 13.56 MHz operating rf on Applied Material DxZ system. The substrates used in this study were B-doped p-type 8in. silicon wafers with (100) orientation. The deposition temperature was maintained at 350°C. The OFSG films were deposited by varying SiF_4 flow rate from 100-500 standard cubic centimeters per minute (sccm). By comparison, OSG films were deposited from reagent mixtures consisting of 150 sccm of oxygen (O_2) and 600 sccm of trimethysilane (3MS). The process pressure and rf power were set at 4 Torr and 600 W, respectively. The thickness and refractive index of 300-500 nm thick films were determined by reflectometry and ellipsometry. Atomic composition was determined by x-ray photoelectron spectroscopy (XPS) using a Physical Electronics 5000LS ESCA spectrometer after sputter with Ar^+ beam to remove the top 20Å of film. Transmission FT-IR spectra were measured using Bio-Rad spectrometer at $4cm^{-1}$ resolution. All spectra are an average of 32 scans, background corrected to a silicon reference. Dielectric constant and hardness were measured by mercury probe at 1 MHz and nanoindentation (MTS), respectively. The residual stress was measured by a Flexus stress measurement system, and adhesion strength was assessed by stud pull test.

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6-1-3 Results and Discussions

It was observed that the deposition rates of the OSG and OFSG films with 100 sccm of SiF_4 flow rate were 6.38 and 5.0 nm/min., respectively. It is supposed that the decrease in the deposition rate for OFSG is due to an etching effect of SiF_4. Furthermore, the deposition rate inhibits slightly decrease as SiF_4 flow increased (100-500 sccm), whereas the etching effect of SiF_4 was considered to be insignificant for different SiF_4 flow in this experiment (Figure

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6-3-1).

The as-deposited film composition was analyzed by XPS, which detected Si (2p), O (1s), C (1p) and F (1s). Table 6-3-1 shows the dependence of the atomic percentages of the atomic percentages of Si, O, C and F on the SiF_4 gas flow rate. While the at. % of Si and O_2 are nearly independent of SiF_4 flow rate, the at. % of fluorine increases at the expense of carbon, suggesting that the presence of SiF_4 effects the replacement of carbon in the film with fluorine.

Figure 6-3-2 displays typical FTIR spectra of the OSG compared to OFSG at different SiF_4 flow rates to further investigate changes in the film structure as fluorine becomes incorporated into an organosilicate film. All films prepared from $3MS/O_2/SiF_4$ show absorption in the region typical for Si-F absorption (930 cm^{-1}). That is, an extra Si-F peak is found for OFSG films. However overlap of the Si-F peak with S-C bonds in the region makes quantitative analysis difficult. The 1272 cm^{-1} absorption peak is the characteristic peak of the carbon-doped SiO_2 film, arising form the symmetric deformation vibration of CH_3 from $Si-CH_3$ group. The weak absorption peak around 1370 cm^{-1} results from the presence of $Si-CH_2-Si$ groups. The absorption peaks corresponding to Si-O stretching and bending vibration modes were observed for all films at around 1040 and 808 cm^{-1}, respectively. The Si-H vibration (2158 and 2235 cm^{-1}) are present in all conditions, but with different relative intensity. CH_m, m=1-3, stretching is at 2890-2990 cm^{-1}. The effect of increasing SiF_4 flow is

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an incremental shift of Si-O vibration peak position from 1030 cm^{-1} toward higher waves numbers until the value of 1040 cm^{-1}, accompanied by a reduction of the peak FWHM from 81.1 to 45.8 cm^{-1}. This is due to the high electron affinity and electronegativity of fluorine attracts more electrons closer to the fluorine ions and depletes the electrons in the neighboring Si-O-Si bonds. This brings about the direct effect of weakening the Si-O-Si bonds so that the films become less rigid and "more stretchable", resulting in a higher stretching frequency. As depicted in Figure 6-3-2, the Si-CH_3/Si-O peak height at 1272 cm^{-1} and 800cm^{-1} decreases with SiF_4 flow (this is due to reduced film thickness). The peak position of Si-CH_3 at about 1272 cm^{-1} moves slightly toward higher wave-number with increasing SiF_4 flow. Figure 6-3-3 presents the variation of content of Si-CH_3 (1272 cm^{-1}) and C-H (3000 cm^{-1}) in the films as a function of SiF_4 flow. The content of Si-CH_3 and C-H_m is analyzed by calculating the peak height ratio. The results tell that the content of Si-CH_3 and CH_m decreases with increasing SiF_4 flow. Moreover, as SiF_4 flow exceeds 300 sccm, the Si-H vibrations are nearly absent. This implies as the SiF_4 vapor is introduced into the deposition chamber, Si-F bonding will replace organic groups and Si-H bonds at the same time.

The refractive index of dielectric films of constant composition and bonding structure can be used to reflect film density. A higher refractive index represents a higher film density, which means less porosity. Figure 6-3-4 presents the variation of refractive index of the films as a function of the SiF_4 flow rate. The refractive indexes increased with SiF_4 flow rate, but

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reach saturation as SiF_4 flow is 400 sccm. The observed refractive indexes dependence of SiF_4 flow may be explained by the film structure variation indicated in FTIR spectra and the change in film porosity (as discuss in the next section).

Figure 6-3-5 and 6-3-6 show mechanical strength and dielectric constant of the films deposited with different SiF_4 flow. It is interesting to note the mechanical strength and dielectric constant trend of OSG film with different SiF_4 flows was trade-off. As SiF_4 flow increases, the dielectric constant and nanoindentation hardness both shift to higher values.

Two hypotheses account for reducing the dielectric constant of OFSG films can be summarized by the following statements: one is fluorine and methyl group incorporation leads to less dense, more porous film by creating voids in the SiO_2 matrix, the other is Si-F/Si-CH_3 reduces the electronic polarizability of the matrix and thus the electronic contribution to the dielectric constant. Si-CH_3 would create more porosity due to its mass group and fluorine is significant less polarizable. As SiF_4 is flushed into process chamber, the more Si-CH_3 bonding was replaced by Si-F bonding as more SiF_4 flow. Increasing the density (increased refractive index) makes the film dielectric constant increase, which indicates the content of Si-CH_3 is dominant factor contribution to the dielectric constant over the content of Si-F bonds. Besides, comparing bonding energy between Si-F and Si-CH_3, the bonding energy of Si-F is about 136 J/mole, higher than bonding energy of Si-CH_3 (83 J/mole). Therefore, the mechanical strength of OFSG films improved as fluorine incorporated into

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OSG films. It is known that the current low *k* value dielectric films as OSG, Silk films suffer lower mechanical strength (hardness is about 1.0-1.5 Gpa), which cause CMP and package problems in manufacture. By incorporating fluorine into OFSG films makes it a potential (and better) substitute to OSG films to be implemented as an IMD film in the integration scheme.

Figure 6-3-7 shows the change of residual stress with respect to an initial stress value, the change of stress was as function of storage time in 45% RH air. The stress becomes less tensile with the storage time and SiF_4 flow rate. The film deposited at SiF_4=100~300sccm shows little change (2%). However, the stress change of the film deposited at SiF_4=400sccm can be reached 4% change after 2 weeks storage time. The result implies that higher amounts of fluorine may promote the water absorption, as has been observed in FSG materials.

The other concern is adhesion of the low k material to other films it is in contact with such as Cu barrier layers. Figure 6-3-8 compares the adhesion strength for OSG and OFSG films. The results were obtained by stud-pull methodology. It was found that the adhesion strength of OFSG films was higher than that of OSG film when in contact with Nitride, silicon carbide and Titanium nitride. For SiCN and SiCO barrier layers significantly larger adhesive strength determined for OFSG reflects a catastrophic failure of the OSG material at the interface. The type of layered materials and respective process conditions have a dramatic effect upon adhesive strength and failure location. The significantly reduced residual film stress and stress-temperature profile for OFSG relative to OSG (shown in previous paragraph 6-1) may be one of the roots causes of the superior adhesion of OFSG films.

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6-3-4 Summary

The effects of the fluorine concentration on the dielectric properties of organo-silica-glass (OSG) films were investigated in this study. The relationship between film properties and chemical structure has been investigated by FTIR, XPS analysis and measurement of deposition rate, refractive index and dielectric constant. The OFSG films from 3MS, O_2, and SiF_4 show lower deposition rate than that from 3MS and O_2. The addition of SiF_4 can reduce the content of $Si\text{-}CH_3$, which increase film mechanical strength. As the SiF_4 flow rate increased, the dielectric constant slightly increases but hardness significant improve. The mechanical strength and adhesion ability between different barrier layer (SiN /SiCN/TiN) of OSG film also increase as Fluorine incorporation.

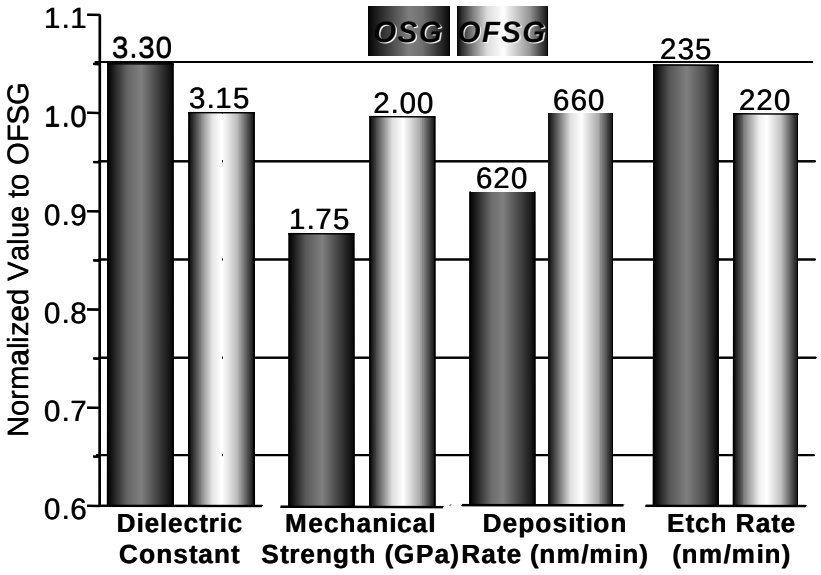


Figure 6-1-1. Optimum materials properties for trimethylsilane-based OSG and OFSG films.

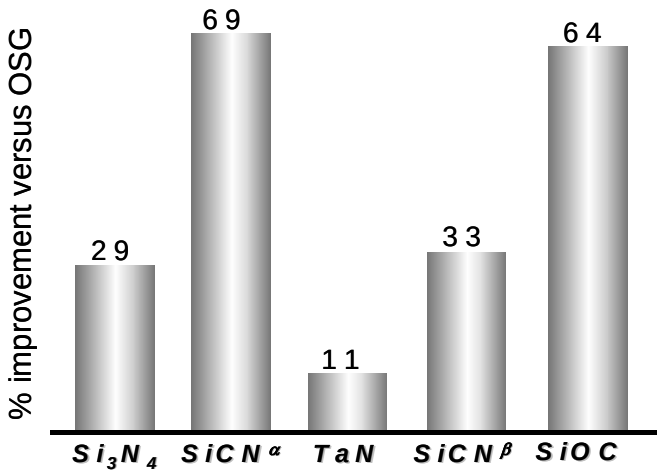


Figure 6-1-2. Relative adhesive strengths for trimethylsilane-based OSG and OFSG films.

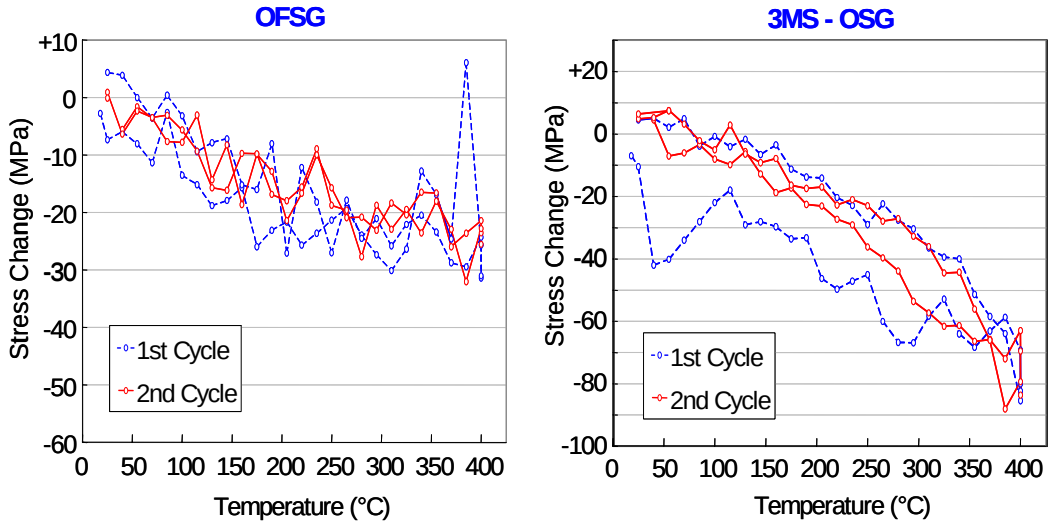


Figure 6-1-3. Stress hysteresis profiles for OFSG and OSG.

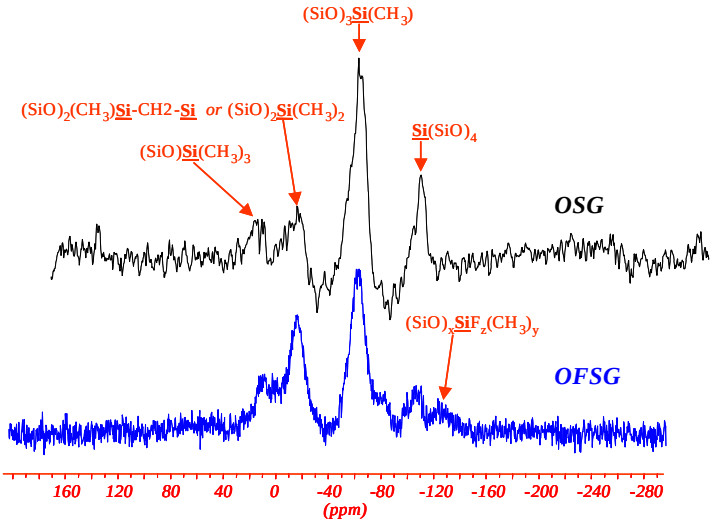


Figure 6-1-4. ^{29}Si-NMR of 3MS-OSG and OFSG.

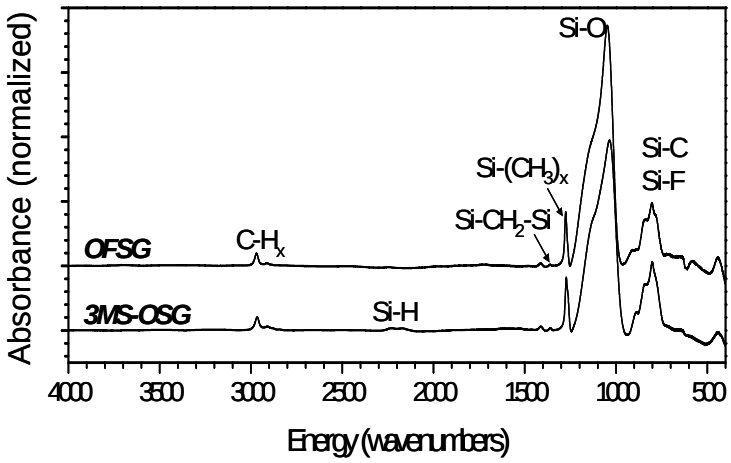


Figure 6-1-5. FT-IR spectra for 3MS-OSG and OFSG

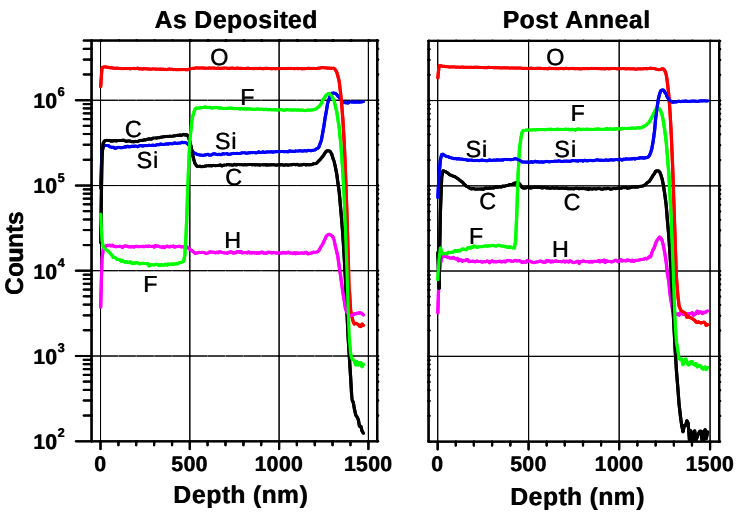


Figure 6-1-6. Dynamic Secondary Ion Mass Spectrometry profiles.

Table 6-2-1. Process Conditions and Film Properties of OFSG and OSG Film

	OFSG	OSG
Process Conditions		
3MS(sccm)	540	540
O2(sccm)	150	150
SiF4(sccm)	250	
RF power(W)	600	600
Pressure(Torr)	4	4
Temperature (^{o}C)	4	4
Film Properties		
Refrative Index	1.45	1.41
Dielectric Constant	3.2	3.3
Modulus (Gpa)	12.5	8
Hardness(H, Gpa)	1.98	1.76
Deposition Rate(mm/min)	450	670

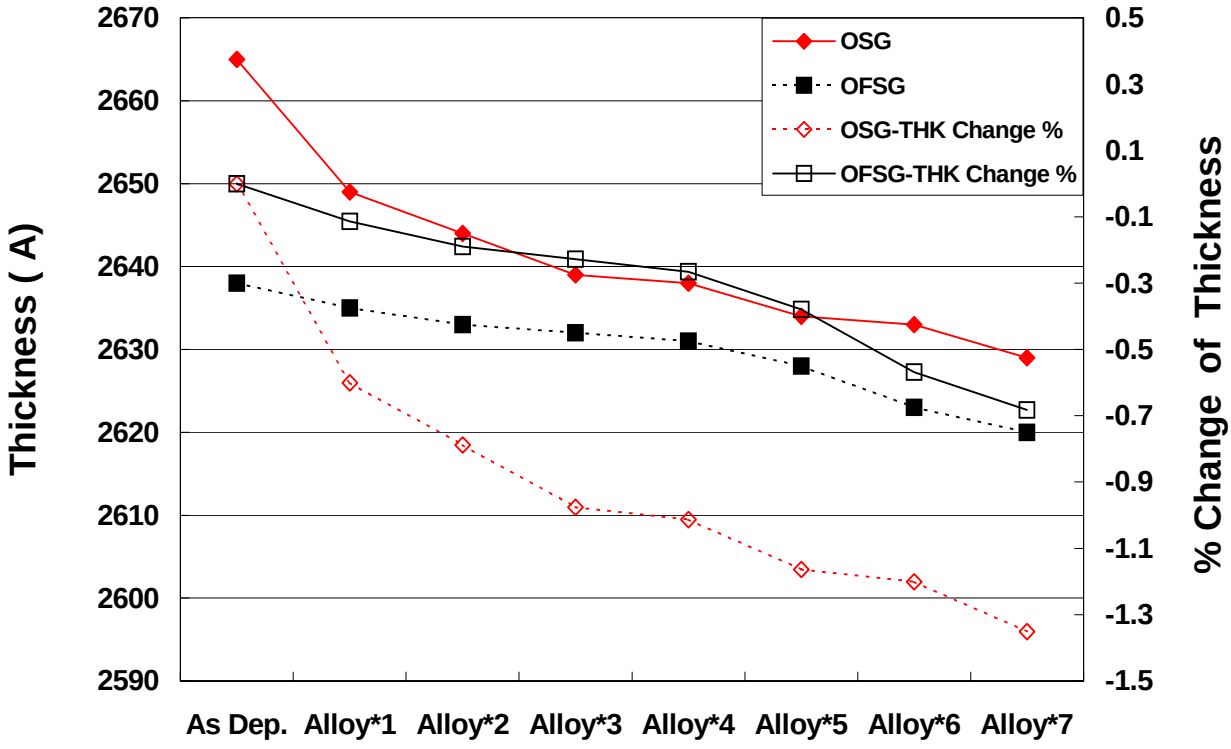


Figure 6-2-1. Heating test (425°C Alloy) on thickness change for OSG and OFSG films.

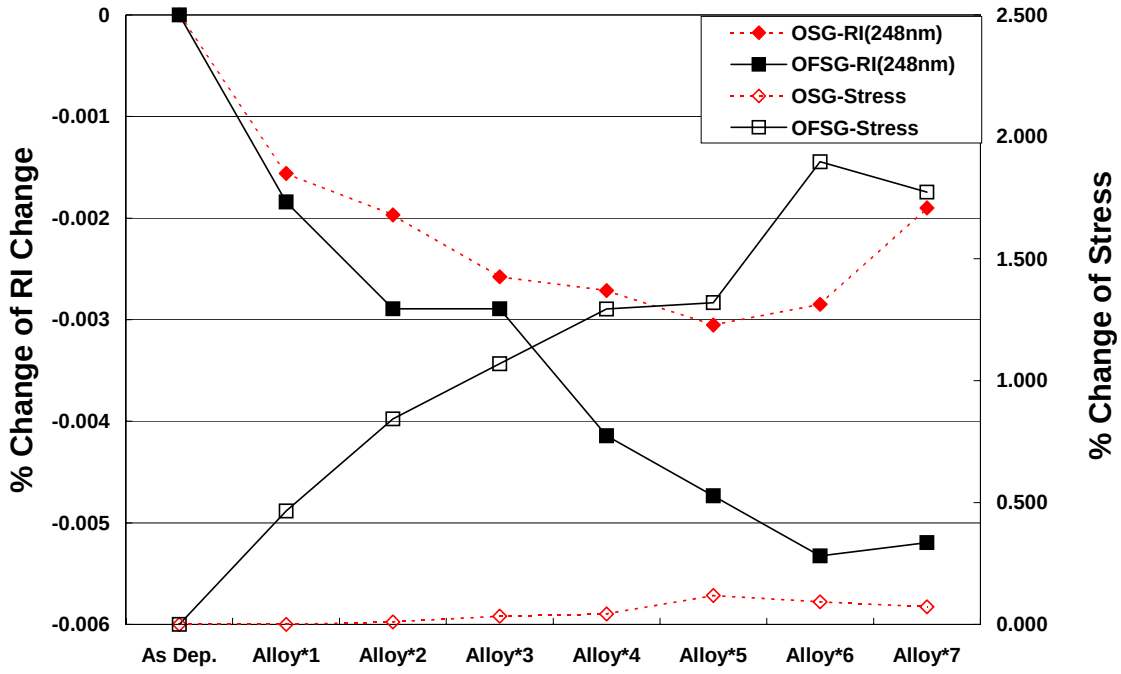


Figure 6-2-2. Heating test (425°C Alloy) on refractive index and stress change for OSG and OFSG films.

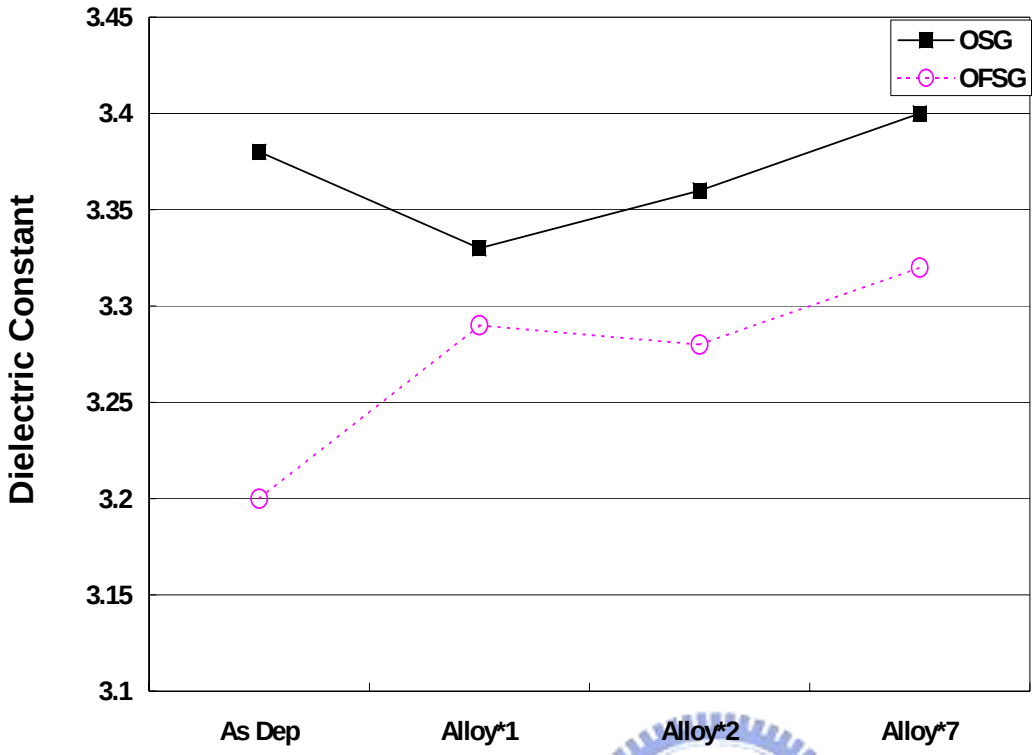


Figure 6-2-3. Effect of Heating test (425°C Alloy) on dielectric constant for OSG and OFSG films.

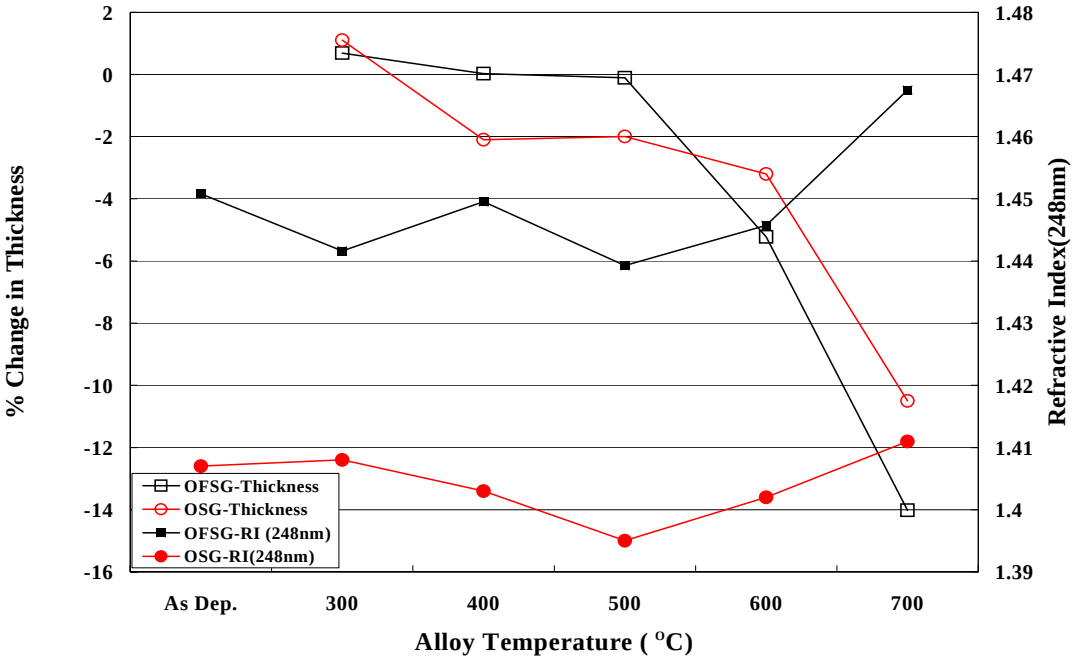


Figure 6-2-4. Effect of different heating test temperature on the change of thickness and RI for OSG and OFSG films

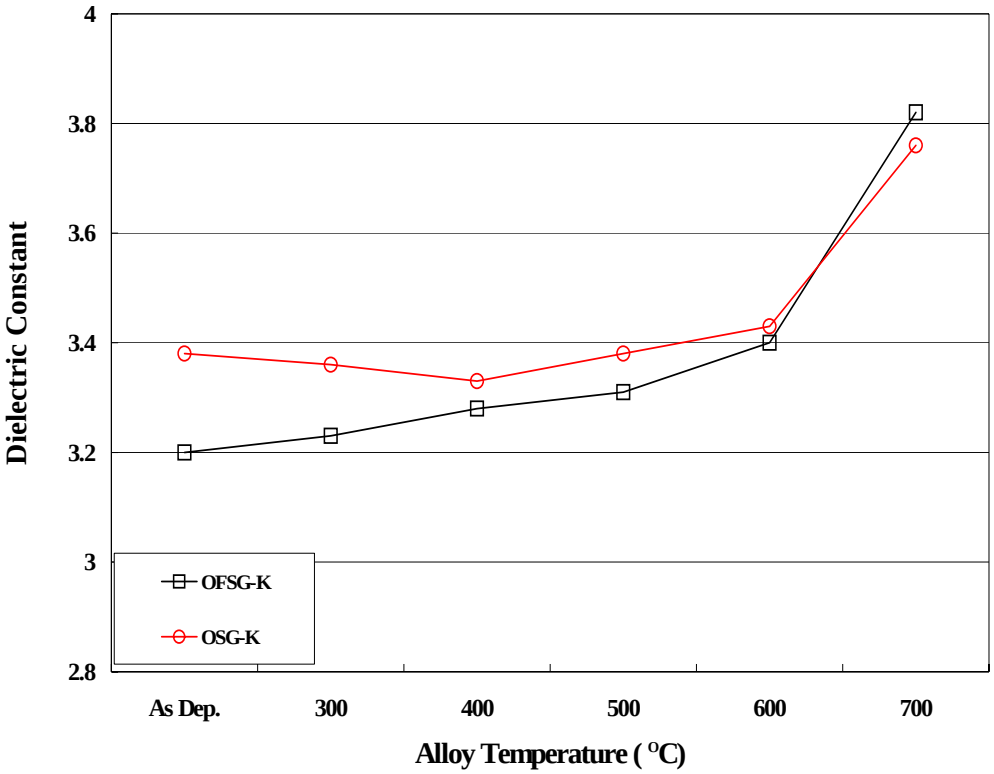


Figure 6-2-5. Effect of different heating test temperature on the change of dielectric constant t for OSG and OFSG films.

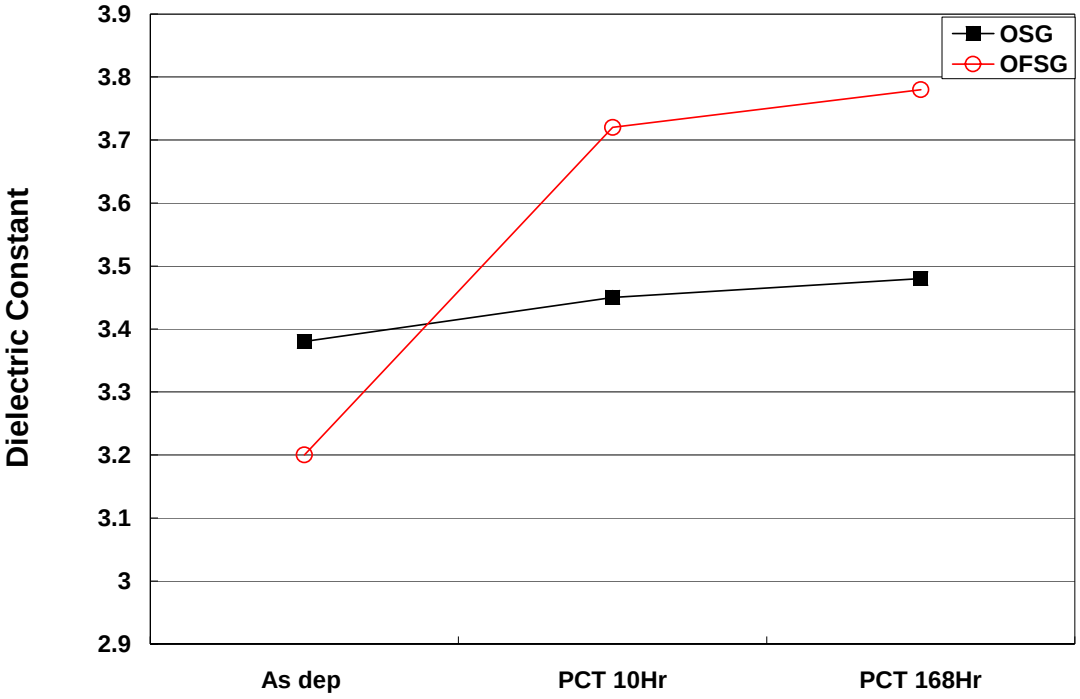


Figure 6-2-6. The Change of dielectric constant of OSG and OFSG films for pressure cooker test.

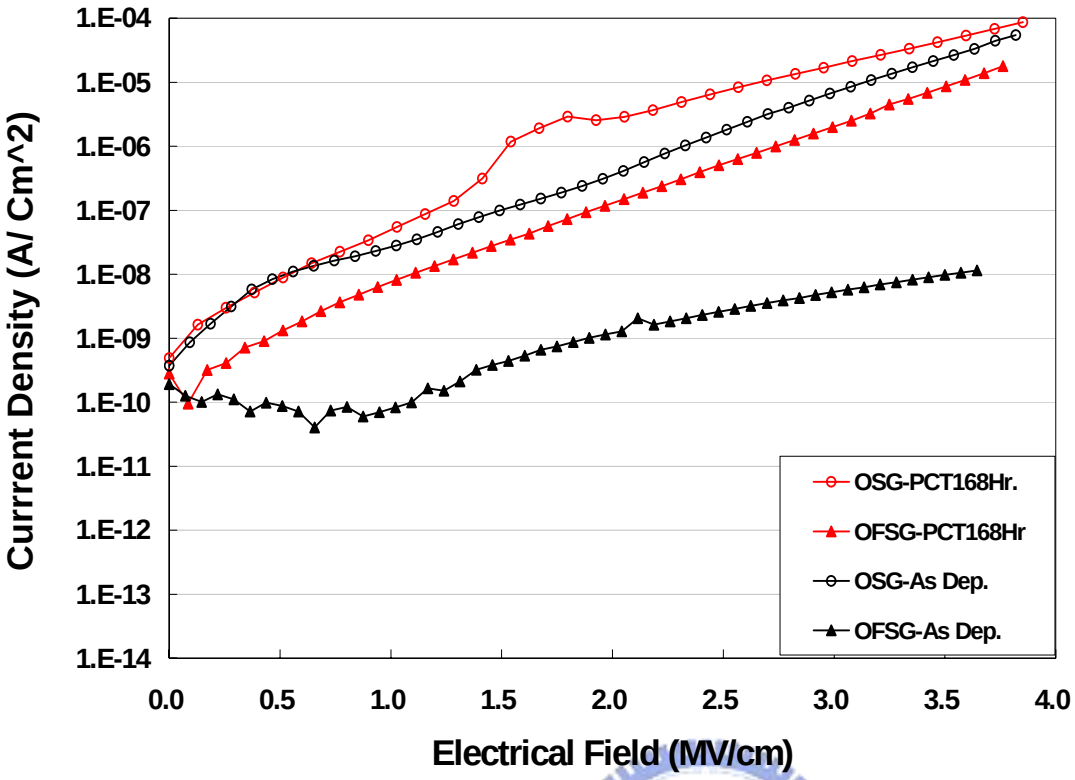


Figure 6-2-7. Effect of PCT test on Leakage current for OSG and OFSG films.

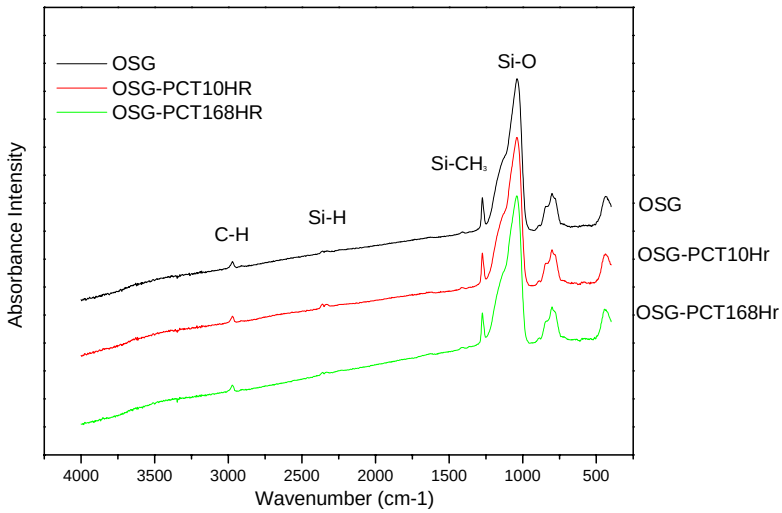


Figure 6-2-8. FTIR Spectrum change of OSG film during PCT test.

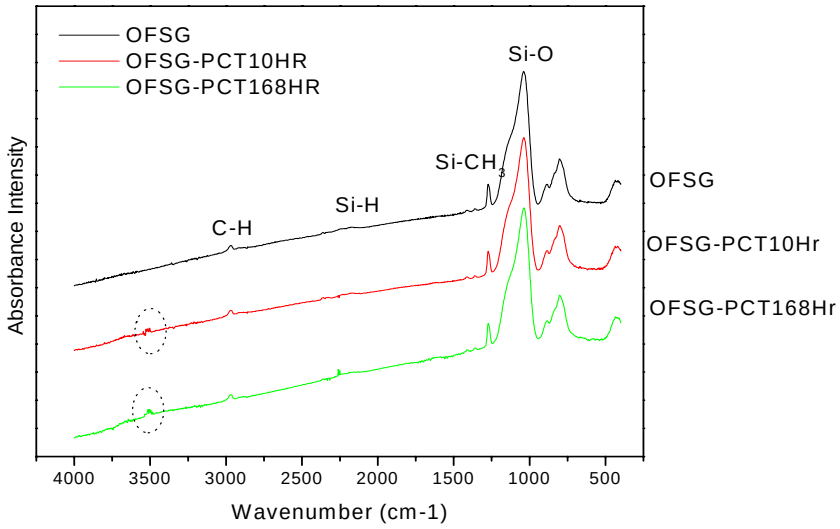


Figure 6-2-9. FTIR Spectrum change of OFSG film during PCT test.

Table 6-3-1. The atomic percentage of element for OFSG flms from XPS Quantification as a function of SiF_4 flow.

SiF_4(sccm)	% Si	% C	% O	% F
0	32.7	31.5	35.8	0
100	32.6	27.1	37	3.3
200	32.9	26.2	36.7	4.2
300	32.8	25.7	36.7	4.8
400	33	25.3	36.5	5.2

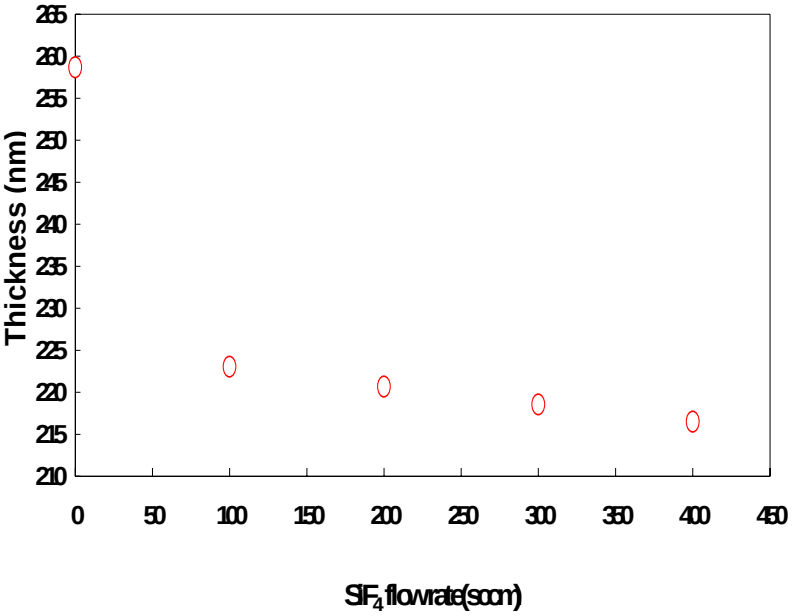


Figure 6-3-1. Deposition rate of OFSG films dependence of SiF_4 flow rate.

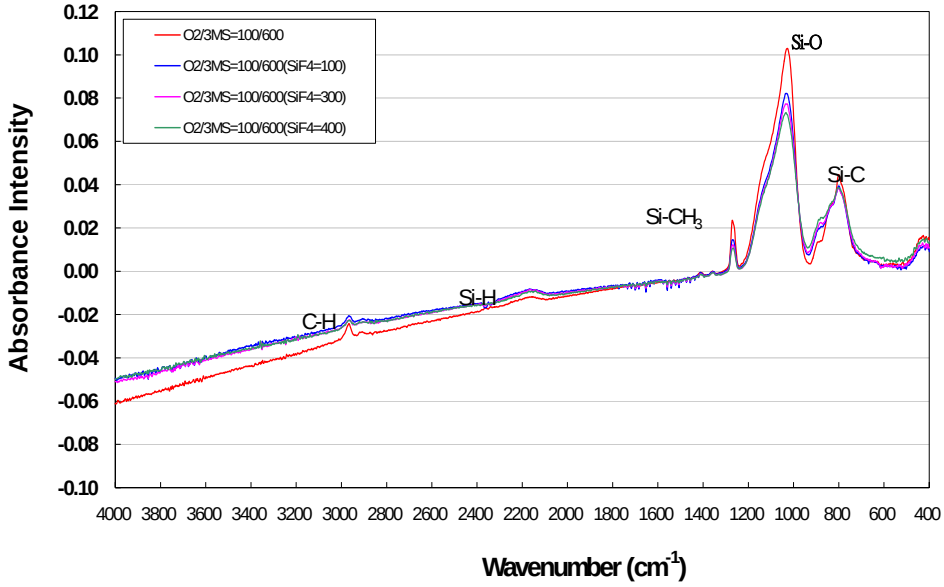


Figure 6-3-2. FTIR spectrum of OFSG films dependence of SiF_4 flow rate.

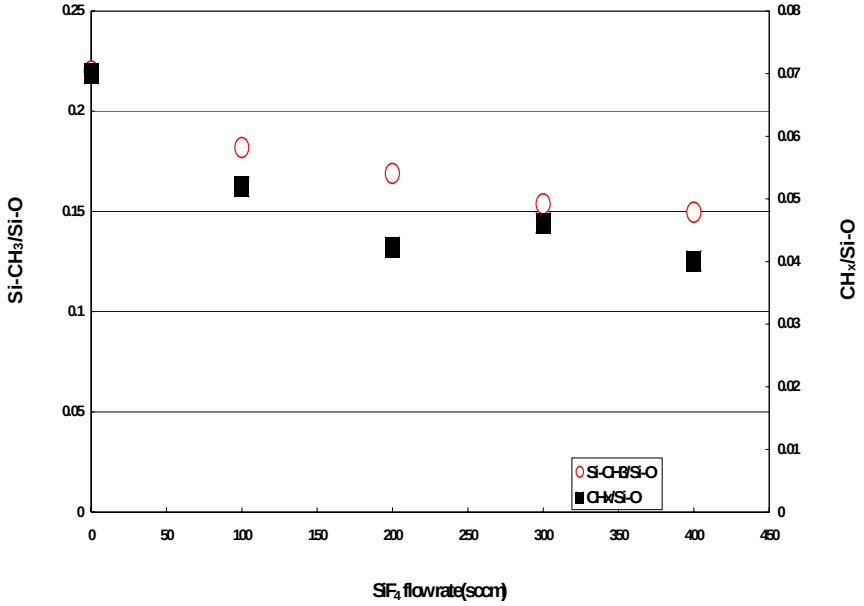


Figure 6-3-3. Si-CH_3/Si-O and C-H_m/Si-O peak ratio in the OFSG films as a function of SiF_4 flow rate.

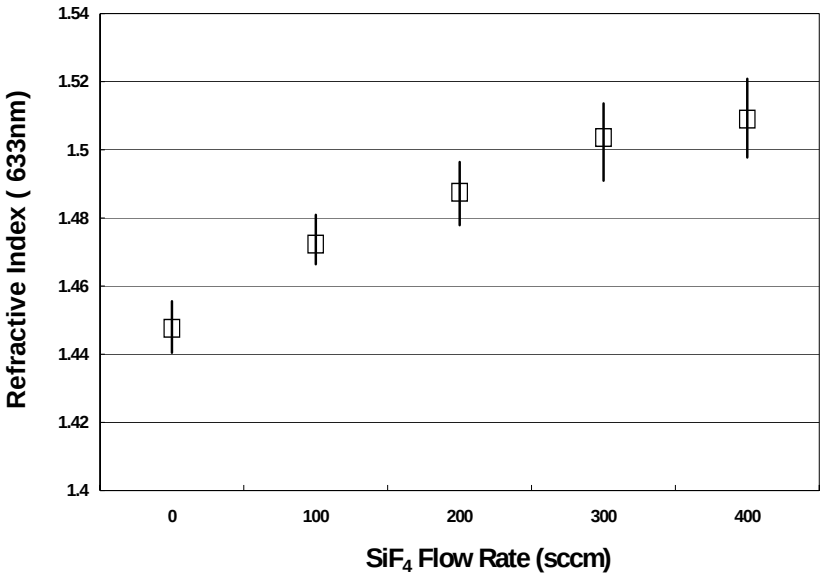


Figure 6-3-4. Refractive index of OFSG films as a function of SiF_4 flow rate.

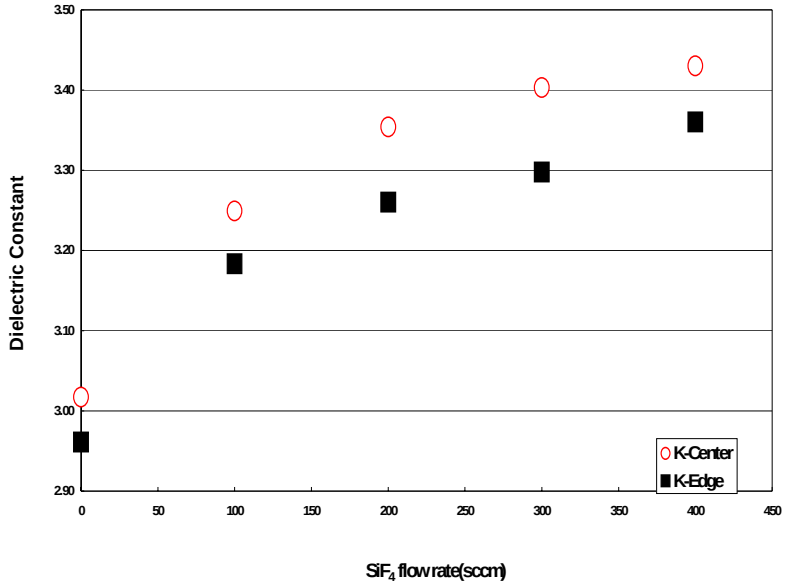


Figure 6-3-5. Dielectric Constant of OFSG films as a function of SiF_4 flow rate.

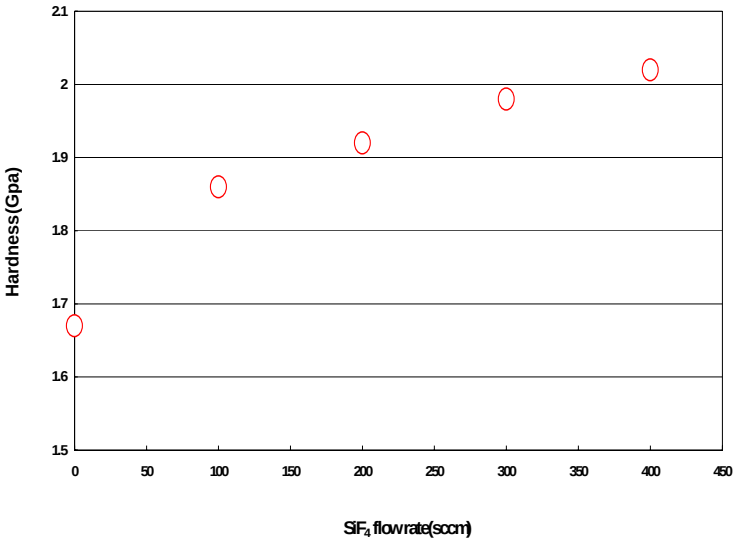


Figure 6-3-6. Hardness of OFSG films as a function of SiF_4 flow rate.

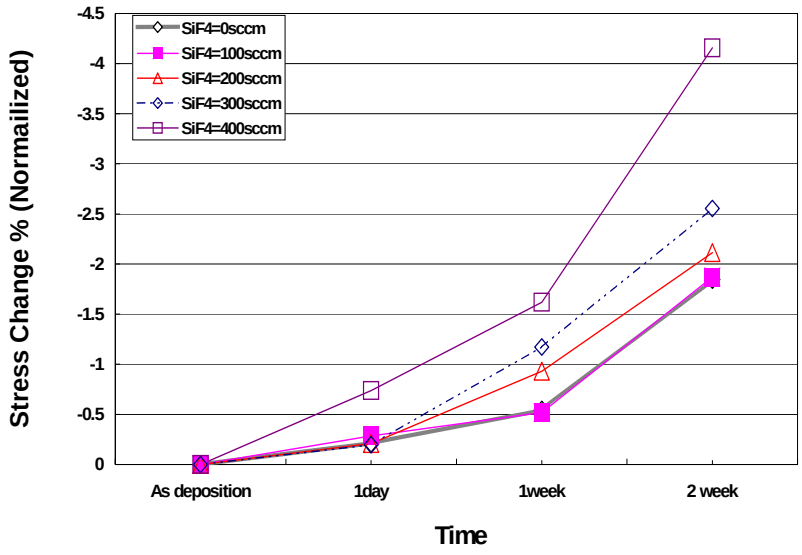


Figure 6-3-7. Normalized stress change of OFSG films with various SiF_4 flow rate as a function of air exposure time.

Chapter 7

Characterization of Copper Barrier Layer

One of the challenging issue facing semiconductor device is how to overcome RC delays in the interconnect layers of both aluminum-based and copper-based devices. To reduce the overall dielectric constant in a copper (Cu) damascene structure, it is crucial to develop a low-*k* barrier/etch stop film that can prevent Cu from interacting with contrasting materials in multilevel interconnect schemes. Additional requirement of a barrier/etch stop layer includes good Cu diffusion barrier properties, good insulating properties, high etch selectivity with respect to the interlayer dielectric, and compatibility with damascene integration. This film also must have good stability under thermal cycles and be extendible to meet the further ULSI production requirements.

Silicon nitride (SiN) has been generally accepted as a first generally generation barrier- not only is it an excellent barrier to Cu, but it also has adequate etch selectivity to oxide for challenging damascene etch steps. However, the *k* value of the SiN is higher than 7.0 and when used conjunction with a low-*k* dielectric, the overall *k* value of the damascene stack is significantly impacted.

Silicon carbide (SiC) is another good candidate for a second-generation barrier/etch stop dielectric in damascene processes. However, carbide films deposited with SiH_4 and CH_4 have a high dielectric constant, high leakage current, and low breakage strength. Furthermore, this carbide film is also difficult to etch.

Another concern is that Cu is easily oxidized even exposed to a low-temperature ambient. In Cu dual damascene fabrication process, subsequent to Cu chemical mechanical planarization of the previous layer, the surface of the Cu will be oxidized, and such oxidation could negatively impact component performance, adhesion ability, and reliability. Hydrogen-based plasma pre-treatment prior to barrier deposition was performed to remove

Cu oxide by the oxidation-reduction reaction.

7-1 The Effect of Copper Barrier Deposition Process on Damascene Copper Interconnect

7-1-1 Motivation

Cu is an increasingly promising material to replace conventional aluminum in deep ultra-large scale integrated circuits since it provides both lower resistivity and higher electromigration over current aluminum alloys [169,170]. However, many process integration issues exist. A major issue is the interaction of Cu with contacting materials in multilevel metallization architecture. Especially, Cu would rapidly drift into silicon-based low-*k* dielectrics during thermal stress, causing the dielectric degradation. Therefore, a barrier dielectric is required in the Cu interconnect to prevent Cu drift/diffusion [171,172]. In the integrated interconnect process for Cu dual-damascene architecture, silicon nitride (SiN) films have been typically used as a barrier dielectric capped on top of a Cu layer, which would efficiently prevent Cu diffusion [173-175]. Apart from the diffusion barrier function, since Cu does not adhere well to the dielectric material, the Cu barrier layer also serves as an adhesion promoter [176,177]. Another concern is that Cu is easily oxidized even when exposed to low-temperature ambient environment. In Cu dual-damascene fabrication process, after completing Cu CMP, the surface of the Cu will be oxidized, and this oxidation can negatively impact on component performance, adhesion ability and reliability [178,179]. NH_3 pre-treatment prior to barrier dielectric deposition was performed to remove Cu oxide (CuO_x) by the following oxidation-reduction reaction:

$NH_3 \rightarrow NH^{2+} + H^-$

$CuO_x + H^- \rightarrow Cu + H_2O$

Furthermore, this oxidation and NH_3 treatment efficiency was dependant upon the waiting time between the Cu CMP process and the barrier dielectric deposition. Time-dependent dielectric breakdown (TDDB) measurement by Noguchi et al. [180] showed that longer waiting times (>5 days) degraded the TDDB lifetime by 9 orders of magnitude.

In Figure 7-1-1, a detailed process sequence from Cu CMP to SiN deposition in the Cu dual-damascene process is shown. Each process step has a significant influence on the interconnect integrated performance. Therefore, the objective of this paper is to clarify the effect of each step in the SiN deposition process on the Cu dual-damascene interconnects.

7-1-2 Experimental Procedures

A film stack of SiN/Cu/TaN/SiO_2/Si (substrate) was prepared for this study, as shown in Figure 7-1-2. The process of the stack film growth is based on Cu dual-damascene technology. First, a 500-nm-thick PE-CVD SiO_2 was deposited on a blanket Si substrate. Next, a 20 nm TaN layer was grown by physical vapor deposition (PVD) to serve as a conductive barrier, followed by PVD Cu used a seed layer. A 1.5-um-thick electroplated (ECP) Cu was subsequently grown. Chemical mechanical polish (CMP) was then performed to remove the top portion (~400-nm-thick) of the ECP Cu layer. Finally, a ~50-nm-thick SiN film was deposited in a PE-CVD deposition system (Centura, Applied Material) using SiH_4 and NH_3 as the reactant gas. SiN films with various concentrations of hydrogen (H) were deposited by controlling SiH_4 flow rate during deposition. Before SiN film deposition, the pre-heat and NH_3 treatment was conducted on the Cu layer in the PE-CVD chamber. Two types of treatment were performed in the study. The first was an in-situ method, where NH_3 plasma treatment and SiN deposition was subsequently conducted in the same chamber without breaking the vacuum. The second type was Ex-situ method, where the NH_3 plasma treatment and SiN deposition were performed in different chambers. The plasma treatment conditions

were the same, with a rf power of 300 W, pressure of 4.2 Torr and the NH_3 gas flow of 80 sccm. These processes were all conducted at 400^oC.

The sheet resistance and reflectance of Cu films were analyzed by Nano-Spec®9100 and a four-point probe, respectively. X-ray photoelectron spectroscopy (XPS) and Rutherford Back Scattering (RBS) was performed to analyze the oxygen concentration on the Cu/SiN surface and the component element of SiN films, respectively. Dynamic Secondary Ion Mass Spectrometry (SIMS) was used to detect the penetration of the Cu ion. Cross-section transmission electron microscopy (TEM) was prepared and imaged in a Philips field-emission microscope.

7-1-3 Results and Discussions

A. Waiting time effect:

To monitor the thickness of the Cu oxide, the spectroscopy reflectometry technique and TEM technique were used simultaneously. As the thickness of Cu oxide increases on the Cu surface, the reflectance of Cu would decrease due to lower reflectance of Cu oxide layer. Therefore, the relation between the change of the reflectance values and the thickness of Cu oxide layer was established. Therefore, the thickness of Cu oxide layer was quickly obtained from the reflectance value. Figure 7-1-3 shows the dependence of the Cu oxide thickness from the TEM measurement along with the normalized reflectance, as a function of the waiting time between the Cu CMP process and the barrier dielectric deposition. Since.

Experiments indicate that the thickness of Cu oxide after the Cu CMP process was about 20~30 A. Moreover, the thickness of Cu oxide increases with increasing the waiting time. However, as the waiting time reached 18 h, the thickness of Cu oxide kept constant, about 45~50 A. To assess the effect of Cu oxide in the Cu interconnects, the tested samples were exposed to E-beam radiation with 10 KV energy. First, the post-Cu CMP wafer was exposed to E-bean radiation, the Cu surface showed no obvious changes observed by SEM. On the other hand, many bubble-like defects were formed on the Cu surface after exposing radiation for the tested sample with a 24 h waiting time, as shown in Figure 7-1-4(a). The bubble-like defects appear on the boundary of the Cu grain, implying that Cu oxide was formed not only on the Cu surface but also on the grain boundary. Surface oxide can be removed by using a hydrogen-plasma treatment described as next paragraph, whereas the oxide on the grain boundary is difficult to remove. Furthermore, it is believed that the Cu oxide of the grain boundary is thicker in the points where grains meet. In order to meet the real manufacture requirement and ensure the better performance, we evaluated some methods to enlarge the waiting time between the Cu CMP process and the barrier dielectric deposition to. Figure 7-1-4(b) illustrates the effect of post Cu CMP clean (citric acid) on the Cu surface with the waiting time up to 24h, where no bubble and delamination occurred on the Cu/SiN surface, implying that post-CMP clean is an effective method to completely remove the Cu oxide on the Cu films.

B. Pre-Heating time Effect:

During the Cu CMP processing, the Cu surface of the interconnects can be severely damaged, resulting in high sheet resistance and poor electromigration endurance. Therefore, prior to the barrier dielectric deposition, thermal time is needed to re-grow the Cu grain and stabilize the Cu resistance. Figure 7-1-5 exhibits the Cu sheet resistance reduction as a function of the pre-heating time. As the pre-heating time reaches 10s, the Cu sheet resistance maintains stable. However, when a Cu sample was exposed too long a pre-heating time (>20s), the top view of the Cu sample undergoing a 20s heating time inspected by SEM revels the formation of hillocks along the grain boundary as shown in Figure 7-1-6. High density of Cu hillock is undesirable because they interfere with defect inspection and might lead to reliability or integration problems. For example, these hillocks would be covered by dielectric in the Cu dual-damascene architecture. In subsequently via definition step the resist over the hillock will be thinner than in other locations. During the etch step, the resist erode quickly, exposing the dielectric to the etch, which may completely remove it. The hillock can possibly short to the next level of the metallization. Furthermore, excessive heating time induces the reliability problem, resulting in a larger variation of via-resistance after 168 h thermal stress. Figure 7-1-7 shows the shift of via-resistance for 4-level Cu metallization after 168 h thermal stressing. As can be seen, the via-resistance of test structure with heating time larger than 20s causes more than 20% shift. Detailed discussion will be conducted on Part C.

C. NH_3 treatment:

Removal of oxide from the Cu surface is considered to be an essential step for Cu dual-damascene interconnects for long-term reliability. NH_3 treatment had been widely used to remove Cu oxide prior to barrier dielectric deposition. Insufficient treatment time induces delamination at the Cu/SiN interface due to poor adhesion of Cu Oxide thin film. X-ray photoelectron Spectroscopy depth profile was used to detect the oxygen concentration on post-Cu CMP Cu surfaces and SiN films for different NH_3 treatment times. For 0, 10, and 20s NH_3 treatment, there is about 9.0 %, 3.8% and ~ 1% oxygen remaining on the Cu/SiN surface, respectively. As a result, ~95% Cu oxide can be removed after 20s NH_3 treatment. Based on this analysis, Figure 7-1-8 shown the oxide removal efficiency as a function of the NH_3 treatment time, along with the comparison of ex-situ NH_3 treatment methods. As shown in Figure 7-1-8, the Cu oxide removal efficiency increases with increasing treatment time and reaches saturation as treatment time rises above 15s, where the removal efficiency can reach as high as 95%. Additionally, the treatment efficiency is independent of the treatment methods. That is, the vacuum-breaking between the NH_3 treatment and SiN film deposition has no significant impact on the Cu oxide removal. However, an interesting finding was found in the via-etch profile. In the case of ex-situ NH_3 treatment, the undercut was observed on the via-bottom (Figure 7-1-9(a)), which may cause a high current leakage and electromigration failure. On the other hand, in-situ NH_3 treatment and SiN deposition

displays no such phenomena (Figure 7-1-9(b)). The root cause was not clarified, but it is presumed that the oxidation reaction occurred in the Cu films during vacuum-breaking process for the ex-situ NH_3 treatment.

Figure 7-1-10 depicts the SIMS depth profile for 0, 10 and 30s treatment when considering the effect of the NH_3 treatment on the Cu diffusion. In zone A, the SIMS profile shows that the Cu level decreased from Cu/SiN interface toward the SiN film, forming a transition region. This is probably due to the rough Cu/SiN surface, since SIMS analysis represents the average atomic concentration. The slightly wider transition region A observed for without treatment case, indicating that no NH_3 treatment had a rougher Cu/SiN surface. On the other hand, no significant difference for various NH_3 treatment times in region A. Since the surface of Cu may result in a high density of dangling bonds due to the damage caused by the Cu CMP process, the fast diffusion path for contaminated ions could be formed in such a damaged surface. It is conceivable that such a damaged surface could be removed and formation of Cu-N bonds. As a result, a higher NH_3 treatment time blocks the Cu ion to drift fusing into the adjacent SiN layer. Furthermore, in zone B of the SiN film, it shows that more Cu ions penetrate into the SiN film when using a lower treatment time and decreases with increasing NH_3 treatment time, indicating that increasing the NH_3 treatment time is an effective way to prevent the Cu ion from diffusing. Therefore, increasing the treatment time is beneficial for minimal oxygen at the Cu/SiN interface and the diffusion capacity based on the

results shown in Fig. 7-1-8 and 7-1-10.

Although further extended NH_3 treatment prior to SiN deposition has advantages for the Cu oxide removal and Cu barrier capacity, too long a treatment time leads to a via-resistance shift as shown in Figure 7-1-7. This shift is mainly attributed to the Cu hump (Figure 7-1-11(b)), which is caused by the Cu stress migration under higher thermal budget conditions. Figure 7-1-11(a) illustrates the formation of the hump mechanism under the higher thermal budget. As a result, precise control of the thermal time is crucial to the Cu barrier film deposition.

D. SiN film deposition:

D-1. Film property:

The basic film properties of the three types of PE-CVD SiN films deposited at 400^{o}C are listed in Table 7-1-1. The low-hydrogen SiN film mainly contributes to the reduction of Si-H bonding (from the FTIR result) by adjusting SiH_4/NH_3 reaction gas ratio. From Table 7-1-1, the electrical characteristics of SiN films are improved by reducing the hydrogen content of the SiN films. The improved electrical features in the SiN films are probability attributed to a low interface trap density and a reduction in the number of carrier trapping sites in the film caused by the presence of less hydrogen.

D-2. Etch Selectivity and Adhesion ability:

The hydrogen content of the SiN film is strongly dependent on the N/Si ratio. A higher

N/Si ratio yields lower hydrogen content in the SiN film. Furthermore, the hydrogen content of the SiN film has been correlated with high etch selectivity and superior adhesion to adjacent low dielectric materials, such as fluorinated oxide (FSG). Figure 7-1-12 depicts the adhesion performance of the various SiN films with FSG film. For hydrogen content above 18%, peeling was observed, as shown in Figure 7-1-12(a). This poor adhesion can be eliminated in the case of SiN films with a hydrogen content below 12%, indicating the importance of controlling the hydrogen content of SiN films in the damascene processing scheme. Poor adhesion arises from the reaction of the extra Si-H bonds in the SiN film and unstable Si-F bonds in FSG films at a higher temperature annealing, following the Eqn. [7-1-1]:

$$\text{Si-H+ Si-F} \rightarrow \text{H-F} \qquad \textbf{[7-1-1]}$$

D-3. Cu Diffusion Barrier ability:

To clarify the Cu barrier ability against the Cu penetration for SiN films, the test wafer of 20-nm-thick TaN/1700-nm-thick Cu/50-nm-thick SiN/Si-substrate structure was prepared. The top layer TaN film was served as a passivation layer to prevent the Cu metal from oxidizing in the subsequent thermal processes. Figure 7-1-13 depicts the Cu depth profiles for the various SiN films after removal of the TaN/Cu electrode, with no apparent difference in the SiN films before the 400^{o}C thermal annealing. However, after performing thermal annealing, the Cu level at the surface of the SiN film with a higher hydrogen content was

about 5 times greater than that at the surface of SiN film with a lower hydrogen content, indicating that more hydrogen contained in the SiN film induces Cu migration during thermal process. A high hydrogen content tends to create a larger number of hydrogen-related defects, such as a Si-H^+-Si hydrogen bridge and Si- dangling bonds, due to Si-H weak bonds (320 KJ/mol). Therefore, the Cu atom may migrate through these hydrogen-related sites.

7-1-4 Summary

This study showed the importance of the Cu barrier dielectric deposition process in a Cu dual-damascene structure. Cu oxide should be completely removed by extending the NH_3 treatment to ensure superior conductivity of the Cu interconnects and to enhance the adhesion of SiN to the post-Cu CMP surface. However, excessive thermal time (pre-heating and treatment time) induces the Cu-hump problem, resulting in a reliability failure. A longer waiting time (>18hr) leads to delamination at the SiN/Cu surface, even after performing the NH_3 treatment. The post Cu-CMP clean seemed to effectively solve this issue, but increased the process complexity. Therefore, optimization of the process time prior to the Cu barrier layer deposition process is crucial for ensuring the performance of the Cu interconnects. In addition, SiN film with lower hydrogen content has a superior etch selectivity and a better electrical performance. As a result, SiN films with less than 10% hydrogen are suitable for use as a Cu-barrier layer and an etch-stop layer in the Cu dual-damascene structure.

7-2 Film Properties of Copper Barrier Films with Different Deposition Temperature

7-2-1 Motivation

Cu is a promising material to replace aluminum (Al) in ultra-large scale integrated (ULSI) conductors due to its low electrical and high electromigration immunity [167,168]. However, because it is easily diffused into adjacent low-*k* dielectrics by heating treatment or under an electric field and easily oxidized at room temperature (<200^{o}C), the insertion of a barrier dielectric between the low-*k* film and the Cu interconnect as a diffusion and oxidation layer is necessary [176].

An optimized Cu barrier layer as an application in the Cu dual-damascene process must meet important requirements. There are: (1) high barrier properties; (2) low dielectric constant for small parasitic capacitance; (3) high etching durability under interlayer dielectric (ILD) in the dual damascene process; (4) improved adhesion ability between the Cu and the ILD film; (5) better thermal and chemical stability, and (6) a processing temperature limitation of less than 450^{o}C [169,170].

For the past several years, SiN films deposited by PE-CVD technology have been widely used as a Cu barrier and etching stop layer in a dual damascene architecture. However, as minimum device features shrink below 180 nm, the increase in propagation delay, crosstalk notice and power dissipation of the interconnect, has become limiting factors in ULSI device performance due to the high dielectric constant (*k*=7.0) of SiN film [169,174]. As a result, an alternative barrier layer with a low dielectric constant is needed to further reduce the RC delay. Recently, a promising low-*k* barrier film, carbon-doped silicon film (*k*<5), deposited by PE-CVD method is a strong candidate owing to the lower electronegativity of the carbon atom. Previous research has investigated both silicon-carbonitride (SiCN) and silicon oxycarbide (SiOC), and has indicated that

nitrogen-doping silicon carbide (SiCN) film has a *k* value in the range of 4.2-4.9, excellent barrier ability to Cu, and adequate etch selectivity to oxide for challenging damascene steps, and oxygen-doping silicon carbide (SiOC) film exhibited further lower *k* values, reaching 3.5-4.2, and has a higher breakdown voltage [177,179,189]. On the other hand, very few papers have reported the effect the deposition temperature on the Cu barrier films, when considering the above requirements. It is widely known that the quality of a PE-CVD film is largely influenced by the deposition temperature. The films deposited using PE-CVD method with higher deposition temperatures have better chemical and electrical properties. In Contrast, higher temperature deposition induces metal diffusion into its adjacent layers. Consequently, the optimum deposition temperature is an important factor during the application of the Cu barrier layer.

This work reported the deposition characteristics of 3MS-based barrier layers, the film composition and properties, and its integration with Cu and ILD, as a function of the deposition temperature dependence. A comparison to the characteristics of conventional PE-CVD SiN film is made and the differences are then discussed.

7-2-2 Experimental Procedures

Deposition was performed on an Applied Materials Producer system with a 200 mm Producer chamber. Thin film was deposited on *p*-type (100) 0.01~0.02 ohm-cm 8-inch silicon (Si) substrates using a radio frequency (13.56 MHz) PE-CVD with a deposition temperature varying from 150 to 450^{o}C. Three kinds of barrier films were deposited, including SiN, SiCN and SiOC. The optimized deposition process conditions are listed in Table 7-2-1.

The film thickness and refractive index were analyzed by reflectometer and/or ellipsometer Nano-Spec®9100, using light of 633 nm wavelength. The values were measured

before and after annealing at 400°C for 2 h in N_2 ambient and O_2 ashing process. The chemical bonding and composition of the film were investigated using Fourier transform infrared spectroscopy (FT-IR) [Bio-Rad Win-IR PRO], X-ray photoelectron spectroscopy (XPS) and Rutherford Back Scattering (RBS), respectively, using 300-nm-thick films. The dielectric constant (*k*) and leakage current were measured by current-voltage (I-V) and capacitance-voltage (C-V) methods (Solid State measurement, 495 CV system), using 500-nm-thick films. The k value was obtained at 1 MHz.

7-2-3 Results and Discussions

Barrier film Deposition characteristics **-** The temperature dependence of the deposition rate of both 3MS-based barrier films and conventional PE-CVD SiN is shown in Figure 7-2-1. In contrast to PE-CVD SiN films, 3MS-based barrier layers, including SiCN and SiOC films, showed a negative temperature dependence deposition rate. The deposition rate decreases with an increasing deposition temperature. Moreover, 3MS-based processes show a very strong surface temperature effect. This indicates that 3MS-based processes could be possibly controlled by a surface reaction step, which may explain the surface sensitivity of this process due to the participation of the surface atoms. The negative temperature dependence suggests the dominance of the surface adsorption. The apparent activation energy values for the SiCN and SiOC processes are 0.53 and 0.60 eV, respectively. As a result, SiCN deposition process shows the higher deposition rate compared to SiOC process due to its lower activation energy. On the other hand, the deposition rate of the PE-CVD SiN film was typically between

240-320 nm/min, showing that it is relatively insensitive to the deposition temperature. When the deposition temperature was raised from 150 to 450^{o}C, the deposition rate increased by 30%. The data exhibits a positive temperature dependence on the deposition rate, which is controlled by the gas phase diffusion. A higher deposition temperature increases the diffusion rate of the reactant gas in the gas phase and slightly increases the deposition rate.

As shown in Figure 7-2-2, the refractive index became smaller with decreasing deposition temperature for all barrier films. This decreasing dependency is assumed to be caused mainly by the change of the deposited films. Therefore, a higher deposition temperature process results in a higher film density.

Figure 7-2-3 shows the deposition temperature dependence of the dielectric constant, which was determined by using conventional electrical capacitance-voltage measurement method. As can be seen, a slight increase in the dielectric constant of the PE-CVD SiN film, from 6.7 at 200^{o}C to 7.3 at 450^{o}C, indicates a smaller temperature dependence. For 3MS-based barrier films, the dielectric constant also increased with the decreasing deposition temperature, but the deposition temperature strongly influences the dielectric constant. Taking SiCN films as example, the dielectric constant can drastically rise to as high as 7.0 at 450^{o}C from 3.8 at 200^{o}C. In addition, SiCO films show the lowest dielectric constant among the three barrier films at the same deposition temperature. The lower dielectric constant is ascribed to the Si-O bonding, replacing the Si-N bonding. Furthermore, we divided the dielectric constant at 1 MHz into three main items, electronic (k_e), ionic (k_{ion}) and orientational polarizations (k_{ori}), as shown in the following equation [7-2-1]:

$$\text{Dielectric constant (1 MHz)} = k_e + k_{ion} + k_{ori} \qquad \textbf{[7-2-1]}$$

Electronic polarization is the square of the refractive index (n) at 633 nm wavelength.

Figure 7-2-4 compares the difference between electronic polarization and other polarization with varying deposition temperatures for the three kinds of barrier films. The ionic (k_{ion}) and orientational polarizations (k_{ori}) slightly increase with increasing deposition temperature for all barrier films. On the other hand, the electrical polarization (k_e) shows a strong increment with rising deposition temperature for 3MS-based barrier films. In contrast, PE-CVD SiN film shows a weak dependence on the deposition temperature. Additionally, SiCO films exhibit the lowest dielectric constant among the three barrier films, mainly caused by the reduction of electronic contribution attributed to the Si-O bonds. When compared with nitrogen and carbon, the oxygen atom has a higher electronegativity, which decreases the polarizability of the bonds and leads to a lower *k* value. It deserves to be mentioned that the electrical polarization (k_e) values of SiCN films is lower than that of PE-CVD SiN films and gets beyond as the deposition temperature is above 350^{o}C. The possible cause of this can be attributed to the fact that SiCN film has more Si-N bonds and its film structure is close to the SiN films as a higher deposition temperature.

The film stress was measured using a flatness tester, which detects the curvature of the substrate. Film stresses of less than $5x10^{9}$ dyne/cm^{2} is acceptable for ULSI circuit applications, as too large a stress causes adhesion failure on adjacent layers. As shown in Figure 7-2-5, 3MS-based barrier films show a compressive stress throughout the entire range of deposition temperatures from 150 to 450^{o}C. A decrease in deposition temperature caused the stress to become lower. It is speculated that the higher incorporated hydrogen content in barrier films with a lower deposition temperature is a factor in relieving stress. Furthermore, SiOC films display a weak dependence on the deposition temperature with stress levels showing a saturation value of about $1.52x10^{9}$ dyne/cm^{2} at 350^{o}C. On the other hand, SiCN films exhibit a higher compressive stress, and the value is greater than $5x10^{9}$ dyne/cm^{2} at 450^{o}C deposition temperature. At a 350 ^{o}C deposition temperature, the stress of SiCN films is

$2.80x10^9$ dyne/cm^2, which is 1.8 times larger than that of SiCO films. The difference arises from the thermal expansion coefficient of the CH_3-Si-O and CH_3-Si-N bonding structure in SiCN and SiCO film, respectively. Different from 3MS-based barrier film, the stress of the PE-CVD SiN film shows a $4.64x10^8$ dyne/cm^2 compressive stress at a deposition temperature of 150°C. As the deposition temperature increases, the stress transforms to tensile stress and becomes larger until the temperature reached 300°C, showing a maximum tensile stress of about $9.0x10^8$ dyne/cm^2. The stress then decreased and reverted back to compressive stress at 400°C. The higher tensile stress arises from the thermal energy, required for the thermal relaxation of the deposited atoms, which results in an enlargement of the atomic distance with tensile restoring force. Higher compressive stress in PE-CVD SiN film above 400°C is attributed to Si-N network with a lower hydrogen content.

Chemical and physical properties of barrier film - The nature of the chemical bonding groups in the barrier dielectrics was analyzed by FTIR spectroscopy. Figure 7-2-6 shows the FTIR spectra of PE-CVD SiN, SiCN and SiCO films deposited at 200°C. As shown, all three films have common infrared absorbance peaks in 2200 cm^{-1}, attributed to Si-H stretching bonds. For PE-CVD SiN film, there is a unique peak in 3300 cm^{-1}, attributed to N-H stretching bonds. 3MS-based barrier films show two peaks in 1270 cm^{-1} and 2800 cm^{-1} related to the Si-CH_3 and CH_n vibration bonds, respectively, contributing to a lower dielectric constant. In the 800-1200 cm^{-1} wavelength range, the infrared absorbance was the main backbone of the film and showed a distinct difference between the three barrier films. The main backbone of PE-CVD SiN film is the Si-N bonds, corresponding to 820 cm^{-1}. For 3MS-based barrier film, the main mainstay is Si-C bonds, corresponding to 780 cm^{-1}.

Additionally, there are other extra bonds on 820 cm^{-1} (Si-N bonds) and 1010 cm^{-1} (Si-O bonds) for SiCN and SiCO films, respectively. As the deposition temperature rises, the hydrogen-related bonds including Si-H, CH_n and N-H bonds decline, showing that these films contain a lower hydrogen content, which improves the film's hardness and etch selectivity [170, 186]. Additionally, it is easy to see that the Si-CH_3 peak will gradually disappear with an increase in deposition temperature. As a result, the dielectric constant increases, and in this regard SiCN film is similar to SiN film.

Furthermore, the barrier films composition was analyzed using an XPS and RBS to investigate the effect of the deposition temperature. The relationship between the composition and the deposition temperature is exhibited in Table 7-2-2. Although XPS analysis cannot detect the hydrogen content, the trend of the other components as a function of the deposition temperature is the same as the results of the RBS analyses. For PE-CVD SiN films, the hydrogen content decreases with increasing the deposition temperature, which agrees with the FTIR result, and the Si/N ratio increasingly approaches 3/4, the perfect stoichiometry for SiN films. In 3Ms-based barrier films, the hydrogen content also declines with an increase in deposition temperature, similar to PE-CVD SiN film. Additionally, the carbon content decreases, whereas the nitrogen content for SiCN films, and oxygen content for SiCO films, increases as the deposition temperature is increased. That is, at a higher deposition temperature (>400^oC), the as-deposited SiCN and SiCO films are close to SiN and SiO,

respectively. As a result, the decreases of hydrogen and carbon contents, and the increases of nitrogen and oxygen contents in barrier films, cause an increase in the film density and an increase in the refractive index. Moreover, at the same deposition temperature, SiCN films show the highest hydrogen content compared to other two barrier films since there is more hydrogen source in the reactant gas during the SiCN barrier deposition, including both 3MS and NH_3 gas. Additionally, SiCN and SiCO films indicate that the H/C ratios are about 2.0 and 1.22, respectively, from the results of RBS analyses. This implies that all carbon atoms are not exactly bonded with the hydrogen atoms (Si-CH_3), and may also produce Si-C-Si or Si-C-O- bonds.

Film properties for the VLSI device fabrication process - In the Cu dual-damascene structure, the barrier dielectrics not only possess Cu diffusion-barrier properties, but also serve a function of etching stopping layer. To avoid resulting in the corrosion of the under-layer Cu, the barrier dielectrics with a excellent etch stop performance are favorable. The better etching stopping for the barrier dielectrics represents a higher etching selectivity relative to the low-*k* dielectrics. Figure 7-2-7 shows the etching rate of various barrier films as a function of the deposition temperatures. The durability under a reactive ion etching (RIE) process was measured under organo-silicate glass (OSG) etching conditions, using $C_5F_8/N_2/Ar$ gas. The etching rate of all barrier films in this study shows a slight increase as the deposition temperature is decreased to 300^oC from 450^oC and a significant increase with

decreasing the deposition temperature to 200°C. Additionally, at the deposition temperatures are below 300°C, the etching rates of the PE-CVD SiN and SiCN films are larger than that of SiOC films. On the other hand, as the deposition temperature is increased to 400°C, the PE-CVD SiN film has the lowest etching rate, whereas the SiOC film has the largest etching rate. It is speculated that PE-CVD SiN and SiCN films deposited at a lower deposition temperature contain more hydrogen content and N-H bonds are easily broken. However, as the deposition temperature is increased up to 400°C, the hydrogen content significantly decreases and the film density increases in the PE-CVD SiN and SiCN films. Compared to Si-N bonds, Si-O bonds in the SiCO films are easy to etch under the same etching condition. Therefore, SiOC film has a higher etching rate as the deposition temperature is increased to 400°C. Taking the case of 350°C deposition temperature as an example, the values of the etching selectivity relative to OSG film are approximately 6.03, 6.84 and 6.25 for PE-CVD SiN, SiCN and SiCO films, respectively. This etching selectivity shows a suitable durability level and indicates that the barrier films can function as an etching stopping layer for the deposition temperatures above 350°C .

Thermal and chemical stability - In the integration fabrication, there are at least 7-8 layers of interconnect dielectric deposition and the deposition temperature is about 400°C. Therefore, the barrier layer should have sufficient heat resistance against the thermal process. The result of seven heating test cycles in a 425°C N_2 ambient environment for 1 h is

illustrated in Figure 7-2-8. It shows that the as-deposited barrier films deposited at higher deposition temperatures have a better thermal resistance. Furthermore, PE-CVD SiN films have superior thermal stability for all deposition temperature ranges in this study. On the other hand, the deposition temperature of SiCN and SiCO films must be above 300 ^{o}C and 350^{o}C, respectively, where the change of the film properties is less than 5%. Therefore, as can been observed from Figure 7-2-9, Si-N bonds have the strongest bonding strength against thermal treatment compared to Si-C and Si-O bonds. Lower deposition temperatures cannot generate enough bonding energy to form Si-C and Si-O bonds. SiCO films were formed by dissociating the CO_2 and forming Si-O bonds. The dissociation energy of C-O bonds and the bonding energy of Si-O bonds are 357.7 KJ/mole and 452 KJ/mole, respectively, which is higher than the N-H dissociation energy (<339 KJ/mole) and the bonding energy of Si-C bonds (318 KJ/mole). As a result, as the deposition temperature falls below 300^{o}C, SiCO films easily degrade under thermal treatment due to an insufficient energy supply for producing robust bonds. Furthermore, the effect of photoresist stripping on the barrier dielectrics is an essential factor when applying the barrier film to the Cu dual-damascene structure since the photoresist stripping is an indispensable step and may degrade the under-layer barrier film. In conventional photoresist stripping step processes, O_2 plasma ashing is commonly implemented because of its superior efficiency in removing polymer. The change of barrier film thickness and refractive index by O_2 ashing is shown in Figure

7-2-9. Among the three barrier films in this study, SiCO films have the worst chemical resistance. However, the deposition temperature is strongly related to the chemical resistance for SiCO films. SiCO films with a higher deposition temperature would enhance their chemical resistance. The deposition temperature of SiCN films must be at least 300 ^{o}C to obtain < 3% change in film properties after the O_2 ashing process. In addition, PE-CVD SiN films remain stable for all deposition temperatures ranging from 200 to 450^{o}C. A possible explanation for this degradation in 3MS-based barrier dielectrics is that the -Si-CH_3 bond has less O_2 chemical resistance, and may undergo the following reaction:

$$Si\text{-}CH_3 + O \rightarrow Si\text{-}OH \text{ or } Si\text{-}O \qquad \textbf{[7-2-2]}$$

However, when the deposition temperature is increased (>350^{o}C), 3MS-based barrier dielectrics (SiCN and SiCO films) contains less Si-CH_3 bonds.

Barrier properties of the barrier layer to Cu thermal diffusion **-** The barrier property of the three barrier dielectrics in this study as a function of the deposition temperature was investigated. It is known that the film with superior barrier ability against Cu thermal diffusion has a correlation to TDDB property under a Cu electrode. The Cu diffusion in the barrier dielectrics was measured by Secondary Ion Mass Spectrometry (SIMS) analysis. Figure 7-2-10 shows the Cu diffusion depth profiles in the SiCO films with the deposition temperatures of 200^{o}C and 400^{o}C, respectively. A TaN layer was deposition between the Cu film and the silicon substrate. A Cu layer was deposited using electroplating. A ~50-nm-thick

SiCO film was deposited, and was subsequently capped by an approximately 100-nm-thick organo-silicate glass (OSG) was capped subsequently. As shown in Figure 7-2-10, the Cu profile transition of the barrier film deposited at a higher temperature is slightly sharper than that deposited at a lower temperature. That is, the diffusivity of the Cu atom was blocked by the SiCO films at higher deposition temperatures. Figure 7-2-10 also reveals a higher Cu level near the SiCO/Cu interface at 200^{o}C deposition temperature than at 400^{o}C. The same phenomenon was also observed for SiCN and PE-CVD SiN films. To compare the Cu barrier capacitance of barrier dielectrics, the Cu diffusion depth is defined as the subtraction of the depths at which Cu concentrations reduce 3-order magnitude from the Cu/dielectric interfacial region. Figure 7-2-11 summarizes the Cu diffusion depth of the various barrier dielectrics as a function of the deposition temperature. The result shows that the barrier films deposited at higher deposition temperatures in this study have a better Cu diffusion-barrier ability. In the diffusion mechanism of Cu into the barrier layers, two main factors affect the Cu diffusion depth, one being the thermal budget, and the other being the quality of the barrier film. At higher temperatures, Cu tends to accelerate its diffusion velocity and has a boarder Cu transition profile. Barrier dielectrics with a poor film quality have insufficient diffusion capacitance against Cu drift into an adjacent layer. The results shown in Figure 7-2-11 suggest that the diffusion velocity of Cu is not as important for barrier films deposited on a Cu layer. The smaller diffusion depth at higher deposition temperatures is assumed to be

the dominant factor in producing a better quality of the barrier films. In comparing the barrier films deposited using various precursors, PE-CVD SiN film prepared using SiH_4 show the best barrier performance, and a reduced temperature dependence, indicating that PE-SiN film deposited at temperatures ranging from 150 to 450^{o}C is desirable for meeting the Cu-barrier film requirements. On the other hand, the Cu diffusion depth of the 3MS-based barrier film increased strongly with decreasing deposition temperature. The Cu diffusion depth of SiCO films is slightly larger than that of SiCN film. A higher Cu drift in 3MS-based barrier film when compared to PE-SiN films may due to the lower film density as the CH_3 group is incorporated into the deposited film. The degradation in the diffusion barrier performance of SiCO film is due to the extra microporous Si-O-Si cage structure in SiOC film.

7-2-4 Summary

PE-CVD SiN and 3MS-based SiCN and SiOC films deposited by PE-CVD have been comprehensively investigated at various deposition temperatures. The essential requirements for the Cu barrier dielectrics were adequately considered in terms of these three films. Of all barrier dielectrics, PE-CVD SiN films with various deposition temperatures (200-450^{o}C) were the most suitable option as a Cu barrier layer film since it possesses higher barrier properties and integration capacitance. However, a lethality attached to this film is a higher dielectric constant, as high as 7.0 in the 200-450^{o}C deposition temperature ranges. Therefore, a great deal of effort needs to given to lowering permittivity for the reduction of the parasitic capacitance. On the other hand, 3MS-based barrier dielectrics, including SiCN and SiCO films, can reduce the dielectric constant to 3~5, depending on the deposition temperature.

Although the barrier dielectrics produced at lower deposition temperatures can further reduce the dielectric constant, they suffer from the predicament of the thermal and chemical stability. As a result, the deposition temperature of the film must be greater than 350^{o}C to improve the film properties and be suitable as a Cu barrier layer.

7-3 Plasma Pre-Treatment Effect on Cu Metallization

7-3-1 Motivation

As the size of device features continues to shrink, resistor-capacitance (RC) delay of the interconnect plays an increasingly important role in determining the integrated-circuit performance. Cu has been considered a promising interconnect metallization materials for deep submicron technology, due to its lower resistivity and higher electromigration resistance [176,190]. However, it was reported that Cu diffuses rapidly into SiO_2 films. Cu impurity in SiO_2 may cause the failure of the time-dependent dielectric breakdown. As a result, a diffusion barrier is required in Cu metallization systems to prevent Cu from entering the interlevel dielectrics [168,169,191].

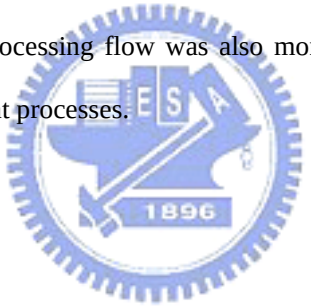
In a Cu and low-k dielectric dual damascene architecture, silicon nitride or silicon carbide can b applied as an etch and CMP stop layer, and as a Cu diffusion /oxidation barrier [192,193]. However, a resulting concern is that Cu can be easily oxidized even at low temperature (<200^{o}C). The forming oxidation could negatively affect the dice electrical and

reliability performance [194,195]. Therefore, prior to barrier layer deposition, a chemical treatment reaction to remove copper oxide is needed, which improves the adhesion ability between the Cu and the barrier layer. NH_3 and H_2 plasma treatments were applied to the current copper process as both generate H species, which can remove copper oxide (CuO_x) from the Cu surface using the following oxidation-reduction reaction:

$$Cu_xO + H \rightarrow \quad Cu + H_2O_{(g)}$$

Where H_2O vaporizes as the chemical reaction proceeds at elevated temperatures [196].

In this report, both NH_3 and H_2 plasma pre-treatment processes, performed by Plasma-Enhanced Chemical Vapor Deposition (PE-CVD) before Cu barrier film deposition, were investigated. The investigation check items included Cu_xO removal efficiency, adhesion ability and the impact on ILD (inter-layer dielectric) film. In addition, the electrical result on pattern wafers with a dual damascene processing flow was also monitored to compare the difference between these two pre-treatment processes.



7-3-2 Experimental Procedures

Control wafer- Based on the Cu dual-damascene process flow, a film stack of SiN (or SiC)/Cu/TaN/SiO_2/Si (substrate) was prepared for this study. First, a 500nm thick PE-CVD SiO_2 film was deposited on a blanket Si substrate. A 30nm TaN layer was then grown by physical vapor deposition to improve the adhesion between the Cu layer and the SiO_2 layer. Next, a 160nm PVD Cu layer used as a seed layer for the subsequent deposition of a ~ 1.3um thick electroplated (ECP) Cu films was grown. Chemical mechanical polishing (CMP) was then performed to remove the top portion (~400nm) of the ECP Cu layer, followed by the citric acid clean to remove the backside Cu contamination. Finally, ~ 50nm barrier layer (SiN

or SiC) was deposited in a PE-CVD DxZ system. Before barrier film deposition, two kinds of pre-treatment, NH_3 and H_2, were conducted in the same chamber to investigate the difference between two treatment conditions. The detailed treatment process conditions are listed in Table 7-3-1.

The Cu_xO removal efficiency test was performed using two methods. The first method used Nano 9100 to measure the Cu Reflectance compared to silicon. The post-clean wafer was performed using an O_2 treatment to form Cu_xO layer. The different pre-treatments were then performed to evaluate the change of the Cu Reflectance**.** The second method used Auger analysis to check the oxygen concentrations between the Cu and the barrier layer.

The adhesion ability was measured by Stud-pull method. The Cu control wafer was under NH_3/H_2 treatment and followed by barrier layer deposition.

Pattern wafer- A diagram of the metal and dielectric layer structure is shown in Figure 7-3-1. After removing Cu layer using Cu-CMP, the dielectric stack for the adjacent layer pre-treatment and deposition subsequently performed. This was followed by the dual-damascene dielectric stack, photo, etch and Cu processing to complete the next inter-dielectric layer. At this point, the wafers were inspected for bubble defects using optical microscopy (OM), as well as scanning electron microscopy (SEM), to check for adhesion failure mode. The metal test structures were also tested for leakage current and Cu-line resistance.

7-3-3 Results and Discussions

The treatment efficiency was determined from the Cu reflectance at a 480nm wavelength. The change of the Cu reflectance percentage (R%) was calculated using the

following equation:

$$R\% = (Cu_{Ri} - Cu_{RO})/Cu_{RCMP}$$

Where Cu_{Ri}, Cu_{RO}, and Cu_{RCMP} represent the Cu reflectance after post treatment, the Cu reflectance after post O_2 treatment, and the Cu reflectance after post Cu-CMP, respectively.

A larger change of the Cu reflectance percentage means a higher treatment efficiency when removing Cu_xO. Figure 7-3-2 compares the effectiveness of the H_2 and NH_3 treatments, indicating that at the beginning 20 seconds pre-treatment, H_2 treatment has a higher Cu_xO removal ability than that of the NH_3 treatment. In addition, the NH_3 treatment efficiency improves as the treatment times increases to 30 seconds, showing a maximum treatment ability comparable to H_2 treatment. The effectiveness then decreases after 40 seconds of treatment time. The decline may be as a result of Cu-N bonding formed at NH_3 plasma environment. X-ray Spectrum (XPS) analysis also demonstrates this hypothesis shown in Figure 7-3-3, implying that there is Cu-N bonding for the NH_3 treatment, while no Cu-N bonding was detected for the H_2 treatment.

Auger analysis was used to check oxygen concentration at the interface between the barrier layer and the Cu surface, shown in Figure 7-3-4. Based on the result of Figure 7-3-4, the oxygen concentration dependence of treatment time is exhibited in Figure 7-3-5. Oxygen concentration decreased with increasing treatment times and reached maximum value at 20 seconds and 30 seconds for the H_2 and NH_3 treatment, respectively. Furthermore, from the

results shown in Figure 7-3-4, the Cu diffusion depth into the barrier layer was comparable, despite the different pre-treatment methods. That is, the Cu barrier effect is attributed to the barrier layer characteristics, independent of the pre-treatment type.

In order to evaluate the adhesion between the Cu surface and the barrier layer under different pre-treatment conditions, we inspected multiple wafers that were processed actual dual damascene flows by OM. Figure 7-3-6 displays a strong correlation between the barrier layer pre-treatment conditions and the appearance of the bubble defect. It is obviously seen from the results that 5-second NH_3 pre-treatment is correlated with a significant density of bubble defect density, and 10-second NH_3 pre-treatment can reduce the occurrence probability to ~ 38%, which is still the margin for Cu_xO removal. On the other hand, the extended NH_3 pre-treatment, as well as the H_2 plasma treatment, largely decreases the bubble defect occurrence probability. This trend with plasma pre-treatment time is consistent with the hypothesis that a certain minimum pre-treatment is needed to fully remove the oxide from the Cu surface along with other possibly residual material. The bubble defect was examined with a focused ion beam (FIB) SEM to determine at which interface the delamination occurred. Figure 7-3-7 strongly indicates that the SiN/Cu interface was the failure point.

The adhesion strength between the Cu surface and the barrier layer with different pre-treatment conditions on the control wafer is shown in Table 7-3-2. On all wafers, 5 points were measured so as to obtain average values in order to acquire a reliable result. From the

results, 10-second NH_3 pre-treatment has the weakest adhesion strength, indicating that some Cu_xO doesn't be removed under this condition. This is agreed with the previous results of Cu_xO removal efficiency. On the other hand, 30-second NH_3 pe-treatment has the highest adhesion strength compared to the three conditions. This arises from the new chemical bonding formed in the NH_3 pre-treatment. Figure 7-3-8 illustrates the possible bonding mechanism to explain this phenomenon. New-forming Cu-N bonding will capture the Si-atom of the barrier film to produce the chemical bonding. As a result, the adhesion between the Cu and the barrier film increases as well.

In a standard dual-damascene processing, the pre-treatment exposes not only the Cu surface but also the under-layer interlayer dielectric (ILD) layer. As a result, the effect of the pre-treatment on the ILD layer should be taken into consideration. For a low dielectric ILD layer, the dielectric constant is the most important parameter. The result dependent of pre-treatment conditions is shown in Figure 7-3-9. The change of dielectric constant is less than 5% for all treatment conditions. Additionally, NH_3 plasma treatment seems to have a slight increment, which may contribute to the nitridation at the top portion of the ILD layer.

The electrical data from the metal test pattern exposed on the wafer surface during pre-treatment has been evaluated to check the Cu line-to-line leakage current and the Cu line sheet resistance. Shown in Figure 7-3-10 is a plot of the Cu sheet resistance with 0.20μm and 3.0μm in width. It is shown that the sheet resistance is essentially independent of the NH_3 and H_2 plasma pre-treatments, as the temperature of the plasma treatment is controlled at

350^{o}C with no significant change to the Cu crystal. The XRD spectrum (not shown) also displays no changes and demonstrates this result. On the other hand, the line-to-line leakage current is sensitive to the pre-treatment conditions as shown in Figure 7-3-11. A NH_3 plasma pre-treatment results in a lower leakage current than H_2 pre-treatment. The possible reason is that the leakage current through the surface path between SiN/Cu and SiN/low-*k* film was greatly improved due to the new chemical bonding form for the NH_3 pre-treatment. As for the pre-treatment time effect, no significant impact on the leakage current for the NH_3 pre-treatment. However, 30-second H_2 pre-treatment had a worse effect on the leakage current than a 10-second H_2 pre-treatment.

7-3-4 Summary

NH_3 and H_2 plasma pre-treatments have been investigated as a method of removing the oxide from the Cu surface, to improve the adhesion of the PE-CVD barrier layer to post Cu-CMP surfaces. H_2 plasma treatment showed an excellent Cu_xO removal rate and had less impact on the low-dielectric ILD layer. A higher leakage current between Cu lines was the main drawback for this pre-treatment. Insufficient exposure to the NH_3 plasma pre-treatment leads to an increased occurrence probability of delamination at the Cu/SiN interface. Optimization of the NH_3 treatment time resulted in the reduction of the adhesion failures and a lower metal leakage current.

Table 7-1-1. Film Properties of SiN films with different hydrogen content

SiN film	SiN-A	SiN-B	SiN-C
Hydrogen (%)	25	14	9
Refractive Index(633nm)	2.1	1.96	1.93
Si/N ratio	1.27	1.16	1.08
Density(g/cm^3)	2.05	2.13	2.24
Stess(dyne/cm^2)	6.80E+08	3.60E+08	2.62E+08
Dilectic constant(1 MHz)	7.40	7.45	7.48
Breakdown Voltage(V)	7.4	7.8	8.5
Leakage Current(2MV/cm)	2.85E-11	4.95E-11	5.88E-12
Etch Rate(C_4F_8/O_2) (nm)	1395	1112	943
Etch Selectivity (to FSG)	3.13	3.92	4.63

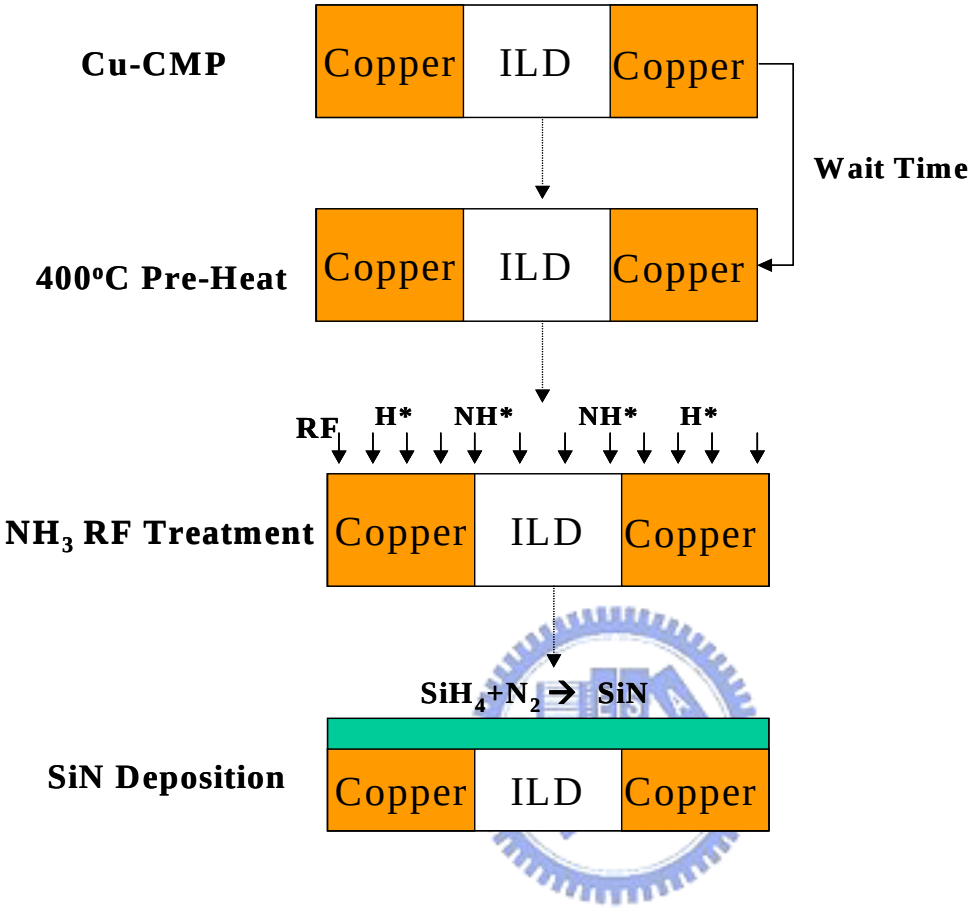


Figure 7-1-1. The process steps between Cu-CMP and SiN deposition.

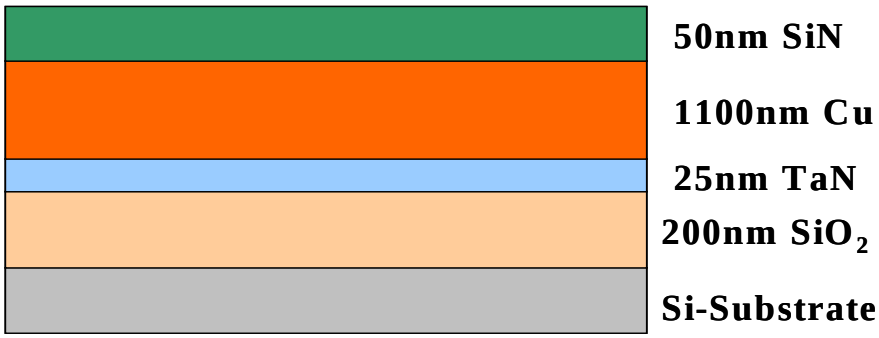


Figure 7-1-2. The experimental film stack of SiN/Cu/TaN/SiO_2/Si (Substrate).

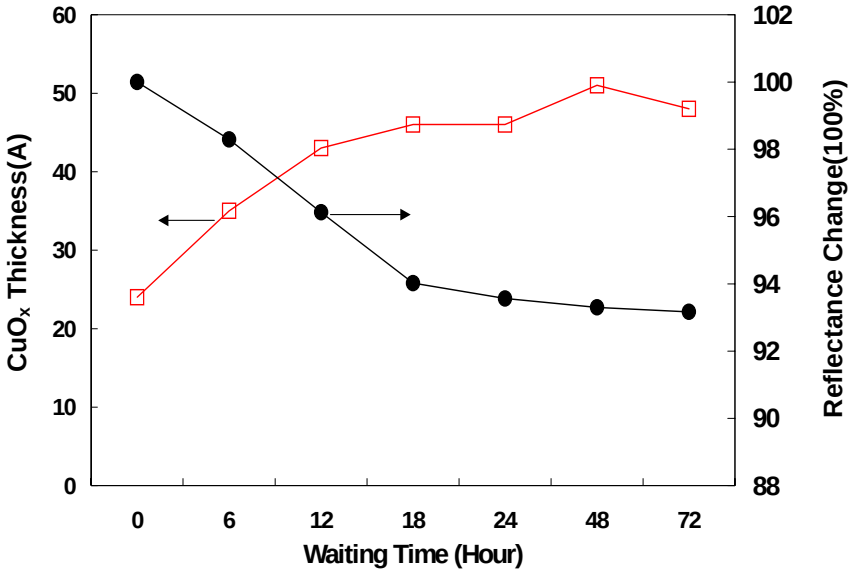
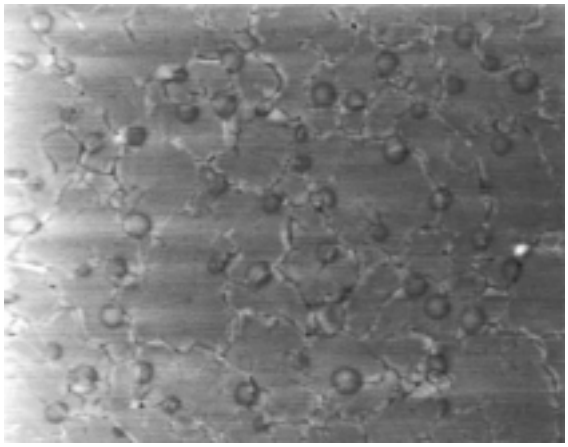


Figure 7-1-3. Cu_xO thickness and the Cu reflectance change as a function of the waiting time.

(a)



(b)

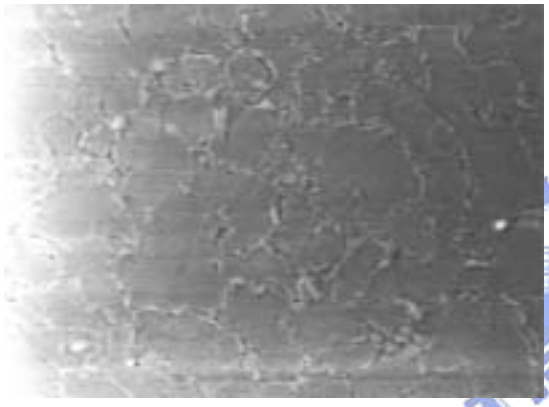


Figure 7-1-4. SEM Image of Cu-Surface with exposing 10KV E-Beam (a) 24hr waiting times with 10sec NH_3 treatment; (b) 24hr waiting time and Post-CMP clean.

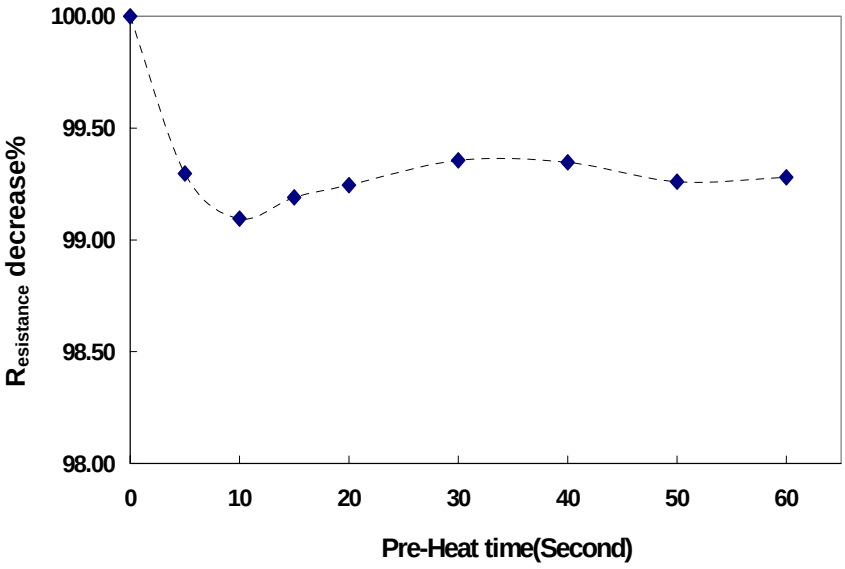
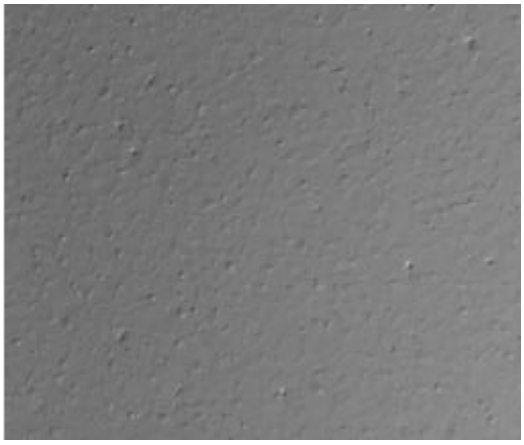


Figure 7-1-5. The Cu resistance decrease percentage as a function of the pre-heating time.

(a)



(b)

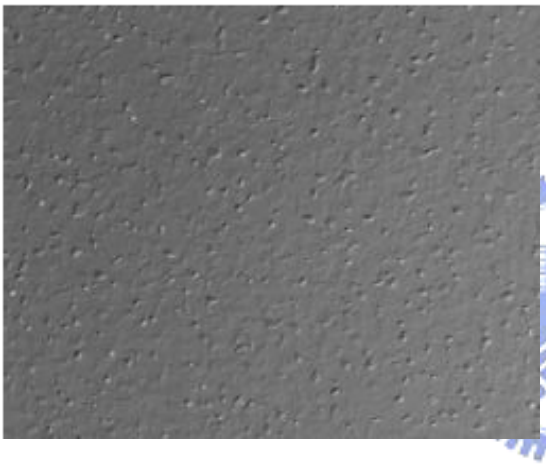


Figure 7-1-6. SEM Image of Cu-Surface Hilllock (a) 10second pre-heating time; (b) 30second pre-heating time.

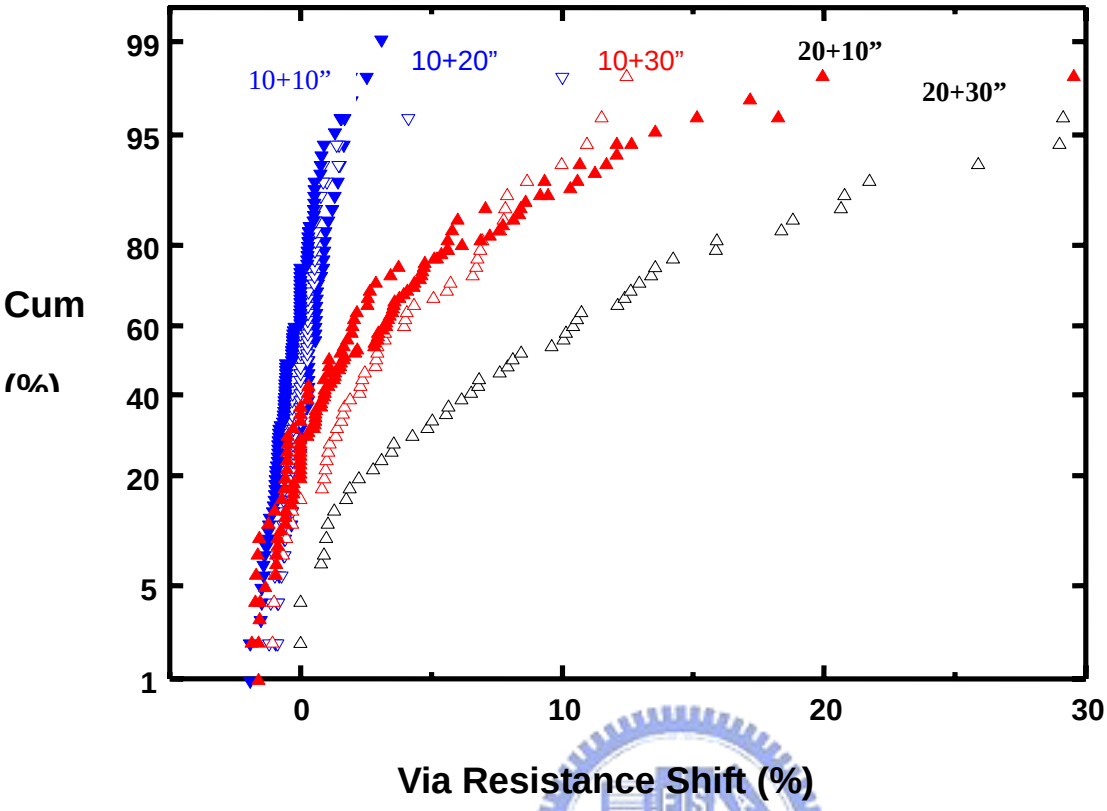


Figure 7-1-7. Effect of pre-heating time and treatment time on the shift of via-resistance.

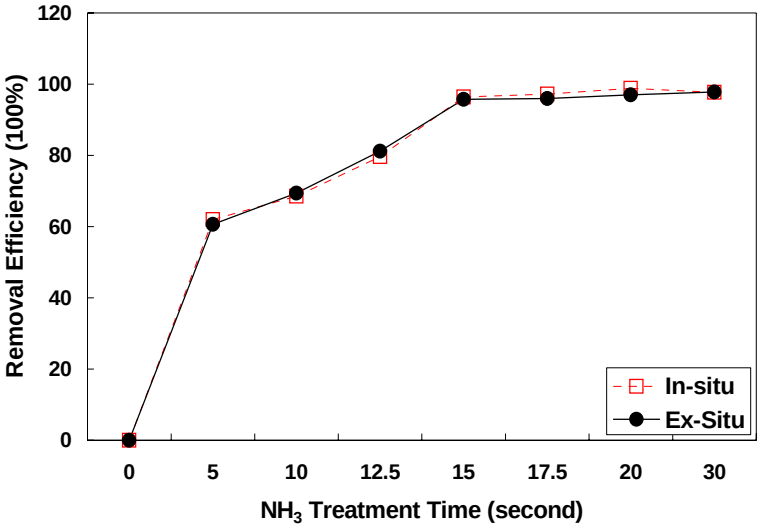
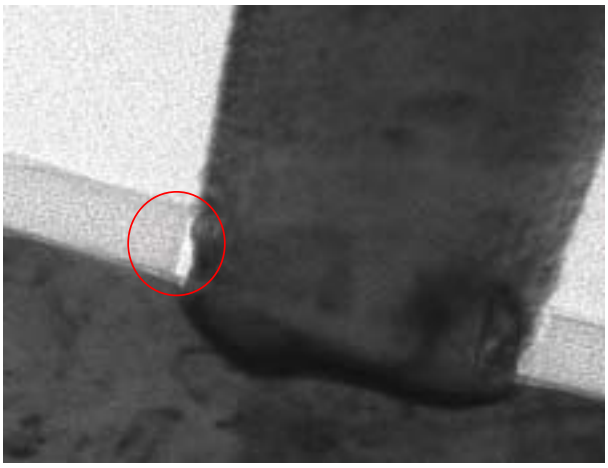


Figure 7-1-8. Cu_xO removal efficiency for in-situ and ex-situ NH_3 treatment.

(a)



(b)

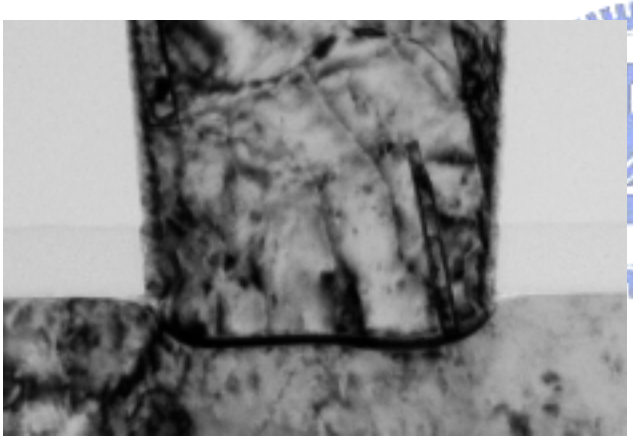


Figure 7-1-9. TEM image of Via profile (a) in-situ; (b) ex-situ NH_3 treatment.

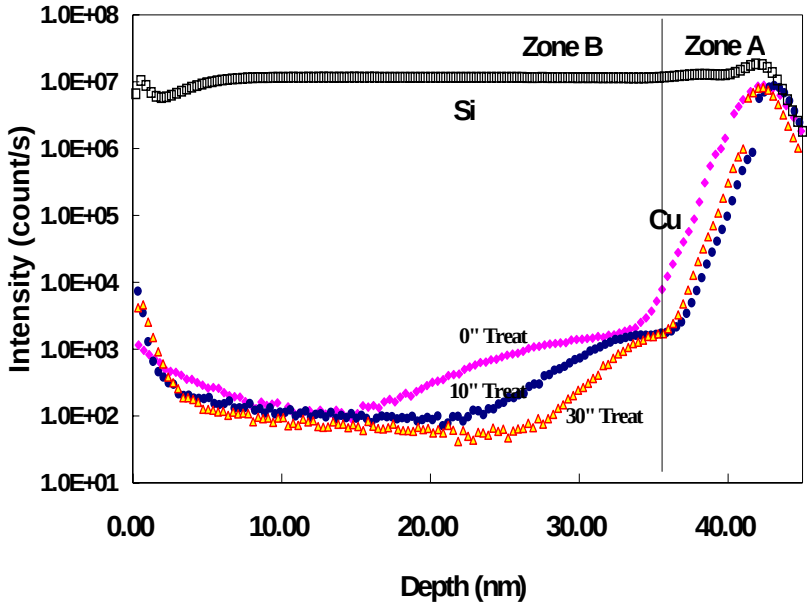
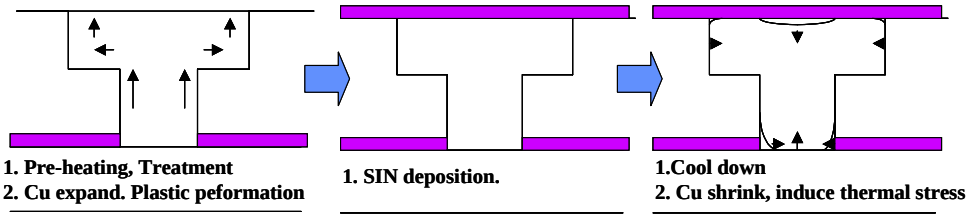


Figure 7-1-10. Secondary Ion Mass Spectroscopy profile of the Cu count with different NH_3 treatment time.

(a)



(b)

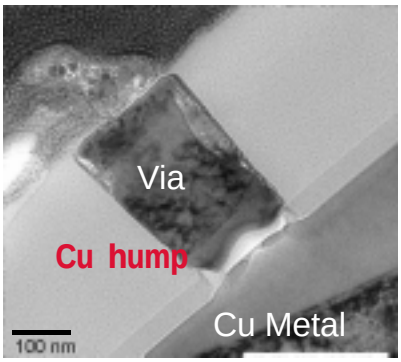
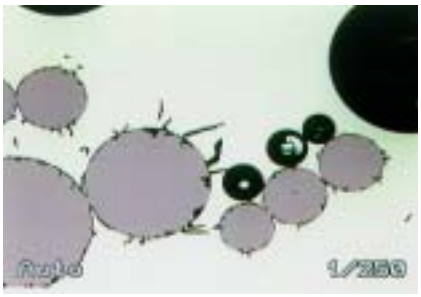


Figure 7-1-11. The possible mechanism of via-resistance shift and TEM image of hump result.

(a)



(b)

Figure 7-1-12. SEM image of adhesion ability of FSG films with varying SiN films (a) SiNA(peeling); (b) SiNC (better adhesion).

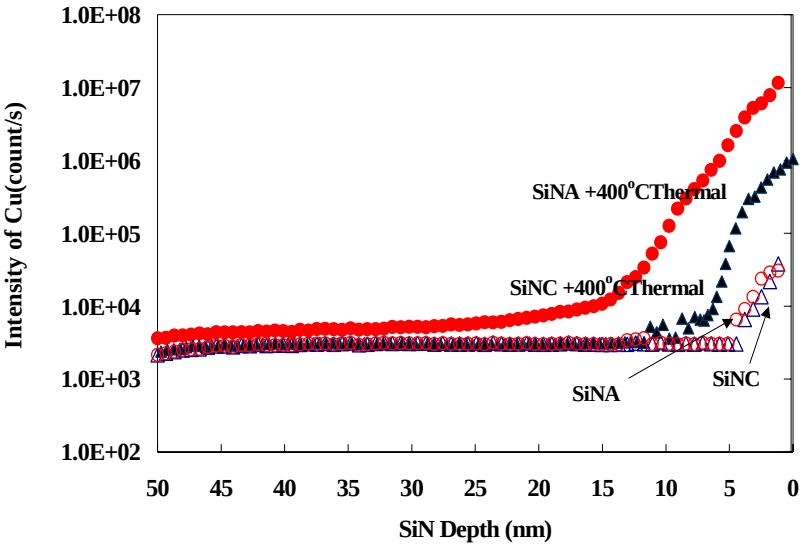


Figure 7-1-13. Secondary Ion Mass Spectroscopy profile of the Cu count with different SiN films.

Table 7-2-1. The process conditions of varying barrier films.

	PE SiN	SiCN	SiCO
Pressure (Torr)	**4.2**	**3**	**3**
RF (W)	**450**	**290**	**290**
Gas flow(sccm)	**SiH_4/NH_3:3 N_2:2500**	**3MS/NH_3:0.5 He:200**	**3MS/CO_2:0.25 He:200**

Table 7-2-2. The component of varying barrier films from XPS and RBS analysis.

	PE-SiN		SiCN		SiCO	
Temperature (°C)	**RBS(Si/O/C/H/N)**	**XPS(Si/O/C/H/N)**	**RBS(Si/O/C/H/N)**	**XPS(Si/O/C/H/N)**	**RBS(Si/O/C/H/N)**	**XPS(Si/O/C/H/N)**
250	38.0/0/0/22/40	43.3/3.8/0/N/52.9	23.8/1.2/25/40.5/9.5	40.2/2.5/35.2/N/22.1	25.5/11.6/28.5/34.4/0	47.1/21.6/41.3/N/0
350	39.5/0/0/13/47.5	44.0/1.0/0/N/54.2	26/0/20/37/17	41/3/31/N/25	28/12.9/26.6/32.5/0	39.2/21.3/39.6/N/0
450	40.5/0/0/7.5/52	44.4/0/0/N/55.6	28.5/0/14/30.5/27	43.3/2/26.8/N/28	31.6/14.8/23.6/30/0	41.5/22.6/36.0/N/0

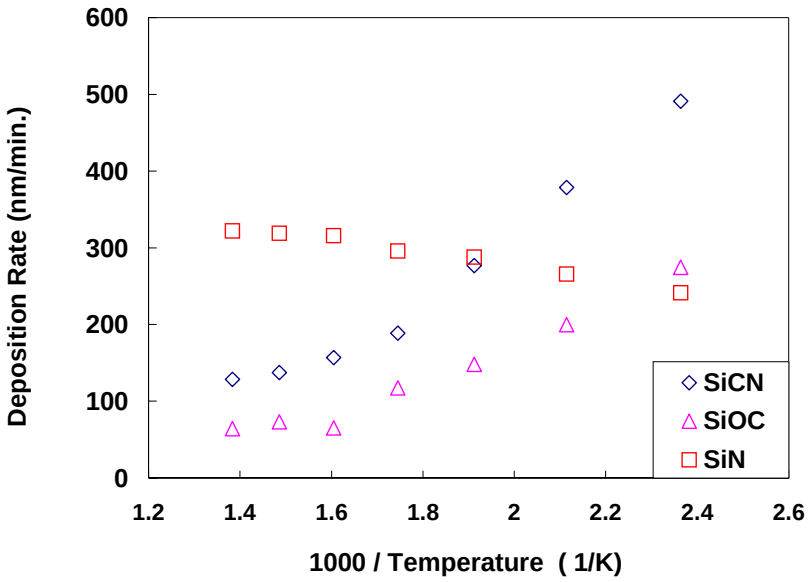


Figure 7-2-1. Deposition rate of SiN, SiCN and SiCO dependence of deposition temperature.

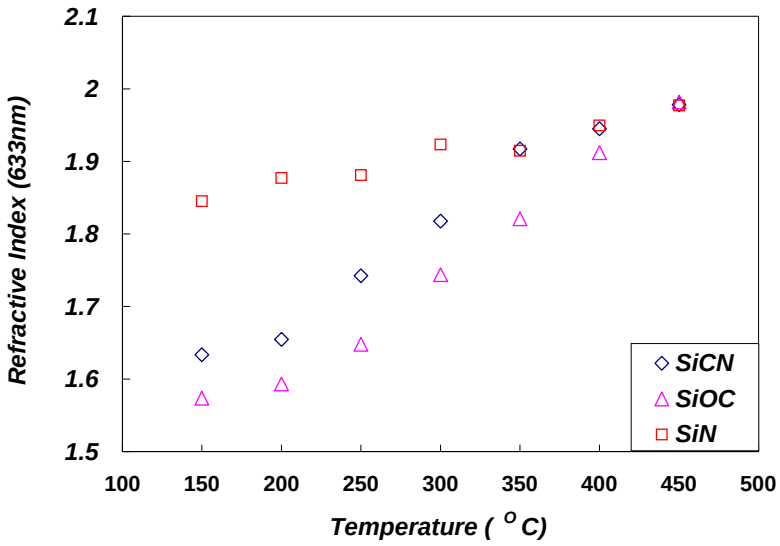


Figure 7-2-2. Refractive index (633nm) of SiN, SiCN and SiCO dependence of deposition temperature.

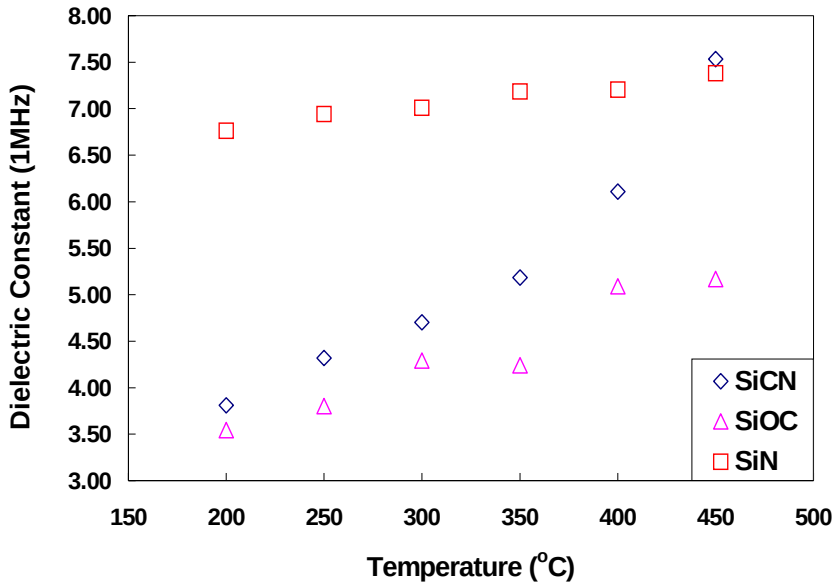


Figure 7-2-3. Dielectric constant of SiN, SiCN and SiCO dependence of deposition temperature.

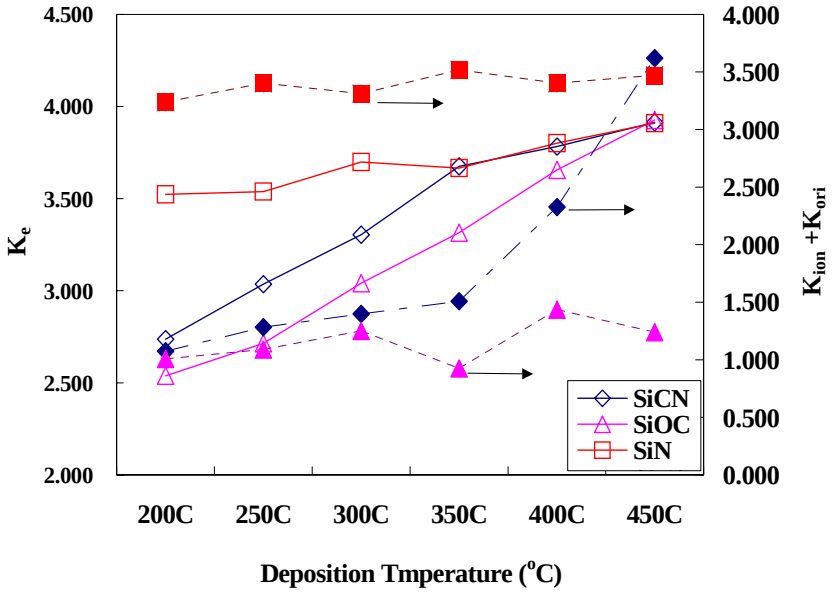


Figure 7-2-4. The electronic polarization (K_e), ionic (K_{ion}) and orientational polarizations (K_{ori}) of SiN, SiCN and SiCO dependence of deposition temperature.

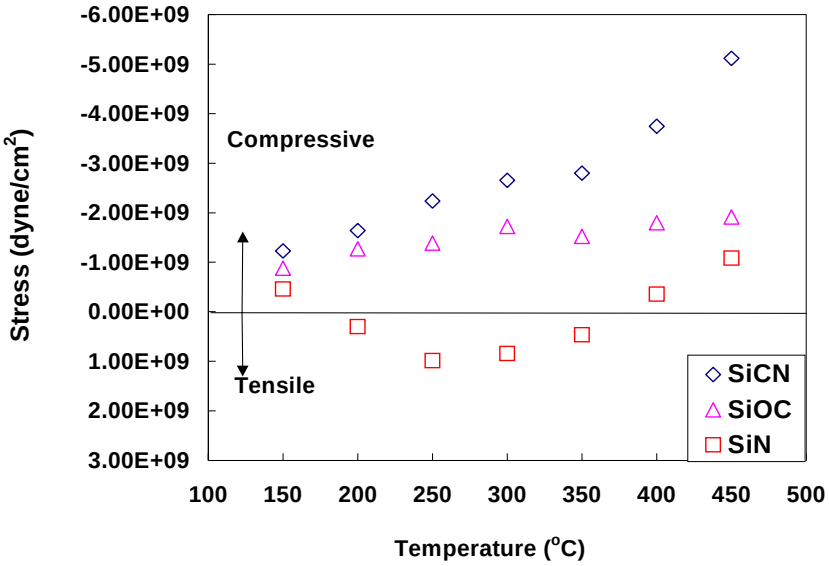


Figure 7-2-5. Stress of SiN, SiCN and SiCO dependence of deposition temperature.

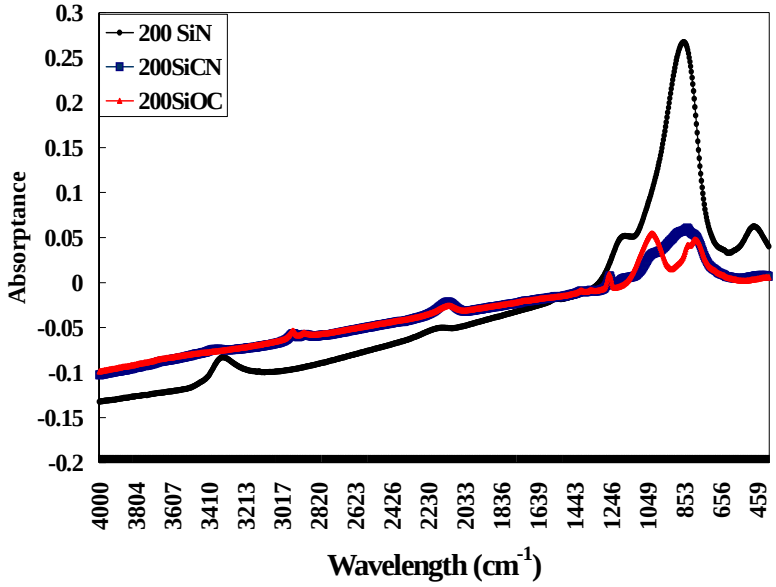


Figure 7-2-6. FTIR spectrum of Barrier films deposited at 200°C.

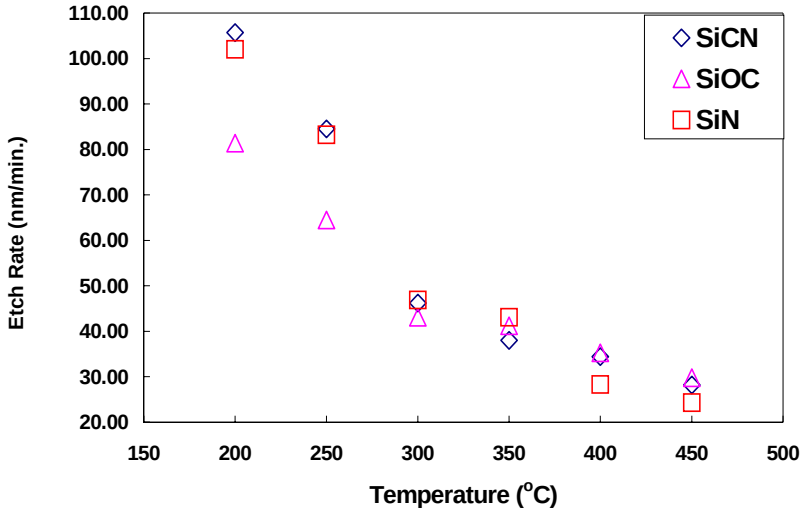


Figure 7-2-7. The RIE rate of SiN, SiCN and SiCO dependence of deposition temperature.

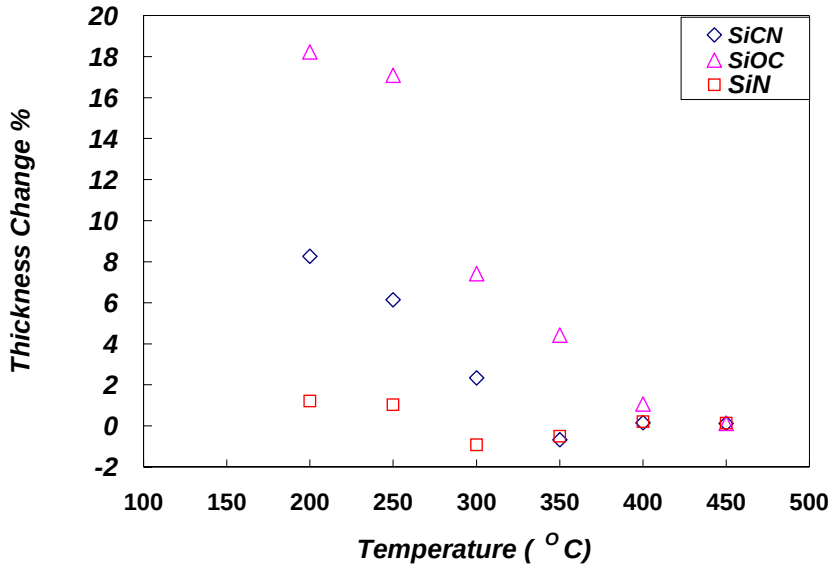


Figure 7-2-8. The thickness reduction of SiN, SiCN and SiCO after 400°C thermal treatment dependence of deposition temperature.

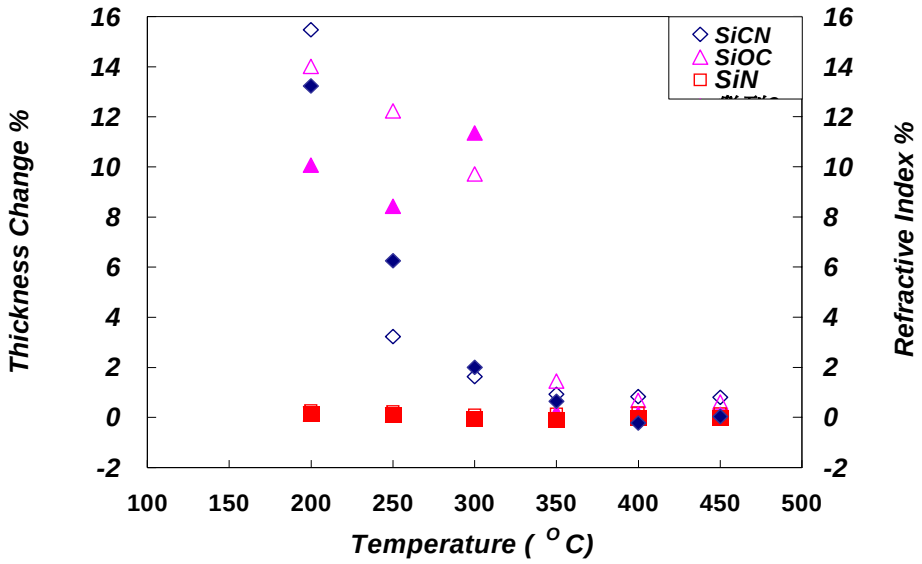


Figure 7-2-9. The Thickness and refractive index change of SiN, SiCN and SiCO after O_2 plasma treatment dependence of deposition temperature.

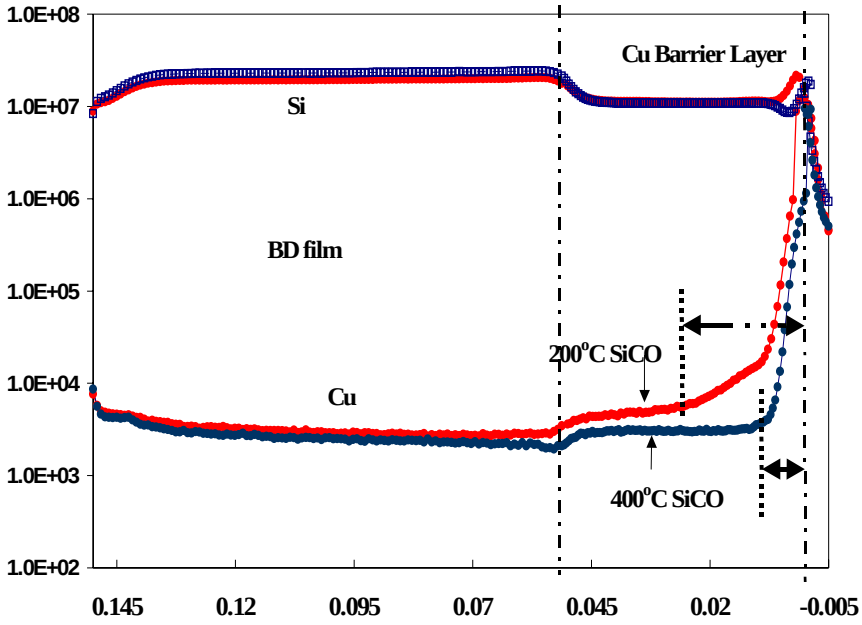


Figure 7-2-10. SIMs spectra of IMD 1k Å /Barrier 500 Å /Cu 8K Å /Si samples. The barrier films were deposited at 200°C and 400°C, respectively.

Table 7-3-1. The process conditions of NH_3 and H_2 plasma pre-treatment.

Process Parameter	NH_3 Treatment	H_2 Treatment
Temperatue (^oC)	350	350
RF power (W)	300	300
Pressure(Torr)	4.2	5.5
Spacing(miles)	450	450
Gas Flow(sccm)	NH_3: 35 N_2: 500	H_2: 300

Table 7-3-2. The adhesion strength between Copper and SiN films for NH_3 and H_2 plasma pre-treatment.

Substrate	Treatment	Brrrier-Layer	Meas.A	Meas.B	Meas.C	Meas.D	Meas.D	Avg(kg/cm^2)	Avg(Mpa)
Cu	H_2 treat 10"	SiN	858	790	798	782	734	792.4	77.6
Cu	H_2 treat 30"	SiN	729	697	843	774	740	756.6	74.1
Cu	NH_3 treat 10"	SiN	363	903	502	621	558	589.4	57.8
Cu	NH_3 treat 30"	SiN	940	820	789	834	867	850	83.3

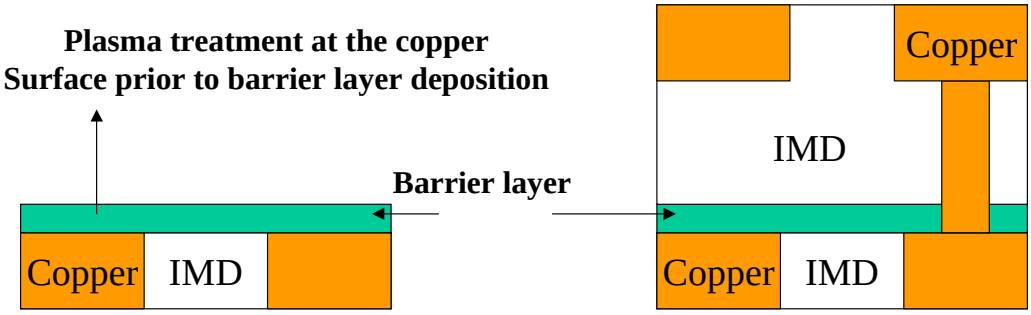


Figure 7-3-1. (a) Cross section diagram of barrier layer(SiN) on planarized IMD/Cu, (b) Diagram of Dual-damascene structure.

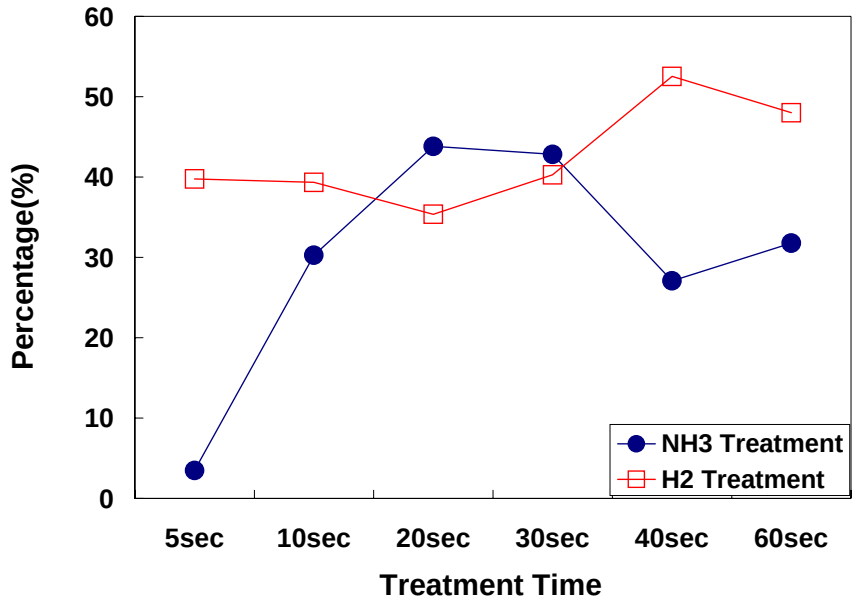


Figure 7-3-2. The comparison of Cu_xO removal efficiency as the function of H_2/NH_3 pre-treatment process.

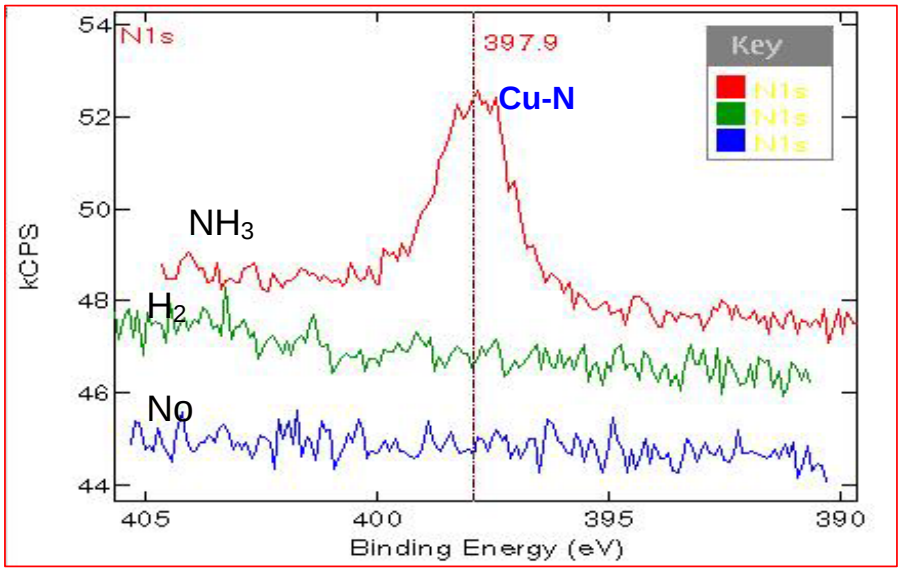


Figure 7-3-3. N(1s) XPS Spectra for different treatment on copper surface.

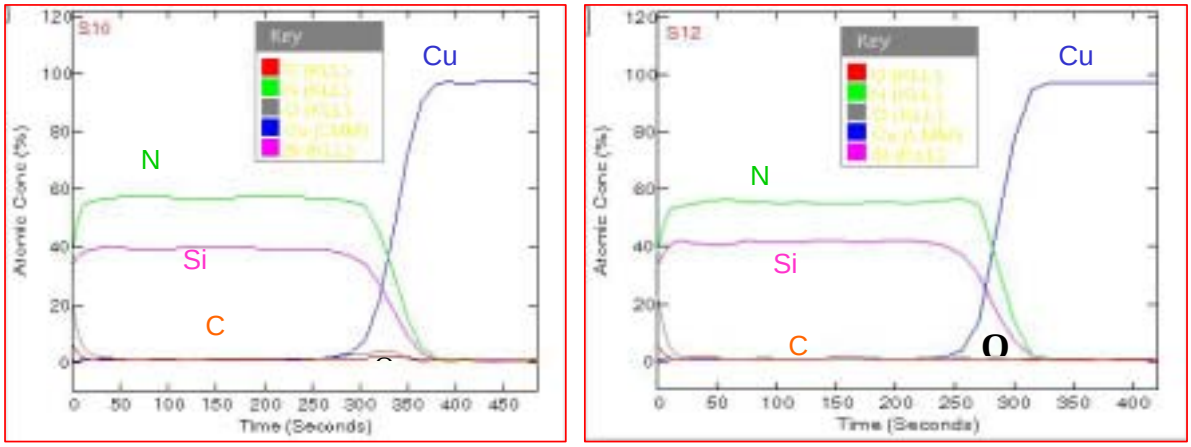


Figure 7-3-4. Auger depth profile (a) 10sec. of H_2 pre-treatment ; (b) 10sec. of NH_3 pre-treatment.

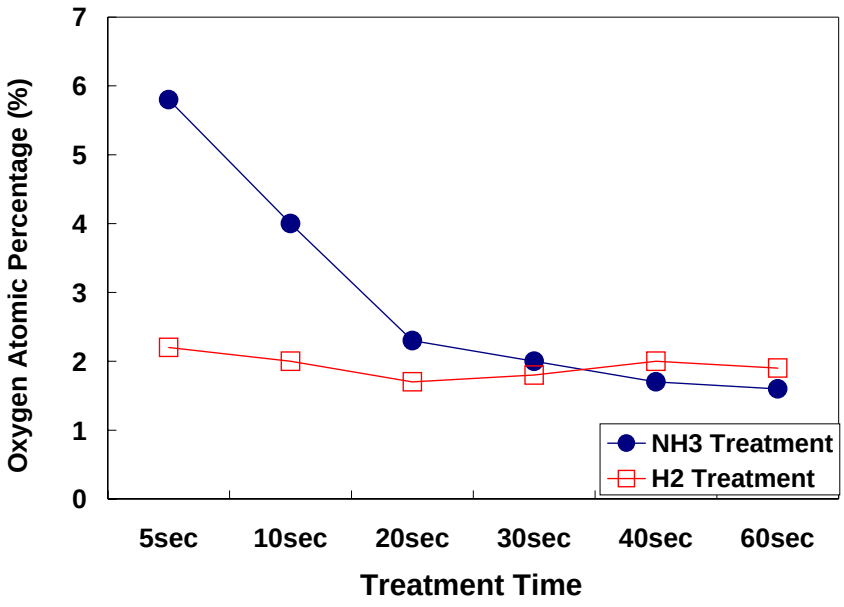


Figure 7-3-5. Oxygen concentration at Cu/SiN interface as the function of H_2/NH_3 treatment process.

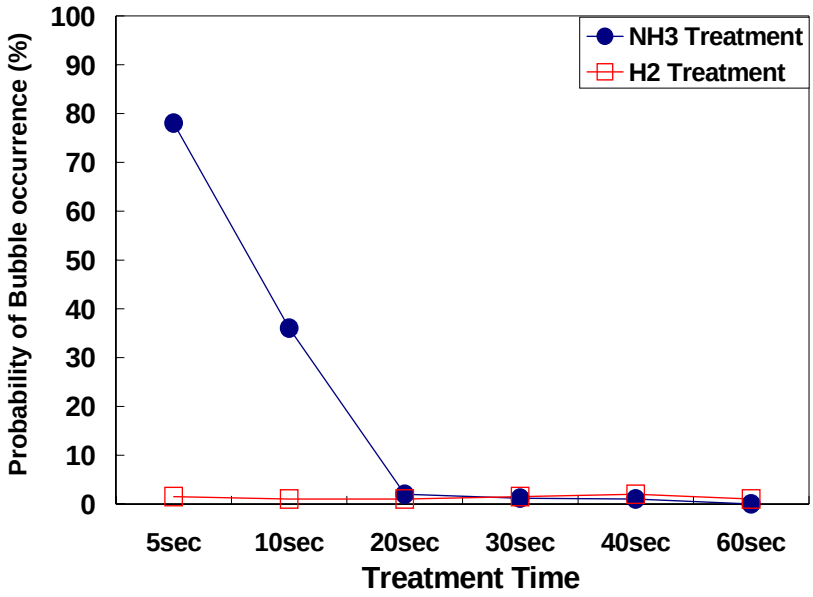


Figure 7-3-6. Probability for bubble defect occurrence as the function of H_2/NH_3 treatment process.

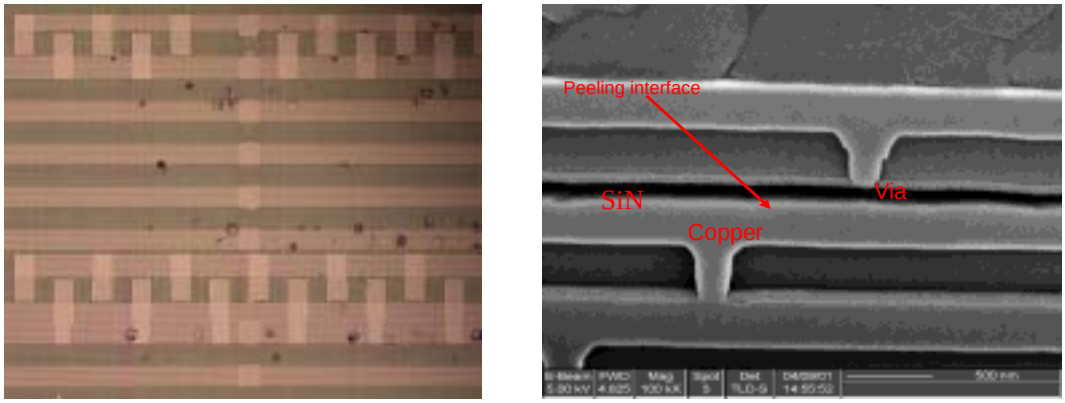


Figure 7-3-7. (a) Bubble Defect on Optical Microscope ; (b) Cross section SEM images of bubble defect.

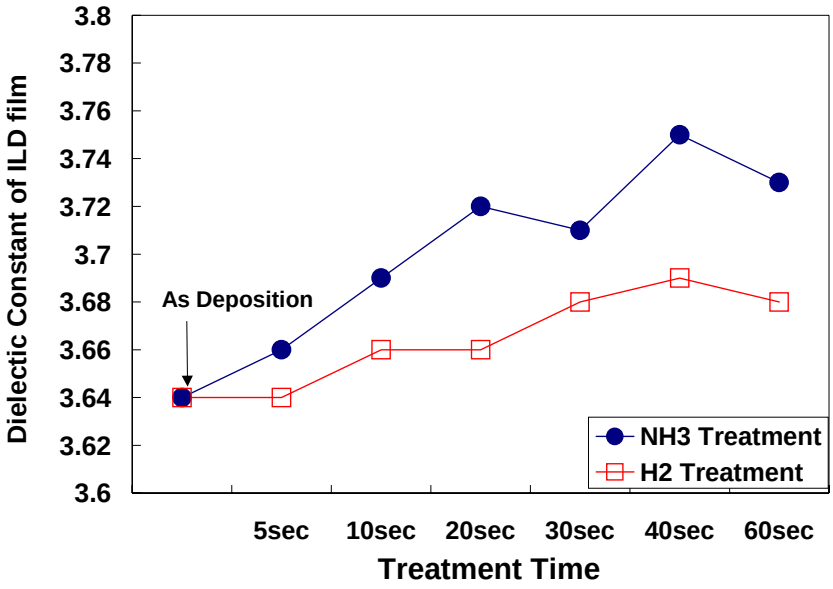


Figure 7-3-8. The change of dielectric constant of ILD as the function of H_2/NH_3 pre-treatment process.

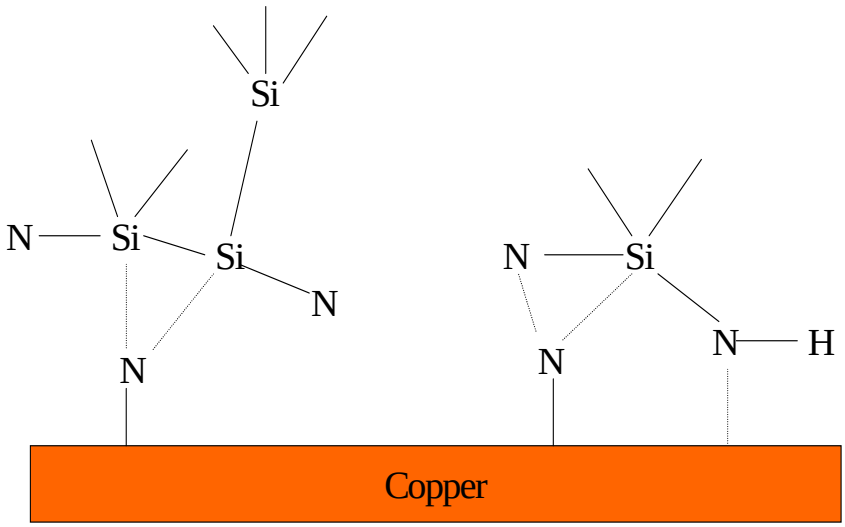


Figure 7-3-9. Diagram of chemical bonding for NH_3 pre-treatment process.

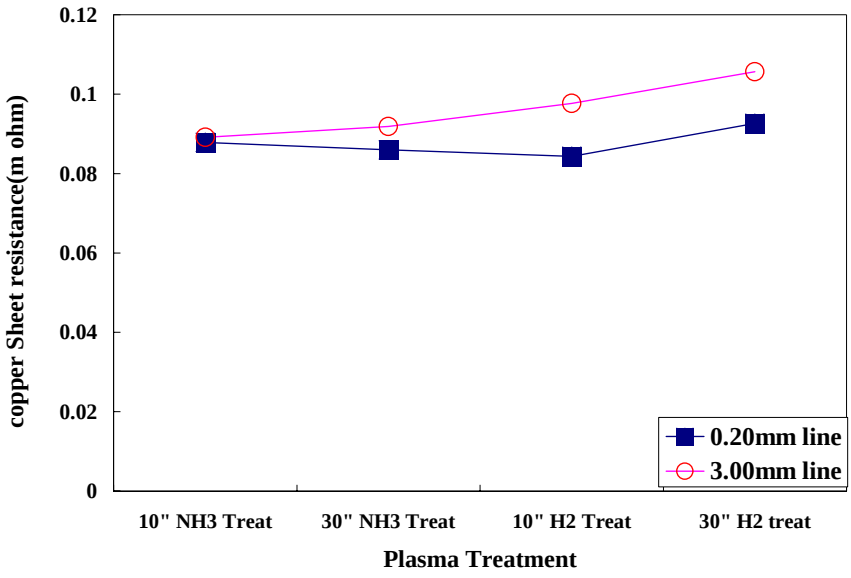


Figure 7-3-10. The sheet resistance of Cu trench for H_2/NH_3 pre-treatment process with two copper line dimensions.

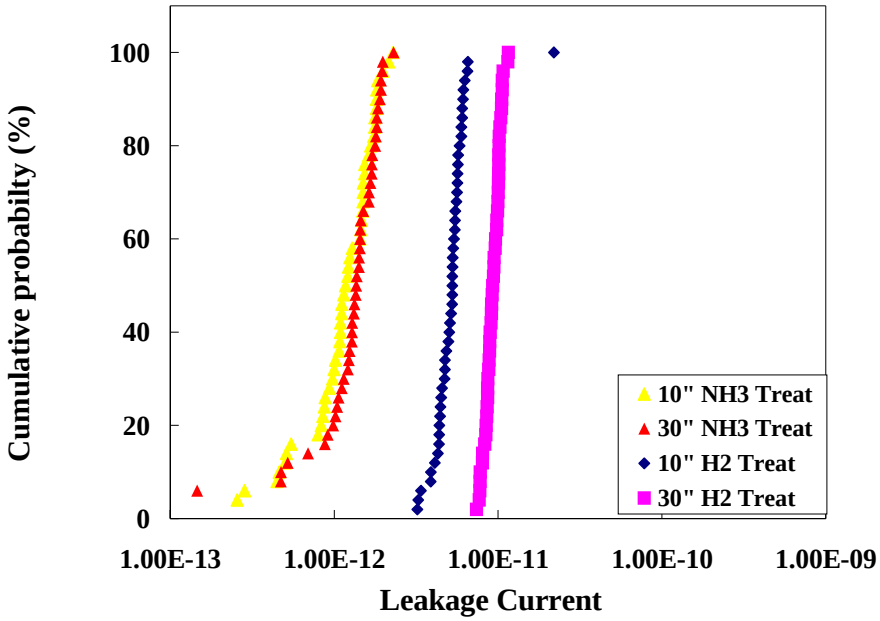


Figure 7-3-11. Metal line-to-line leakage current for H_2/NH_3 pre-treatment process.

Chapter 8
Summary and Future Work

8-1 Summary

In this thesis, the film characteristics and integration issues of developed low-dielectric -constant materials were investigated. The major achievements in this thesis are summarized as follows:

(1) Characterization of HDP-CVD FSG:

There is approx. 0.2 % of F variation between the center and the edge of wafers. This non-uniform F distribution leads to the variation in dielectric constant for about 0.2 at the center and the edge of wafers. Because of that, the device performance will vary for devices processed on the same wafer and it will be a concern to put FSG into production. The SIMS data shows that the thermal stability of FSG can be enhanced by using a cap layer and SRO is superior than PE-OX in blocking the F diffusion at high temperature and moisture environment. HDP-FSG can fill the gap as small as 0.23 μm gap which indicates that FSG can be used for the 0.18 μm processes. However, it will be more difficult to use FSG in process less than 0.18 μm.

In additional, the thermal stability for fluorine-doped silicon dioxide deposited by high-density plasma chemical vapor deposition is highly influenced by deposition temperature. All analyses, including SIMS, TDS, and annealing thermal tests, have shown that SiOF films deposited above 400°C have better thermal stability. However, the high deposition temperature (over 450°C) creates metal (AlCu) extrusion and melting issues. Patterned wafers with short-loop results have also demonstrated that low deposition temperature results in F-bubble formation because of greater amount of more free fluorine. Results of this study demonstrate that the deposition temperature of SiOF films is extremely

important for the films thermal stability.

(2) Set up a robust FSG scheme in 0.18 μm:

For robust integration of FSG films, a double interlayer of high-density plasma FSG and SRO has been developed to control fluorine instability for sub-0.18 μm device. On the other hand, the interconnect conditions need further study for robust integration. A higher FSG deposition temperature, PE-N_2 plasma treatment on FSG layer, and a stack of HDP-FSG and PE-FSG layer interconnect are proposed to prevent FSG bubble, Al delamination, and Interconnect crack. HDP-FSG can fill the gap as small as 0.23 μm gap which indicates that FSG can be used for the 0.18 μm processes. In 600Å USG/8000Å FSG/2,000Å SRO cap layered structure, HDP-FSG shows 7.45 to 7.7% line-to-line capacitance reduction and has similar via resistance to that of USG film.

(3) Characterization of Carbon-doped low-*k* films:

Lower dielectric constant as well as higher mechanical strength of PE-CVD low-k films are required for circuit speed and package. Low-*k* films process conditions, such as deposition temperature, carrier gas, and process precursors, significantly influenced the film's properties. In our study, low-k films deposited by PE-CVD using 3MS and O_2 precursors in Ar carrier gas exhibited the strongly improvement in deposition rate, non-uniformity, leakage current and hardness due to decreasing micro-porous. However, a bit scarification on dielectric constant of the deposited low-*k* films occurred. On the other hand, The DEMS-based low-*k* films had a lower dielectric constant, higher hardness and higher

chemical and thermal stability than those of the 3MS-based films. From the results of blanket films and four-level interconnect test devices, the DEMS-based films were found to have superior electrical performance than that of the 3MS-based films. Above results clearly reveal that the DEMS-based films are the promising low-*k* materials in the next technology generation.

Additionally, a higher heat resistance is necessary to prevent degradation during the interconnect fabrication process. The films deposited from the DEMS precursor at higher temperatures show a lower amount of C and a preference for monomethylated Si atoms relative to lower deposition temperatures and the higher cross-linking bonding due to CH_n bridging network, resulting in higher hardness strength and thermally stability. The electrical performance films from DEMS deposited at different temperatures in ILD test structures was provided similar results as blanket films, showing good electrical performance.

The composition, bonding configuration, optical, mechanical, electrical properties and thermal stability of SiCOH films using diethoxymethylsiliane (DEMS) and oxygen (O_2) as a precursor by PE-CVD method have been investigated in this work. The refractive index of SiCOH increases with increasing deposition temperature yet decreases with increasing oxygen addition to the deposition recipe. The addition of oxygen dramatically enhanced the plasma deposition rate of DEMS. The as-deposited films also show lower the dielectric constant and decreased mechanical hardness and modulus. The effect of which is reduced at

higher temperatures. The results can be accounted for by the changes in composition and bonding configuration, as determined from FT-IR and elemental analyses. The low dielectric constant organo-silica-glass (OSG) films deposited by DEMS and oxygen is shown to be the most reliable: the dielectric constant are stable even after a heating test at 700^{o}C and a pressure cooler test for 168hr, and superior to other PE-CVD low-*k* films deposited by other precursors. However, O_2 plasma ashing process lead to the dielectric degradation in deposited low-k films during photoresist removal processing. The nitrogen plasma treatment is proposed to prevent the damage from oxygen attack on the low-*k* films deposited by DEMS.

(4) New developed low-*k* films: Combination of FSG and Carbon-doped low-*k* advantage:

A new low-*k* interlayer dielectric material, organofluorosilicate glass, has been developed and characterized in this study. The addition of silicon tetrafluoride to a trimethylsilane-based organosilicate glass deposition process provides chemical and structural changes to the deposited film that result in improved mechanical strength at comparable dielectric constants to their non-fluorinated analogs. The presence fo SiF_4 in the plasma affects the replacement of more labile organic species with 2-3 atomic percent inorganic fluorine, providing enhanced material stability. The chemical and structural changes also result in enhanced adhesive strength and reduced residual stress and stress hysteresis. The resistance of organo-silicate glass (OSG) and fluorine-doping

organo-silicate glass (OFSG) films against heat and moisture stress test was investigated. Compared with OSG films, the OFSG films were shown to be have superior thermal stability and electrical properties. The enhanced degradation of the dielectric constant of OFSG films during moisture stress tests was attributed to the hydrolytic instability of Si-F bonds. Consequently, similar to fluorosilicate glass, moisture resistance of the OFSG film will require attention during integration of this material.

(5) Characterization of Cu barrier/stop later with lower dielectric constant on Cu dual-Damascene:

In Cu dual-damascene structure, Cu barrier layer deposition becomes more and more essential. This barrier layer not only must have as low as dielectric constant to further reduce the effective dielectric constant of the Cu interconnect system, but also have good adhesion strength with Cu layer. Silicon nitride is still the primary candidate for the Cu capping barrier and etching stop layer required in the Cu dual damascene structure. However, high dielectric constant (k ~7.0) constrains silicon nitride usage.

Silicon nitride (SiN) and 3MS-based silicon carbide (SiCN and SiOC) films deposited by plasma-Enhanced Chemical Vapor Deposition (PE-CVD) have been comprehensively investigated by varying deposition temperature. The important requirements for the Cu barrier layer were adequately considered in terms of these three films. Among these barrier films, PE-SiN films with varying deposition temperature (200-450^{o}C) still were the excellent option as Cu barrier layer film due to the possession of high barrier properties and integration capacitance. In addition, SiN film with a low hydrogen content has a superior etch selectivity

and a better electrical performance. However, the lethality of this film is higher dielectric constant, as high as 7.0.in the 200-450^{o}C deposition temperature. Therefore, much effort need to done to lower permittivity for the reduction of the parasitic capacitance. On the other hand, a 3MS-base barrier film, including SiCN and SiCO films, can reduce the dielectric constant to 3~5, depends on the deposition temperature. Although the film with lower deposition temperature can further reduce the dielectric constant, it suffers from the predicament of the thermal and chemical stability. As a result, the deposition temperature of the film must above 350^{o}C to improve its properties to have a good fit as Cu barrier layer.

(6) An optimized Integration process for Cu barrier layer deposition:

Cu can be easily be oxidized when exposed to commonly used processing environments at low temperatures (<200^{o}C), and such oxidation could negatively impact component performance and reliability. Therefore, copper oxide should be completely removed by reduction reaction through Hydrogen treatment to ensure superior conductivity of the Cu interconnects and to enhance the adhesion of SiN to the post Cu-CMP surface. NH_3 and H_2 plasma pre-treatments have been investigated as a method of removing the oxide from the Cu surface, to improve the adhesion of the PE-CVD barrier layer to post Cu-CMP surfaces. Optimization of the NH_3 treatment time resulted in the reduction of the adhesion failures and a lower metal leakage current. In addition, excessive thermal time (pre-heating and treatment time) induces the Cu-hump problem, resulting in a reliability failure. A longer waiting time (>18hr) leads to delamination at the SiN/Cu surface, even after performing the NH_3 treatment. The post Cu-CMP clean seemed to effectively solve this issue, but increased the process complexity. Therefore, optimization of the process time prior to the Cu barrier layer deposition process is crucial for ensuring the performance of the Cu interconnects.

8-2 Suggestion and Further Research:

When the device generation continuously shrinks to 90 nm or below, some effects on Cu layer and lower dielectric become an issue and related to this thesis which deserves further studies:

(1) Evaluation of porous low-*k* material (k<2.5) based on deposition method, process conditions, precursors, and post-treatment for future application.

(2) Investigation of intrinsic characteristics of low-dielectric-constant materials in high-frequency environment.

(3) As trench width below 100 nm, Cu scattering effect makes the Cu resistivity increase. Set-up a model to describe this effect and provide a solution to overcome this issue.

(4) As the *k* value of low-*k* dielectric further decrease, its heat dissipation would also decrease. This induces the serious interconnect Joule heating issue. Not only will thermal effect be a major reliability concern, but also the increase of resistivity with temperature can be degrade the speed performance. As a result, establishment of thermal analysis in deep submicron interconnects with different low-*k* dielectrics.

(5) The effect of the low-*k* dielectric materials, including barrier layer and ILD layers, on the electron-migration, stress migration induced voiding, and time-dependent dielectric breakdown performance of Cu interconnects. Create the correlation between film properties and the reliability performance and set-up a predicted model to simulate the reliability performance.

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論文題目：低介電常數材料之研究及其在深次微米金屬半導體積體電路之製程整合之研究

Study of Low-Dielectric-Constant Materials on Process Integration of beyond sub-micron MOS integrated circuits

Publications

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[2] **中華民國專利 No. 90107073.** “ 去除高密度電漿化學氣相沉積室殘存氟氣體之方法”

[3] **中華民國專利 No. 89120186.** “ 高密度電漿化學氣相反應器的清洗方法”.

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[5] **中華民國專利 No. 90124099.** “ 以氟矽玻璃當作金屬層間介電層的製造方法”.

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and those of oxygen and carbon decrease as the SiF_4 flow rate increase

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indicating that oxygen and

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asymmetric deformation vibration of the CH_3 from