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Design and Realization of a Digital Multiphase-Interleaved VRM Controller Using FPGA

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Abstract - **Voltage Regulator Modules (VRM) are used for low-voltage, high-current dc-dc converters used for high-performance microprocessors and graphic processors. This paper describes the development of a digital PWM controller architecture in applications to multiphase-interleaved VRM. A digital current control technique with interleaved PWM generation and synchronous current sampling has been developed to improve the transient response under large load disturbances. The proposed control scheme for the interleaved multiphase buck converter employs feedback signals of output voltage, output current, and per-phase inductor current. By using a synchronous over-sampling technique for the detection per-phase inductor current and double-edge PWM modulation technique, the current response can reach a dead-beat performance for step current command. Current sharing control is used to equalize the current of each phase converter under possible parameters mismatch. A computer simulation study has been carried out to illustrate the feasibility and performance of the proposed digital control technique.**

Index Terms— **VRM, multiphase buck converter, interleaved, synchronous sampling, FPGA digital control, current sharing control.**

I. Introduction

In order to reduce the power consumption of advanced microprocessors, various technologies are being developed to solve this challenging power design issues. These include low power VLSI design technique, asynchronous digital circuit design technique, dynamic power management, adaptive voltage scaling, and parallel processing technique. Modern microprocessors are designed with lower voltage power supply to reduce power consumption in reaching higher clock rate and higher chip density. When microprocessor suddenly turns on, it needs plenty of current in short time. Low operating voltages and highly dynamic nature of the modern microprocessors require tightly regulated supply voltage. The requirement of dynamic and steady state become stricter and design process of power supply become harder.

The VRM is designed to provide scalable output voltage with low output voltage and high output current that meet the fast dynamic response requirements of advanced microprocessors [1]. In order to improve the power density and efficiency of the VRM, the multiphase-interleaved synchronous buck converter is a major choice in this applications [2]-[3]. The multiphase-interleaved converters are used to solve the need of high power high current and better efficiency. Phase-shift interleaved PWM scheme can effectively reduce the output ripple and distortion with lower switching frequency. The mismatch of device in each phase causes the phase current mismatch [4], and the cost of VRM will be increased. As a result, some control schemes are proposed to control the current sharing problem [5]-[6].

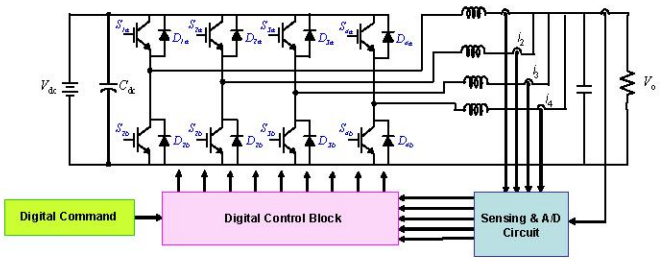

Fig. 1. Block diagram of a four-phase interleaved VRM buck converter with closed loop control.

This paper proposes a digital realization technique of a four-phase interleaved PWM converter with digital closed-loop regulation to reduce its output current ripple with lower PWM switching frequency. Digital current loop control and DPWM control is adopted to solve the possible current mismatch problem. In Section II, the inductor current and output voltage ripple between single-phase and n-phase VRM are analyzed and compared at their open–loop steady-state. Section III describes the hardware design and implementation of the proposed digital control scheme. The developed digital VRM controller includes a phase-shift PWM generator, a digital compensator, and a synchronous ADC sampler. The simulations study of the designed digital controller is given in Section IV and Section V is the conclusion.

II. Digital Controller Design for VRM

Fig. 1 shows the block diagram of the proposed digital controller for the four-phase interleaved VRM buck converter. The output load current is aloes used as feedback to improve dynamic response under large step load change. The core of the digital VRM buck converter is a digital multi-phase PWM control with a synchronously controlled multiplexed ADC converter. The ADC converter is synchronized with both the leading and trailing edges of the PWM output signals and timed to trigger in sampling the middle points of both the rising and falling slopes of the per-phase triangular current. A current sharing controller is used to generate the desired current command of each phase converter within half of its switching period. A digital phase-shift controller is used for generating four pairs of phase-shifted PWM signals and a programmable dead-time

controller is designed to prevent shorted-circuit operation of each phase leg. A digital compensator is designed for the loop compensation of the switching amplifier. The advantages and design issues of the proposed digital controller for multiphase dc-dc converters are addressed in the following.

A. Reduction of Total Inductor Current Ripple

Assume the system works in CCM, for single-phase buck converter, the current ripple of total current could be express as:

$$\Delta I_{1p} = \frac{V_o \cdot (V_{in} - V_o)}{2 \cdot V_{in} \cdot L_o \cdot f_{sw}} \tag{1}$$

where V_o is the output DC voltage, V_{in} is the input DC voltage, f_{sw} is the PWM switching frequency, and L_o denotes the output inductance for a single-phase buck converter. The current ripple of n-phase interleaved VRM is:

$$\Delta I_{np} = \frac{V_o \cdot (V_{in} - V_o)}{2 \cdot V_{in} \cdot L_o \cdot n \cdot f_{sw}} = \frac{\Delta I_{1p}}{n} \tag{2}$$

and the output ripple current can be reduced by a factor n. The reduction of the totoal inductor current ripple means that we can choose a smaller output filter capacitor or to lower the switching frequency of each phase converter to achieve a same output voltage ripple.

B. Reduction of Output Voltage Ripple

The output voltage ripple in a single-phase buck converter could be derived as

$$\Delta V_{o1p} = \frac{V_o \cdot (V_{in} - V_o)}{16 \cdot V_{in} \cdot L_o \cdot C \cdot f_{sw}} \tag{3}$$

and the output ripple of n-phase interleaved VRM is:

$$\Delta V_{onp} = \frac{V_o \cdot (V_{in} - V_o)}{16 \cdot V_{in} \cdot L_o \cdot C \cdot (n \cdot f_{sw})^2} = \frac{\Delta V_{o1p}}{n^2}. \tag{4}$$

Therefore, the value of the output voltage ripple can be reduced by a factor of n^2. In practical applications, the ESR of the output filter can significantly increase the output voltage ripples due to its voltage drops. A set of parallel connected capacitors can be used to minimize this effect. However, variations of the filter inductance and $R_{DS(on)}$ of the power MOSFET of per-phase converter will unbalance the current sharing for each phase converter and proper feedback control technique is needed to be developed to solve this problem.

Fig. 2 shows the block diagram of current loop of the four-phase VRM. The voltage applied to the inductor and current injected into the output capacitor can be expressed as

$$L \frac{di_{Li}}{dt} + i_{Li} r_{Li} = v_{di} - v_o \tag{5}$$

and

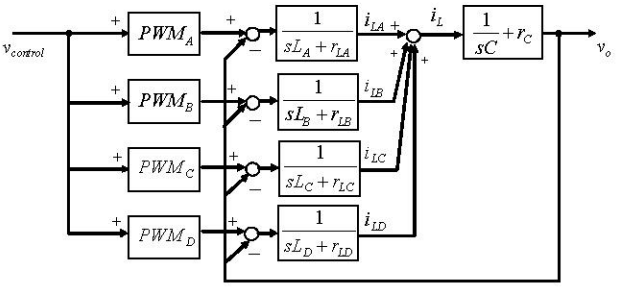

Fig. 2. Block diagram of current loop of the four-phase VRM.

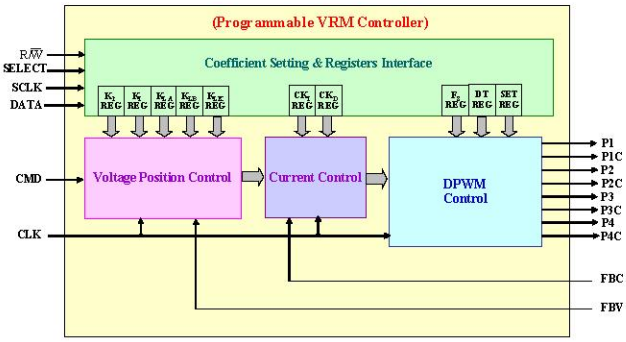

Fig. 3. Block diagram of digital controller.

$$\frac{1}{C} \int i_L dt + i_L r_C = v_o \tag{6}$$

where i_{Li} denotes the current of each phase and i_L is the total current. The key for the current sharing control of an interleaved multi-phase converter is to fast and robust current response under specified parameter variations. An inner current loop controller is applied to each per-phase converter to achieve fast dynamic rsponse and an integrated voltage loop controller is applied for the regulation of the output voltage. A dgital current command is generated at every synchronous sampling frequency to achieve a dedbeat current response control.

In order to avoid the switching noises and get the accurate averaged value of the inductor current, the sampling of the phase inductor current is triggered by its PWM signal on both leading and trailing edge to get the mid-point value on rising and falling slopes. The FPGA circuit realization has been used for both simulation and experimental verification of the proposed digital control scheme for multi-phase interleaved dc-dc converters. Fig. 3 shows the functional block diagram for the realization of the proposed digital multiphase interleaved PWM controller.

III. Digital Controller Realization Issues

In the realization of digital controller, some key specifications should be defined to determine the design parameters, such as the system operating frequency, digital sampling frequencies, and the computational format of each control parameters. The proposed VRM control scheme is realized by using a single-chip FPGA EP2C35 from Altera

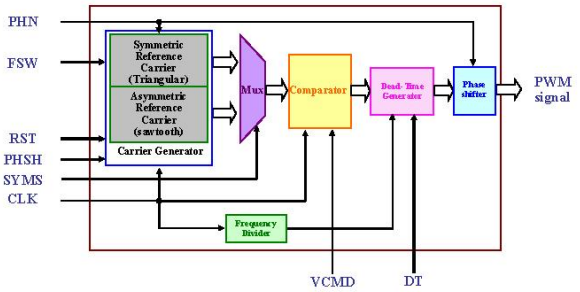

Fig. 4. Block diagram of digital PWM generator.

TABLE I
PIN DEFINITION OF THE DPWM GENERATOR

	Status	Range	Description
CLK	W	0 / 1	Eternal clock, max = 200MHz
SYMS	W	0 / 1	Symmetric selection 0：symmetric wave 1：asymmetric wave
RST	W	0 / 1	Reset output 0：disable output 1：enable output
PHSH	W	0 / 1	Phase shift 0：disable 1：enable
PHAM[2..0]	W	0~7	out put phase number = PHN+1
FSW[11..0]	W	0~4095	Switch frequency = FSW/CLK
DT[6..0]	W	0~127	Dead-time = DT/CLK
VCMD[11..0]	W	0~4095	PWM input signal
PH1-PH4, PH1C-PH4C	R	0 / 1	PWM output signal

Cyclone II device family. The Cyclone™ II devices offer up to 150 18-bit x 18-bit embedded multipliers capable of implementing common digital signal processing (DSP) functions such as finite impulse response (FIR) filters, fast Fourier transforms (FFTs), correlators, encoders/decoders, and numerically controlled oscillators (NCOs). The embedded multipliers provide higher performance and logic efficiency compared to logic element (LE) based multipliers. The embedded multipliers in Cyclone II devices are ideal for low-cost DSP and high-performance digital control applications. The design and realization for each control block of the proposed VRM controller is described in the following.

A. Interleaved DPWM Generator

The increasing of PWM frequency and resolution will require a very high clock frequency and imposes a design constraint both for high-frequency digital circuit design and cost. Various realization schemes, such as counter-comparator, delay-line, and hybrid one, etc., have been developed for the generation of digital PWM signals in order to reduce the clock rate for an acceptable PWM resolution.

Higher switching frequency also companies with higher

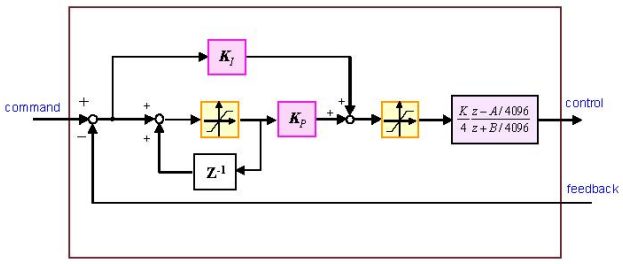

Fig. 5. Block diagram of compensator.

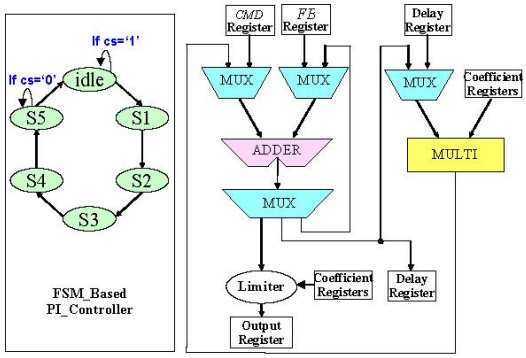

Fig. 6. Hardware circuit schematic of compensator.

switching losses and electromagnetic interference. Therefore, it becomes a design trade-off between the required PWM switching frequency, control resolution, control scheme, and circuit topology. Interleaved PWM technique with phase-shift control has been developed for high-density DC-DC converter to enhance its current output capability in VRM applications. Phase-shift interleaved PWM scheme can effectively reduce the output ripple and distortion with lower switching frequency.

Fig. 4 shows the functional block diagram of the proposed DPWM and the pin definition of the digital PWM generator is listed in Table I. In the proposed approach, the timing clocks for the digital controller and the digital PWM generator are interlaced with each other to achieve a minimum delay at a same sampling and switching frequency. The DPWM is designed to apply flexibility to different power applications. The interleaved phases, dead-time setting, symmetric or asymmetric reference carrier alternating, and PWM switching frequency, is designed as programmable. The maximum speed of DPWM can be clocked to 200MHz.

The PWM reference carrier generators are set into two sources which can both produce symmetric and asymmetric reference carrier waveforms. Setting the “SYM/ASYM” pin, we can decide which one to pass on to the comparator. The waveform of SYM is triangular and ASYM is sawtooth wave. This carrier signal is compared with the modulation signal to generate a timing triggered PWM signal.

By the shape of the modulation sawtooth wave, there are leading-edge modulation and trailing-edge modulation. Both of them belong to asymmetric wave, while the dual-edge modulation is the symmetric reference. The leading edge modulation scheme is good for the transient of load-

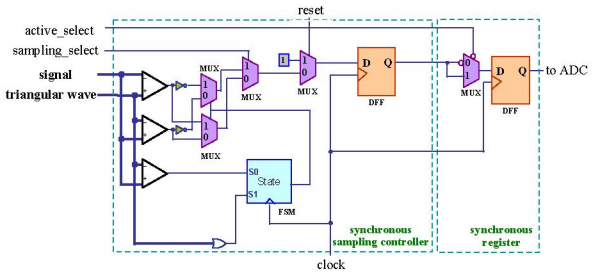

Fig. 7. Circuit realization of the synchronous current sampling scheme.

adding event. In the other hand, the trailing-edge modulation is good for load-releasing transient event. To suit different kinds of application, sometimes we have to change the modulation carrier. That's why the block offers the different modulation reference.

In order to prevent the two switches of each phase in VRM system from conducting in the same time, dead-time is required to design into the PWM signal. The dead-time is programmable for the symmetric carrier wave. The phase shifter can offer up to 4 pairs PWM signal that determine the switches on/off in VRM. Divider and multiplier are applied to generate different number of phase. The phases of each output will be shifted with $2\pi / n$ degree.

B. *Digital Compensator*

Fig. 5 shows the block diagram of the designed digital compensator. A scheduling strategy for realizing the PI controller by using finite-state-machine (FSM) is presented. Fig. 5 shows the hardware circuit architecture of the compensator. The whole computing process takes one adder, one unit delay register, and one multiplier. Furthermore, each control parameters can be programmed.

The compensator can be separated into two parts. One is the PI controller, the other is lead controller. The limiter in the integrator of PI controller is designed programmable boundary. The lead controller is implemented with direct form II, and the difference equation of lead controller could be derived as:

$$D(z) = \frac{y(z)}{x(z)} = K_0 \frac{1 - A_0 z^{-1}}{1 + B_0 z^{-1}} \Rightarrow \begin{cases} y(n) = K_0 (w(n) - A_0 \cdot w(n-1)) \\ w(n) = x(n) - B_0 \cdot w(n-1) \end{cases} \quad (5)$$

C. *Synchronous Sampling*

The current control loop of a DC/DC converter plays an important role for robust performance and current sharing control for multiphase synchronous buck converter, however, the switching of power transistors will induce voltage spikes in the current sensing circuit due to the common-mode noises. These coupling noises not only corrupt the dynamic response of the current loop they may also cause result system unstable. This phenomenon is especially severe in a digital current control loop when the sampling frequency is asynchronous with the switching frequency.

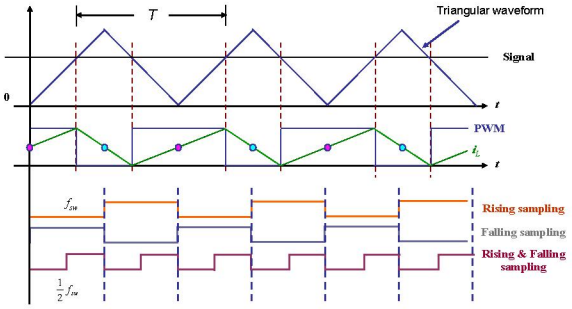

Fig. 8. Timing diagram of the synchronous sampling process.

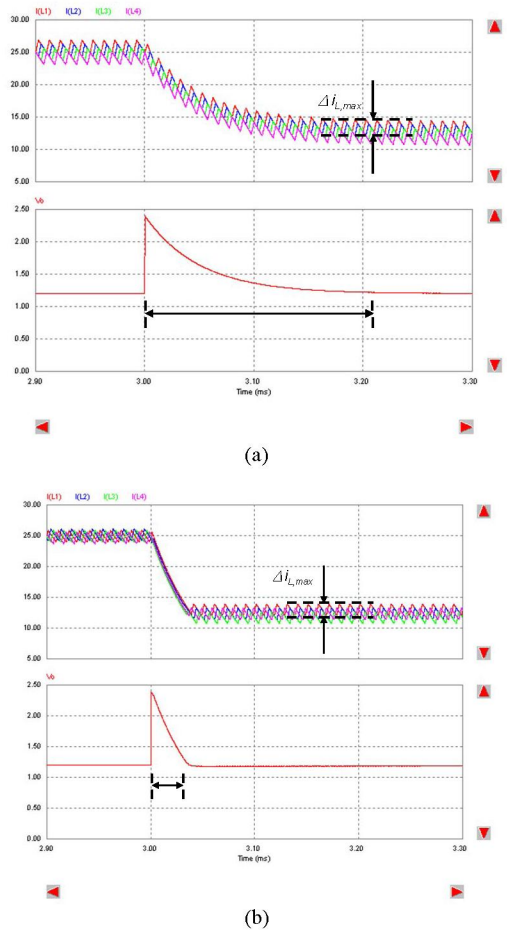

Fig. 9. Output voltage and phase currents for load current step up (a) without feedback control, and (b) with feedback control.

The low-pass filters within the feedback loop can reduce high frequency noises, however, they also impose time delay and slow down the dynamic response. Therefore, the use of low-pass filters for feedback signal detection should be avoided in VRM applications. Because the switching noise is synchronized with its PWM switching, we can sample the current signal in the middle of the two switching to obtain a maximum signal-to-noise ratio. Fig. 7 shows the synchronous sampling circuit. The sampling mode can be chosen as rising or falling, while the active mode can be set as active low or active high.

In order to sample the phase current and prevent the current spike or disturbance, the synchronous sampling

TABLE II
PARAMETERS OF THE DESIGNED FOUR-PHASE VRM.

V_{ref}	reference voltage	1.2V
V_{in}	input voltage	5V
k	number of phase	4
f_{sw}	switching frequency	100kHz
L_i	phase inductors	4.8uH
C_o	output capacitance	10nF
r_L	inductor ESR	1mΩ
r_C	capacitor ESR	1mΩ
V_{ref}	reference voltage	1.2V

circuit offers the sampling signal by the PWM carrier wave. The load current is sampled in each synchronous digital current control loop and is used as the current feedback for load current sharing control.

Fig. 8 shows the illustrated timing diagram of the synchronous sampling process. The rising and falling edge of the PWM switching signal is used to trigger a timer with a preset value of half of its switching intervals during both on and off periods. The average value of two samples is used as the instantaneous averaged value of the current sampling period and is used for the current regulation and current sharing control of the digital current controller.

IV. SIMULATION VERIFICATION

Fig. 9 shows the simulation results of output voltage and phase currents for load current step down without and with feedback control. By using the interleaved PWM scheme, the inductor current ripple could be reduced. Table II shows the typical parameters of a designed four-phase VRM converter. The load current is changed from a light load of 0.95A to a heavy load of 25A. It can be observed that the current response is about four sampling periods of the digital current controller. Fig. 10 shows simulation results of phase current response in steady state with unmatched converter parameters. It can be observed that the current derivation due to unmatched parameters can be reduced by using a designed digital current sharing control scheme.

V. CONCLUSION

This paper presents the design and realization of a digital current control technique for digital VRM controller used for high-performance microprocessors. A digital over-sampling with double-edge modulation technique has been developed to improve the current response of a multi-phase interleaved synchronous buck converter. The proposed digital current control scheme has been verified by using co-simulation with MATLAB and Modelsim with FPGA based fully-digital circuit realization. The experimental verification of the proposed digital control technique will be carried out in future research works.

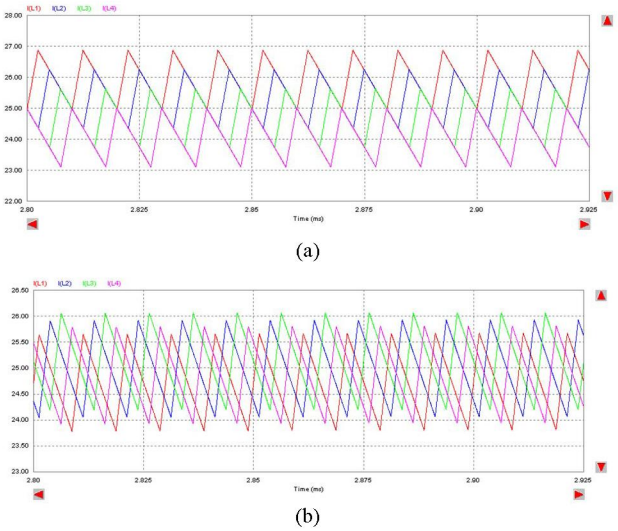

Fig. 10. Simulation results of phase current response in steady state with unmatched converter parameters under (a) open-loop control, and (b) closed-loop control.

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