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BRIEF PAPER

A Design of CMOS Class-E Power Amplifier with Phase Correction for Envelope Elimination and Restoration (EER)/Polar Systems

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SUMMARY A circuit technique to correct V_{dd}/PM distortion and improve efficiency as supply modulation of cascode class-E PAs has been proposed. The experimental result shows that the phase distortion can be improved from 20 degrees to 5 degrees. Moreover, a system co-simulation result demonstrated that the EVM can be improved from −17 dB to −19 dB.

key words: *envelope elimination and restoration (EER), polar system, class-E power amplifier, orthogonal frequency division multiplexing (OFDM)*

1. Introduction

The class-E power amplifier achieves 100% drain efficiency theoretically and is a good candidate for envelope elimination and restoration (EER) or polar transmitters. Considering reliability issues of PAs in CMOS process technology, a cascode topology of class-E power amplifier has been presented and shows the significant performance [1]. In EER or polar systems, the modulated signal is decomposed into the envelope signal and the phase signal. The phase signal is used to drive the class-E PA to be operated as a switch while the envelope signal modulates the supply voltage of PA. In theory, the class-E PA can adequately recombine both envelope and phase signals. However, a cascode class-E PA introduces undesired V_{dd}/AM and V_{dd}/PM distortions due to supply modulation. As mentioned in [2], V_{dd}/AM distortion is small enough to be neglected but, on the other hand, V_{dd}/PM distortion results in significant nonlinear phase shift in the supply voltage range. This nonlinearity will be damaging to the modulation accuracy of signal transmission. Since this effect is due to the variation of drain to source capacitance and drain to source conductance [2], a circuit technique to attain the constant drain to source impedance is proposed which can correct the V_{dd}/PM distortion to meet the system requirement. Detailed description of this technique is elaborated in Sect. 2. Section 3 shows the comparison of the simulation and measurement results. Moreover, a system co-simulation with orthogonal frequency division multiplexing (OFDM)-based signal has been established to demonstrate that this circuit technique for V_{dd}/PM distortion correction can effectively improve system error vector magnitude (EVM) performance. Finally, Sect. 4 draws conclusions.

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2. Circuit Principle and Design Methodology

2.1 Circuit Principle

Figure 1 shows the schematic of the class-E PA. The gate voltage of the transistor M_2 is generally biased at supply voltage V_{dd} or a fixed voltage V_{dc} and the inductor L_3 and capacitor C_3 are added to improve the efficiency [1].

In practice, due to supply modulation the variant condition of the transistor M_2 leads to a non-constant drain to source voltage function of the transistor M_2 and, then, varies the drain to source impedance ($Z_{DS2} = |V_{DS2}/I_{DS2}|$) of the transistor M_2, where V_{DS2}, I_{DS2} means drain to source voltage and drain to source current of the transistor M_2, respectively. Furthermore, the variable impedance results in the V_{dd}/PM distortion as supply modulation. During modulating the supply voltage of PA, the operating conditions of the transistor M_2 are inferred as follows:

1. When $V_{dd} < (V_{dc} - V_{th})/(V_{d2,max}/V_{dd,max})$, the transistor M_2 induces the strong inversion channel layer for current conducting but only occupies extremely small drain to source voltage headroom, where $V_{dd,max}$=1.8 V and $V_{d2,max}$ is the peak drain voltage of the transistor M_2.

2. Until $V_{dd} \geq (V_{dc} - V_{th})/(V_{d2,max}/V_{dd,max})$, it would be large enough to completely turn on the transistor M_1 and, hence, the transistor M_2 could have the ability of current driving and get the significant voltage headroom.

The relationship of impedance and voltage of the transistor M_2 can be found in Fig. 2. This simulation result shows that the non-constant voltage V_{DS2} would apparently vary drain to source impedance Z_{DS2}. Furthermore, the voltage waveform at carrier frequency on the drain node of

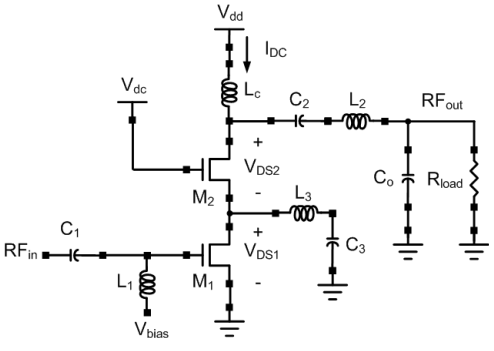

Fig. 1 A cascode class-E power amplifier.

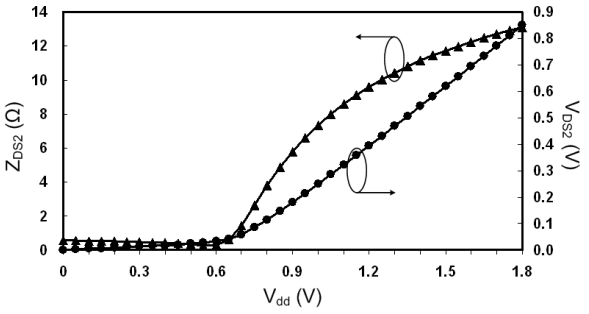

Fig. 2 The simulation result of Z_{DS2} and V_{DS2} as supply voltage variations.

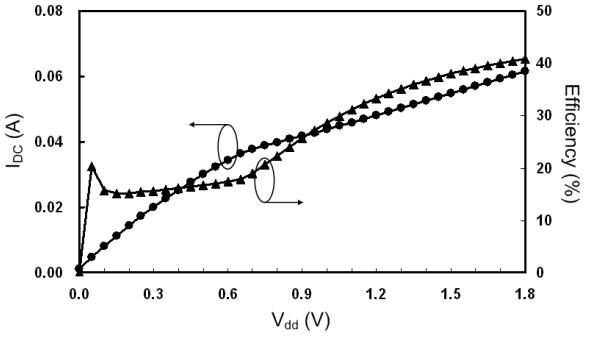

Fig. 3 The DC current (I_{DC}) and efficiency of the PA.

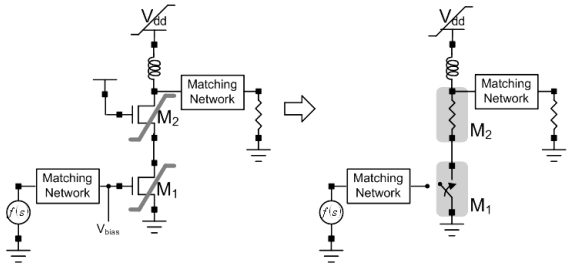

Fig. 4 The equivalent model of proposed cascode class-E PA.

the transistor M_2 would suffer from the phase shift due to the non-constant impedance Z_{DS2}. Then, the output signal would accompany the phase shift from drain voltage of the transistor M_2. This phase shift is called V_{dd}/PM distortion.

In addition, the other impact on the PA due to the non-constant voltage is the drain efficiency reduction. Figure 3 shows the simulation results of DC current and drain efficiency. In small supply voltage range, DC current increases rapidly and, hence, results in a serious reduction in efficiency. Unfortunately, this efficiency property is not suitable for polar applications.

2.2 Design Methodology

A design methodology which can correct the V_{dd}/PM distortion and improve the efficiency is proposed in this paper. Since the variable impedance induces the nonlinear phase shift, the constant impedance Z_{DS2} is expected to cancel this distortion effect. Figure 4 shows the equivalent model of

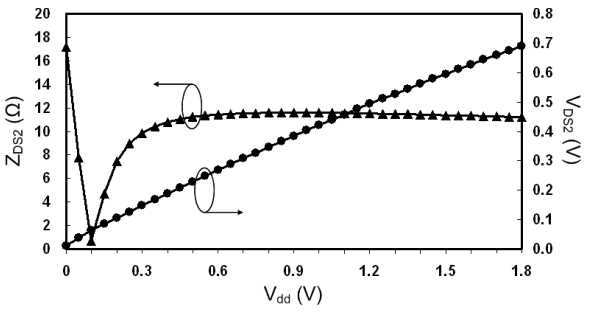

Fig. 5 The simulation result of Z_{DS2} and V_{DS2} of proposed PA as supply voltage variations.

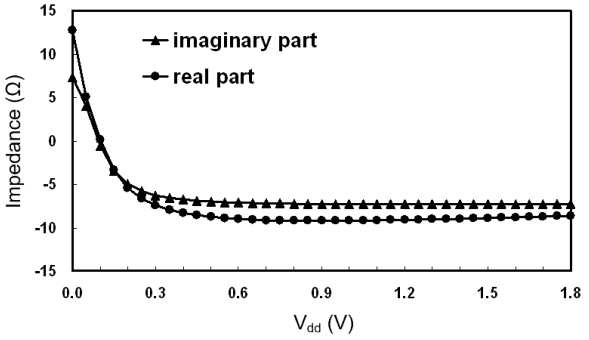

Fig. 6 The real part and imaginary part of drain to source impedance of the transistor M_2.

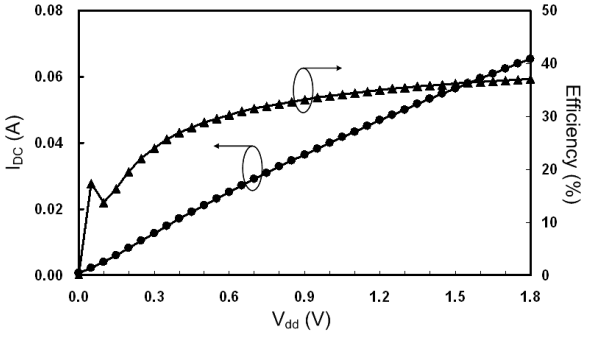

Fig. 7 The I_{DC} and improved efficiency of proposed cascode class-E PA.

proposed cascode class-E PA, in which the transistor M_1 is operated as a switch and the transistor M_2 is degenerated into a resistance. The simulation result of Z_{DS2} and V_{DS2} as shown in Fig. 5 shows that the voltage V_{DS2}, indeed, develops the almost constant impedance Z_{DS2}. The voltage V_{DS2} and constant impedance Z_{DS2} would be beneficial for supply modulation of the PA. For more detail of this analysis, the simulation result of the real part and imaginary part of drain to source impedance of the transistor M_2 is shown in Fig. 6. It demonstrated that the expected impedance, the almost constant real part and imaginary part of the drain to source impedance, can be achieved when the transistor M_2 has been degenerated into a resistance.

The more gain of the degenerative transistor M_2 is to pull up PA drain efficiency in small voltage range of V_{dd} and,

therefore, can extend the operating voltage range as supply modulation. This obtained property of drain efficiency is further serviceable for EER/polar systems. The simulation result of improved efficiency can be found in Fig. 7.

As shown on Eq. (1), when the PA with or without V_{dd}/PM distortion correction technique operates on the identical condition of P_{out} and V_{dd}, the efficiency would have an inverse proportion of I_{DC}.

$$\text{Efficiency} = \frac{P_{out}}{P_{DC}} \times 100\% \propto \frac{P_{out}}{V_{dd}I_{DC}} \propto \frac{1}{I_{DC}} \quad (1)$$

Comparing the result of Fig. 3 and Fig. 7, in small supply voltage range the PA with V_{dd}/PM correction can have the lower I_{DC} value and, hence, the efficiency of PA can be improved by 15%. The proposed technique flattens the drain efficiency curve and, therefore, is beneficial for EER/Polar systems.

3. Simulation and Measurement Results

The simulation result of V_{dd}/PM response in Fig. 8 shows that the output signal phase shift of PA can be improved from 20 degrees to less than 5 degrees in 0.3 V to 1.8 V of supply voltage V_{dd}. It exhibits that the proposed technique could evidently reduce the output signal phase shift.

Therefore, the small phase shift variations can extend the supply voltage range of PA in EER/Polar systems. The cascode class-E PA has been implemented using 0.18-μm CMOS process technology as shown in Fig. 9 and its area is $1.25 \times 1.3\,\text{mm}^2$. The measured result as shown in Fig. 10 reveals that the PA with V_{dd}/PM distortion correction technique can improve the output signal phase shift from 30 degrees to 6 degrees in 0.4 V to 1.8 V of supply voltage V_{dd}. As V_{dd} below 0.5 V, the serious output signal phase shift due to the transistor M_1 switching incompletely, may have severe degradations in system performances and, hence, the operating voltage above 0.5 V is recommended for EER/polar applications [2]. In Fig. 10, the result, meanwhile, represented that the proposed V_{dd}/PM distortion correction technique indeed decreases the output signal phase shift and, on the other hand, it demonstrated that the measured result is close to the simulation result.

Furthermore, a system co-simulation platform of EER architecture has been established to manifest the influence of V_{dd}/PM effect of cascode class-E PA on system per-

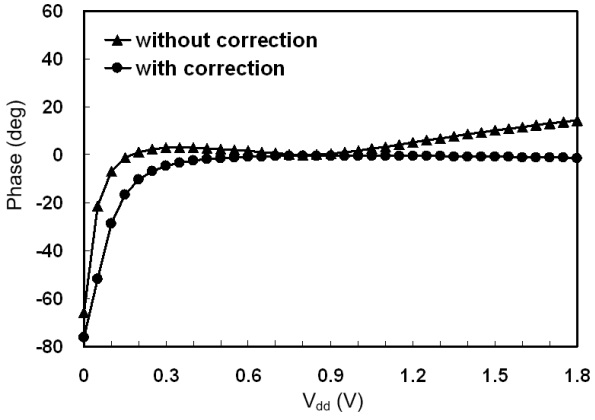

Fig. 8 The simulation results of V_{dd}/PM response of cascode class-E PA.

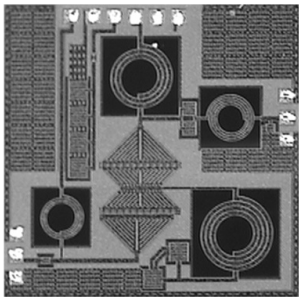

Fig. 9 Die micrograph.

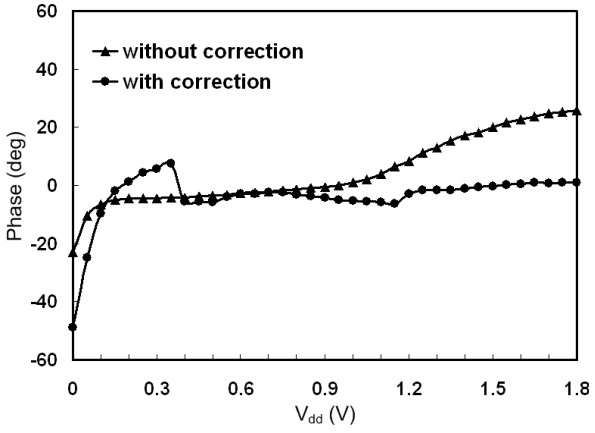

Fig. 10 The measured result of V_{dd}/PM response of cascode class-E PA without and with correction technique.

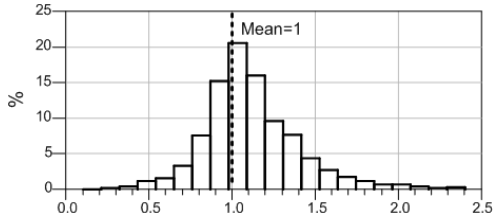

Fig. 11 Histogram of the envelope voltage.

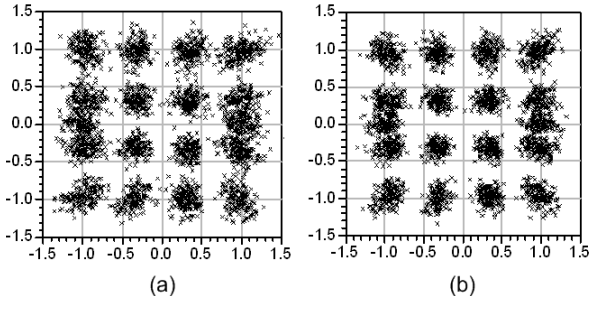

Fig. 12 Received constellation (a) without correction, (b) with correction.

formance. The signal source, IEEE 802.11a-like broadband OFDM transmission having 20 MHz bandwidth and operating at 2.6 GHz frequency band, is generated by ADS Ptolemy simulator. The histogram of envelope signal shown in Fig. 11 has 93% in the range from 0.5 to 1.8 V and the mean voltage is 1 V while the requested time delay is 2.8 ns [3]. With a V_{dd}/PM distortion correction technique of cascode class-E PA, the EVM can be improved from −17 dB to −19 dB and received constellation is shown in Fig. 12.

4. Conclusions

The technique, degenerating M_2 into a resistance, which can effectively correct the V_{dd}/PM distortion has been proposed. Moreover, the technique can improve the drain efficiency of the PA and extend the supply voltage range of the PA for EER/Polar systems. The measured result of V_{dd}/PM response has a good agreement with the simulation result. And, the system co-simulation result demonstrated that the proposed technique improves system EVM performance effectively.

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