國立交通大學

材料科學與工程學系

博士論文

無電鍍沉積薄膜應用於鉛錫擴散阻障層之研究

Investigation of Electroless Deposited Films as the Diffusion Barrier of Pb-Sn Solder

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摘　　要

本研究以無電鍍與焊錫擴散鍵結等兩種製程，取代深次微米半導體金屬墊層(UBM)元件物理氣相沉積製程(PVD)階梯覆蓋性不佳的現象，使金屬墊層(UBM)仍具良好的元件鍵結附著力，並兼具擴散阻障、潤濕及保護作用，可達覆晶構裝低成本、高密度與優良電性的需求。

本研究進行無電鍍製程沉積實驗，其等向沉積成長元件之金屬墊層，可解決元件鍍膜階梯覆蓋性不佳的問題。首先在氮化鋁基板上製作無電鍍鎳/銅雙層線路及凸塊，由元素線掃描結果顯示，錫無法突破鎳層之阻絕，證實鎳層是一良好的擴散阻絕層；其次，本實驗以無電電鍍沉積技術（Electroless Plating）在矽晶基板上製作無電電鍍鈷磷（Co-P）合金薄膜，再以電鍍方式沉積錫鉛（Pb-Sn）銲料於其上，用以探討無電鍍鈷磷薄膜做為銅製程覆晶接合（Flip-chip Bonding，FC）凸塊底部金屬化（Under Bump Metallurgy，UBM）之應用可行性。*X* 光繞射（*X*-ray Diffraction，XRD）顯示無電鍍鈷膜主要應由非結晶與微晶（microcrystalline）混合組成。元素線掃描分析結果顯示，在錫、銅及鈷之相互擴散反應過程中，當做為潤濕層的銅被完全消耗掉

之後，錫仍只在鈷磷鍍層與銲錫的界面處；經 250°C、24 小時之熱處理後，錫無法穿透鈷磷層的阻擋，而底層的銅亦無法擴散至銲錫層中，證實無電鍍鈷磷層可同時做為銅導線與銲錫凸塊之擴散阻障層（Diffusion Barrier），而其阻擋能力主要由高磷含量之初鍍鈷層形成之非晶質結構所提供。進行無電鍍鎳、銅與氮化鋁基板之拉桿黏著強度試驗，顯示鎳和銅之間黏著力亦大於 761 kg/cm^2，皆符合電路元件之黏著強度之要求。以無電電鍍搭配微影成像及蝕刻技術，在基板上製作無電鍍鎳或鈷/銅雙層線路及凸塊；另藉由電鍍方法沉積錫鉛於無電鍍鎳/銅上，用以模擬鎳銅凸塊與銲錫球產生之界面反應，無電鍍法所沉積的鎳磷(Ni(P))與鈷磷（Co(P)）薄膜具有良好階梯覆蓋性，可同時做為銅製程之銅導線與銲錫凸塊之擴散阻障層，此 Ni 或 Co 層阻擋能力主要由高磷含量之鈷層形成之非晶質結構所提供。

本研究另提出擴散接合的製程，乃一種低溫金屬銲錫擴散鍵結的構裝接合技術，這篇論文便研此新穎的構裝接合技術，將多層薄膜 Cu/Ti/Si 與 Au/Cu/Al_2O_3 在攝氏 250 度至 400 度間以焊錫鍵結，實驗研究結果顯示在結合界面將產生金屬界面化合物 η-$(Cu_{0.99}Au_{0.01})_6Sn_5$ 與 δ-$(Au_{0.87}Cu_{0.13})Sn$，此金屬界面化合物的成長受限於擴散控制，可減少焊接的缺陷產生(如凝結裂縫或氣孔等)，而且期抗拉強度可達 132 kg/cm^2 ，達無鉛構裝產業應用價值。

依據這些實驗結果顯示無電鍍與焊錫擴散接合法確實是光電半導體覆晶金屬墊層可應用的優良技術。

Investigation of Electroless Deposited Films as the Diffusion Barrier of Pb-Sn Solder

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Abstract

Under bump metallization (UBM) provides good adhesion between the bonding pads and the bumps, and serves as a diffusion barrier, wetting, and protective layer for flip-chip bonding. Both Au and Cu are so-called fast diffusers in Sn, and can diffuse very long distances in Sn in a relatively short time.. All of UBM metals are in general deposited by physical vapor deposition (PVD). However, as being used in the recent deep sub-micron Cu-IC process, the PVD suffers from poor step coverage. Numerous efforts have been made to solve this difficulty.

To solve the step coverage problems, a new idea was provided that the diffusion barrier layer in the Cu-IC process can be formed by using an electroless plating method. At first, the application of electroless copper/nickel (Cu/Ni) films on aluminum nitride (AlN) substrates was explored. The Ni film remained a mixture of amorphous and microcrystalline structures, and the Cu film was polycrystalline. Subsequent Pb-Sn solder bumping experiments indicated the amorphous Ni(P) film was a good diffusion barrier layer since Sn could not diffuse through it. The electroless Ni(P) layer has a step coverage and simultaneously serve as a diffusion barrier of Cu interconnects and UBM structure of flip-chip Cu-ICs. Pull-off tests revealed that the Cu/Ni films strongly adhered on both types of AlN substrates and that the adhesion strength exceeded 761 kg/cm^2. Next, electroless plating technique was utilized to prepare the cobalt-phosphorous Co(P) thin film to serve as the diffusion barrier layer of lead-tin solder. The *x*-ray diffraction (XRD) in conjunction with composition analyses revealed that the electroless Co(P) layer was a mixture of amorphous and nanocrystalline structures. The fact that Sn and Cu underlayer could not penetrate Co layer after such a liquid-state annealing evidenced that the Co(P) layer may simultaneously serve as a diffusion barrier interlayer dielectrics and UBM for flip chip copper (Cu) ICs.

The multi-layer thin-film systems of Cu/Ti/Si and Au/Cu/Al_2O_3 were diffusion-soldered at temperatures between 250°C and 400°C by inserting an Sn thin-film interlayer. Experimental results showed that a double layer of intermetallic compounds η-$(Cu_{0.99}Au_{0.01})_6Sn_5$/$\delta$-$(Au_{0.87}Cu_{0.13})Sn$ were formed at the interface. Kinetics analyses reveal that the growth of intermetallics was diffusion-controlled. The activation energies as calculated from Arrhenius plots of the growth rate constants for $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ are 16.9 kJ/mol and 53.7 kJ/mol, respectively. The satisfactory tensile strength of 132 kg/cm^2 could be attained under the diffusion bonding condition of 300°C for 20 min for Cu/Ti/Si and Au/Cu/Al_2O_3.

Results in these experiments demonstrate that electroless plating and diffusion soldering are indeed excellent technology for UBM structure of flip-chip ICs.

Acknowledgements

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Chapter 1 Introduction

1.1 Motivation

In recent years, the state-of-the-art semiconductor related techniques have developed rapidly and competitively. All the leading manufacturers have made efforts in developing IC components with lower costs, smaller sizes, and higher performances. In addition to the leading technologies for 12-inch silicon wafer and deep sub-micron fabrication, the package technology has become a more important issue as well. Conventional package techniques such as lead frame package (LFP), ball grid array (BGA) package, and tape automatic bonding (TAB) package have been improved to allow IC components to have smaller sizes, higher throughput and better performances. Today, there are at least three popular chip-level connections, namely, face-up wire bonding, face-up tape-automated bonding, and flip chip. Among these three technologies, flip chip provides the highest packaging density and electronic performance and the lowest packaging profile which will meet the demand for packaging at ever higher frequencies. Therefore, more and more companies and universities have devoted themselves to the development of flip chip packaging for semiconductor. The flip chip interconnect is based on three fundamental building blocks, the bumps on the chip, the substrate and the method to attach the chip to the substrate. Among the various types of bumps, the solder bump is by far the most common and reliable for Flip Chip bonding, especially the eutectic lead/tin solder.

Ceramic material has excellent characters of heat conduction and electric insulation, and the characters can be adjusted by modulating its chemical compositions, so the application of ceramic material is very extensive in electric package; it not only is the common material of interposer and seal cap, but also can be used to fabricate Multilayer Interconnection Substrate for high density package when cooperating with thick film metallization process. Aluminum oxide (Al_2O_3) and aluminum nitride (AlN) are common material of ceramic package substrate; wherein AlN has Wurtzite structure, so AlN substrate has better heat conductivity (AlN: 230 W/m°K, Al_2O_3: 20 W/m°K, Si: 150 W/m°K, GaAs: 50 W/m°K), lower dielectric constant (in 1MHz, AlN: 8.8, Al_2O_3: 8.5), approximate thermal expansion coefficient with GaAs (AlN: 4.5 ppm/°K, Al_2O_3: 7.3 ppm/°K, Si: 2.6 ppm/°K, GaAs: 5.73 ppm/°K), and better electrical and mechanical properties; moreover, it is compatible with all thin/thick film metallization process. Aluminum nitride is an important substrate material for electronic packaging due to its good electrical, mechanical and heat conduction properties. It not only serves as a good heat sink for GaAs MHEMTs, but also hosts all the passive circuit components such as transmission lines, resistors, capacitors.

Under bump metallization (UBM) provides good adhesion between the bonding pads and the bumps, and serves as a diffusion barrier, wetting, and protective layer for flip-chip bonding. There are mainly four types of diffusion barrier layer: sacrificial barriers, stuffed barriers, passive compound barriers and amorphous barriers. [1] The most common materials used in UBM as diffusion barrier layer are refractory metals, such as titanium (Ti), tungsten (W), and molybdenum (Mo), and the alloy thereof. All of these metals have superior diffusion barrier capability at high temperatures and are in general deposited by physical vapor deposition (PVD). However, as being used in the recent deep sub-micron Cu-IC process, the PVD suffers from poor step coverage. Numerous efforts have been made to solve with this difficulty, which comes up with the idea that the diffusion barrier layer in the Cu-IC process can be formed by using an electroless plating method[2,3] and presently the electroless plated nickel (Ni) is most commonly adopted for UBM [4-7].

Because the PVD suffers from poor step coverage, numerous efforts have been made to solve this difficulty. Electroless plating is based on the theorem of oxidation-reduction, making metal proceed selective deposition on the wanted plating surface. The Electroless plating technology on the surface coverage of tradition metal device has been applied for a long time, and is tried to apply on the semiconductor wafer fabrication to reduce fabrication cost and improve the competitiveness; the main character of electroles plating is that it can process a great deal of wafers, such as 25pcs or 50pcs in the same time by using cassette, to relatively reduce the whole process time. So far electroless plating technology has been widely applied to electronic industry due to it simple process and low cost features. Nickel (Ni) and cobalt (Co) are the most common metals that could be deposited using electroless plating process. The electroless metal has been utulized as a diffusion barrier for multilayer microelectronic structure, it is also a good barrier metal to inhibit the interdiffusion between the solder bump and metallization of integrated circuits (ICs). This technique easily allows the parallel processing of multiple wafers so that it can lead to a high throughput. Therefore the electroless process is a promising technology for flip chip packaging applications because a low cost is always a key issue in production. To solve the step coverage problems, the electroless plating method was provided.

Diffusion soldering (also known as solid-liquid interdiffusion bonding) is a novel joining technique based on the principle of isothermal solidification. A low melting, metallic thin-film interlayer is employed in the process, which melts at low temperatures and reacts rapidly with both high-melting (HT_1 and HT_2) layers or substrates to form intermetallic compounds (IMs). Since the intermetallic compounds formed at the interfaces possess much higher melting points than the original low-melting interlayer, a special feature of bonding at lower temperatures and usage at higher temperatures can be achieved [8]. Such a superior characteristic enables diffusion soldering to broaden its application potentials in the electronics industry [9-11].

1.2 Thesis Outline

According to the underlying principle of the diffusion soldering process, it is obvious that interfacial reactions play a key role in the joining efficiency of this technique. The effort of this study is thus concerned with the intermetallic compounds formed at the interfaces and their growth kinetics during the diffusion soldering of the multi-layer thin-film systems bonded onto Si wafers and Al_2O_3 substrates. In addition, the tensile strengths of the diffusion-soldered specimens are evaluated. In the chapter 4-1, I studied thin-film reactions during diffusion soldering of Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers. The multi-layer thin-film systems of Cu/Ti/Si and Au/Cu/Al_2O_3 were diffusion-soldered at temperatures between 250°C and 400°C by inserting an Sn thin-film interlayer. Experimental results showed that a double layer of intermetallic compounds η-$(Cu_{0.99}Au_{0.01})_6Sn_5/\delta$-$(Au_{0.87}Cu_{0.13})Sn$ was formed at the interface. Kinetics analyses revealed that the growth of intermetallics were diffusion-controlled.

In recent years, the fabrication techniques for both ultra large scale integrated circuits (ULSI) and liquid crystal displays (LCDs) tend towards lower temperatures in order to avoid degradation of the device characteristics due to the thermal stress on the thin films. Owing to novel low-temperature related techniques, various low melting-point substrates such as glass substrates and plastic substrates are suitable for use in growth of high-quality thin films with low thermal stress at low temperatures. In the chapter 4-2, we studied the electroless copper/nickel (Cu/Ni) films deposited on aluminum nitride (AlN) substrates applied to high-frequency power GaAs device packaging. Experimental results showed metal films deposited on polished AlN surfaces possess flatter surface, finer grain structure, and lower resistivity than those on unpolished surfaces. The Ni film remained a mixture of amorphous and microcrystalline structure, and the Cu film was polycrystalline. Subsequent Pb-Sn solder bumping experiments indicated the amorphous Ni(P) film was a good diffusion barrier layer since Sn can not diffuse through it.

Since the capability of electroless Co(P) as a barrier layer in UBM structure is yet to explore, we hence carried out this study in order to investigate its feasibility to serve both as the barrier layer of interlayer dielectrics and UBM for flip-chip Cu-ICs. The chapter 4-3 tried to explain the investigation of electroless cobalt-phosphorous layer and its diffusion barrier properties of Pb-Sn solder. The capability of cobalt-phosphorous (Co(P)) layer, which was grown *vi*a electroless plating process, to serve as the diffusion barrier of lead-tin (PbSn) solder was investigated. The *x*-ray diffraction (XRD) in conjunction with composition analyses revealed that the electroless Co(P) layer was a mixture of amorphous and nanocrystalline structures; however, AES depth profile and subsequent analysis indicated that the first formed Co(P) layer should be amorphous since it contains as high as 18 *at*.% P. This implied a good barrier capability for electroless Co(P) that, as revealed by EDX line scan, the Sn and Cu atoms could not penetrate the Co(P) layer after the PbSn/Cu/Co(P)/Cu/Ti/Si sample was subjected to annealing at 250°C in forming gas ambient for 24 hrs. The electroless Co(P) mainly behaves as a sacrificial diffusion barrier. Experimental analysis indicated that electroless Co(P) could also be a stuffed barrier since the P element residing at the boundaries of nano-grains simultaneously offer the barrier capability. The combined barrier property of electroless Co(P) evidenced that it could be a potential barrier layer in UBM structure of flip-chip Cu-ICs.

Finally, the conclusion and suggestion for future research are given in the chapter 5.

Chapter 2 Literature Review

2-1 Diffusion soldering

Diffusion soldering is a useful joining technique at low temperatures in metal welding. For the manufacturing of a ceramic multi-chip modulus, Si dice are attached to multi-layer ceramic substrates [12]. The bonding temperature for this die attachment process must be lower than 400°C to avoid any damage to IC chips. Polymer adhesives, glass bonding, metallic soldering and Au-Si eutectic bonding are the traditional methods applied for this purpose. However, this causes strength degradation in the joining interfaces when the IC chips are functioning at elevated temperatures. Given the advantage of the diffusion soldering technique in pairing high operation temperature with low bonding temperature, its applicability in die attachment for high-density ceramic packages is hence examined.

2-2 Electroless Ni plating

Flip chip provides the highest packaging density and electronic performance and the lowest packaging profile which will meet the demand for packaging at ever higher frequencies. Electroless plating technology has been widely applied in the electronic industry due to it simple process and low-cost features. Nickel (Ni) is the most common metal that could be deposited by the electroless plating process. It is also a good barrier metal for inhibiting interdiffusion between the solder bump and metallization of integrated circuits (ICs). [13-15] Brenner was the first to propose a chemical reduction mechanism related to hydrogen atom absorption. The atomic hydrogen produced by hypophosphate adheres to the catalyzed surface, reducing nickel ions to metal nickel and combining two hydrogen atoms to become hydrogen gas. Besides this mechanism proposed by Brenner, there are different theories. [16-18] Under bump metallization (UBM) is required for solder bumping to provide adhesion/diffusion retardation between the bonding pads of the die and the bumps, solder wetting, and oxidation prevention. [19,20] Electroless Ni (EN) plating has been used for both UBM deposition and bump formation for flip chip applications. [21-23] Nickel has a relatively low diffusion rate and reaction rate with solder, thus it is a suitable UBM for solder bumps. The UBM with 5 μm Ni in thickness provides good reliability with solder bumps. The low-stress status of EN is more advantageous than that of Ni produced by sputtering. [24] Amorphous EN Ni has no grain boundaries for diffusion and exhibits good barrier properties. Furthermore, EN plating is a selective chemical deposition method and can reduce the bumping cost significantly since it does not require masking or metal sputtering. [23]

Nickel has a relatively low diffusion and reaction rates with solder and the Ni layer with 5 μm in thickness provides suitable reliability for UBM applications. Further, the low stress status of electroless Ni is more advantageous than that of Ni prepared by sputtering[24]. Since the plating baths for electroless Ni in general contain sodium hypophosphite (NaH_2PO_2) as the reducing agent, phosphorus (P) atoms are deposited simultaneously so that electroless Ni is in fact a nickel-phosphorous alloy (Ni(P)). It is known that the phosphorous content in Ni(P) can be adjusted by the pH value of plating bath and the crystalline structure of Ni(P) changes with the phosphorous content[7.25]. The mixture of microcrystalline and amorphous grains constitutes the Ni(P) when phosphorous content is in the range of 7 to 10 *wt*.%; when phosphorous content exceeds 10 *wt*.%, the Ni(P) layer becomes amorphous. The amorphous electroless Ni(P) possesses good barrier property due to the non-existence of fast diffusion paths such as grain boundaries.

2-3 Electroless cobalt plating

Electroless cobalt-phosphorous alloy (Co(P)) serving as the diffusion barrier of Cu and polyimide dielectrics in multilayer microelectronic structure has been studied by O'Sullivan *et al*[26]. Their investigation showed that electroless Co(P) is highly effective to inhibit Cu diffusion at elevated temperatures, even at Co(P) thickness as low as 50 nm. The electroless Co(P) also exhibited a better diffusion-barrier effectiveness in comparison with Ni(P) and pure metals (Co, Ni). The study of electroless Co(P) further indicated that the phosphorous codeposition behaviors and its effects on the crystalline structure of Co(P) are similar to that of electroless Ni(P). Binary phase diagrams revealed a relativity low solubility of Sn or Pb in Co[27], it can thus be speculated that electroless Co(P) should possesses good barrier capability for UBM applications.

There are studies about applying electroplated or PVD Co in UBM for solder bump [28,29]. Since the Co layers prepared by these methods are polycrystalline, either W or P elements were doped into the Co layer to clog up the grain boundaries and thereby improved the diffusion retardation ability. For instance, the alloy of $Co_{0.9}W_{0.02}P_{0.08}$ exhibited better barrier property in comparison with $Co_{0.9}P_{0.1}$ and was capable of withstanding annealing at 450°C[30,31]. However, the electroplating is not suitable for ceramic or organic substrates in the UBM process. The PVD methods such as sputtering are costly.

The under bump metallurgy (UBM) structure can be divided into adhesion layer, diffusion barrier layer, and wetting layer or anti-oxidation layer. According to Marc-Aurele Nicolet, the diffusion barrier can be classified into four categories: sacrificial barriers, stuffed barriers, passive compound barriers and amorphous barriers. [32] The most common materials used in UBM as diffusion barrier layer are refractory metals, such as titanium (Ti), tungsten (W), molybdenum (Mo) and their alloys, which have good adherence and superior diffusion-barrier capability. Conventionally, physical vapor deposition (PVD) such as sputtering is adopted to prepare the UBM structure. However, in recent sub-micron Cu-IC process, the thin films deposited by PVD suffers from poor step coverage. [33]

The electroless Co(P) exhibited superior barrier capability to counter the interdiffusion between Cu and interlayer dielectric (ILD) in the Cu-ICs in comparison with electroless Ni(P) that, for a thickness of only 50 nm, electroless Co(P) remained an effective diffusion barrier layer up to 400°C. [26] Moreover, it possesses a low sheet resistance, good step coverage, and has potential to replace conventional barrier layers for Cu-ICs, such as Ta, TaN, *etc.* [34] Our previous study confirmed that the electroless Co(P) film may also impede the interdiffusion between eutectic PbSn solder and Cu elements. [35] Previous studies[31,36,37] reported that the electroless Co(W,P) films containing 8 to 10 *at.*% of P are nano-crystalline; it is a mixture of nano-crystalline and amorphous structures when the P content is between 10 to 12 *at.*%; the films are entirely amorphous when the P content exceeds 12 *at.* %. According to the results presented above, the electroless Co(W,P) films prepared in present work become non-crystalline when the pH value approximately exceeds 8.6 or, the P content of the film is higher than 9 *at.*%. The Co(W,P) microstructure was in fact determined by the plating conditions, *e.g.*, the pH value of plating solution. Such a spherical granular surface morphology was attributed to the dispersed Pd-island clusters on activated substrate surface that initialize subsequent Co plating reaction[38]. During plating, the granules grew and coalesced with each other and thus the grain coarsening was observed with the increase of plating time. The researches [31,36,37] revealed the enhancement of thermal property and diffusion barrier capability of Co(W,P) films due to the existence of W element in the thin films.

Electrochemical reactions involved in electroless Co plating are given as: [39]

$$H_2PO_2^- \rightarrow (HPO_2^-)_{ads} + (H)_{ads} \qquad (1)$$

$$(HPO_2^-)_{ads} + OH^- \rightarrow H_2PO_3 + 2e^- \quad (2)$$

$$Co^{2+} + 2e^- \rightarrow Co \quad (3)$$

$$H_2PO_2^- + 2H^+ + e^- \rightarrow P + 2H_2O \quad (4)$$

Electrochemical reactions depicted by Eqs. (2) and (3) indicate that high pH values promote the electron release and hence the deposition of Co element. Paunovic *et al.* studies the effects of pH values on deposition rate of electroless Co(W,P) and found that the plots of deposition rate *versus* pH values of plating solution form concave-down curves, *i.e.*, the deposition rate first increases with the increase of pH values, reaches a peak rate and then decreases with further increase of pH values. Their study indicated that in high pH-value environment, the hydroxyl ions (OH^-) become the dominant factor on the kinetics of plating process by lowering its charge transfer coefficient (*i.e.*, the probability of combining electron and metal ion thereby triggering the plating), leading to the drop of deposition rate [40] Since OH^- ions are reactants in the charge-transfer step of the anodic partial reaction

$$(HPO_2^-)_{ads} + OH^- \rightarrow (H_2PO_3^-)_{ads} + H_{ads} + e^-$$

The spectra in the transmission electron microscope taken from the center of the individual grains did not show any evidence of phosphorous. However, when the electron beam was located at the triple point of grain boundaries, the phosphorous peaks were detected. [41] Thus, the phosphorous was significantly segregated to the grain boundaries.

Previous study reported the accumulation of P at the PbSn/Ni(P) interface due to the relatively low solubility of P in solder and, when the content of P was sufficiently enough, the Ni_3P IMCs might form.[42]

Chapter 3 Experimental

3-1 Experimental Method for Thin-Film Reactions during Diffusion Soldering of Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn Interlayers

Ever since IBM first started research on copper interconnection technology,[43-45] copper metallization has drawn considerable attention in the IC industry. For the diffusion soldering of Si with Al_2O_3 substrates, Ti (20 nm), Cu (6 μm) and Sn (4 μm) were sputter-deposited sequentially on a Si wafer. A Cu layer (4 μm) and an Au layer (6 μm) were also deposited on an Al_2O_3 substrate by sputtering. The specimens with dimensions of 4 mm x 4 mm were cut with a diamond saw. The surfaces of the specimens were stripped with a deoxidized agent prior to diffusion soldering in order to remove any oxide film. The multi-layer thin-film specimens were then sandwiched as shown in Fig. 3-1, and heated at various temperatures ranging from 250°C to 400°C in a vacuum furnace of 5.3×10^{-4} Pa. After diffusion soldering, the specimens were cross-sectioned, ground with SiC paper, and polished with 1 μm and 0.3 μm Al_2O_3 powders. Morphology observations and growth rate measurements of the intermetallic compounds were mostly conducted via a scanning electron microscope (SEM). Chemical compositions of the intermetallic compounds were analyzed using an electron probe microanalyzer (EPMA). For the evaluation of bonding strengths of the diffusion-soldered specimens, tensile tests were conducted using a microforce tester at a crosshead speed of 0.01 mm/s.

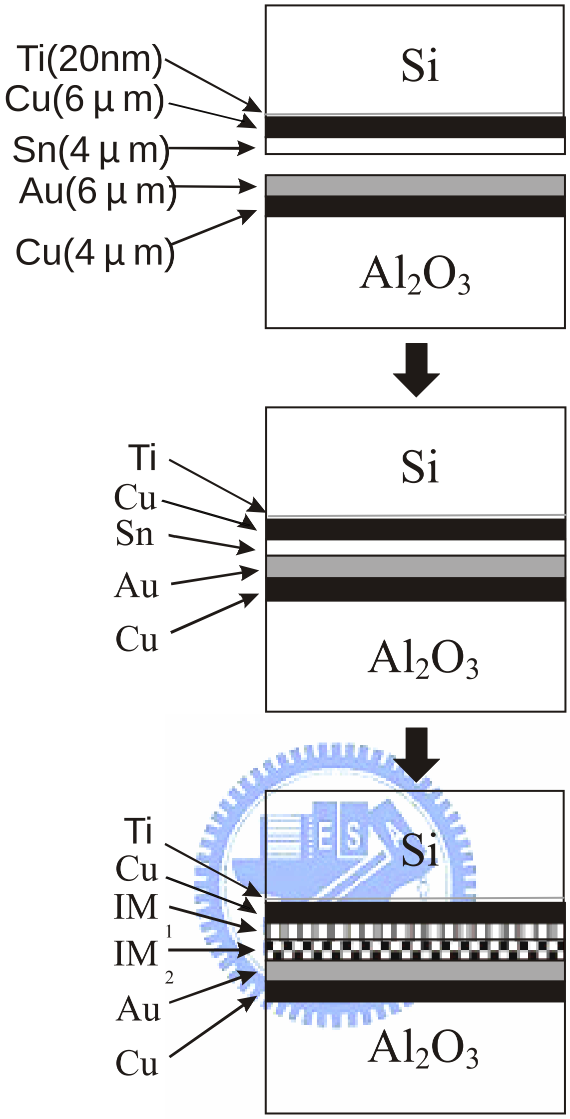


Fig. 3.1：The scheme of diffusion soldering for Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers.

3-2 Experimental Method for Electroless Copper/Nickel Films Deposited on AlN Substrates

3-2.1 Metallization of AlN substrates

Pretreatments of the surface of nonmetal substrates including roughening, sensitization, activation, and acceleration are necessary before electroless plating. [46-48]

Polished and unpolished AlN substrates provided by Stellar Industries were used in this work. Figure 3.2 shows the process flow of pretreatments and the metallization of AlN substrates. Firstly, the substrates were soaked in acetone and ultrasonically cleaned for 5 min to remove the contaminants and then etched in 4 wt% NaOH solution for 30 min. The substrates were further ultrasonically cleaned in deionized water to remove the solution residues, and then dried with helium gas. The surface roughness was evaluated using a surface profiler (KLA-Tencor P-10) and an atomic force microscope (AFM, Digital Instruments Nanoscope Ⅱ).

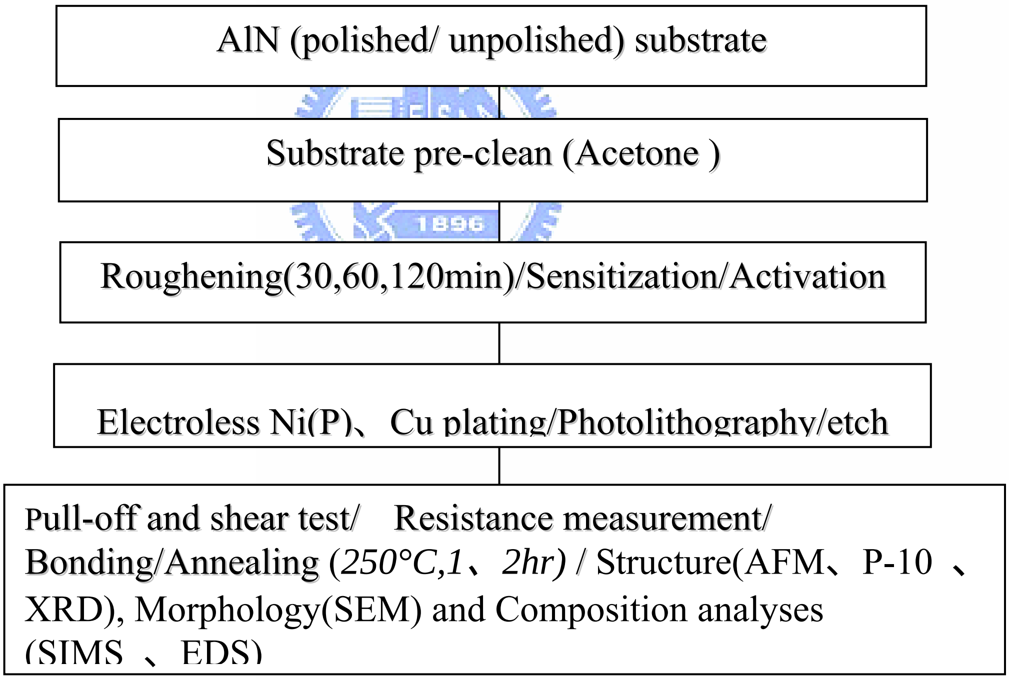


Fig. 3.2 Process flow of AlN substrate metallization [46-48].

The cleaned AlN substrates were then sensitized and activated with the solutions listed in Table 3.1. The EN plating was followed using the solution consisting of 132 ml/l

Slotonip 33 Ni solution, 0.8 ml/l (40%) Slotonip 36 stabilizer, 177 ml/l Slotonip 31 hypophosphite complexing agent and 690.2 ml/l DI water. The deposition was carried out at a temperature of 90°C and the pH of the solution was kept at 4.5. The deposition rate of the EN layer was approximately 21 μm/h.

Table 3.1. Compositions of sensitization and activation solution.

Steps	Composition	Concentration	Soaking time
Sensitization	$SnCl_2 \cdot 2H_2O$	10 g/l	10 min
	HCl	40 ml/l	
Activation.	$PdCl_2$	1 g/l	10 min
	HCl	20 ml/l	

The electroless Cu plating solution consisted of MACuShield 185A Cu solution, MACuShield 185B chelating agent, MACuShield 185D modifying agent, MACuShield 185G stabilizer and 37% formaldehyde reducer. During the deposition, the pH value was adjusted in the range of 12 to 13. The Cu layer deposition rate was approximately 4 μm/h.

3-2.2 Surface morphology and composition characterization

The metallized AlN substrates were observed using a Hitachi S-2500 scanning electron microscope and FEI FIB-200 focused-ion-beam (FIB) system. The composition of the Ni layers was analyzed with an energy-dispersive spectrometer attached to the scanning electron microscope as well as with a PHI Adept 1010 quadrupole secondary-ion-mass spectrometer. The crystal structure of deposited films was characterized by X-ray diffraction analysis (Siemens D-5000).

3-2.3 Pull-off test

A pull-off test was employed to measure the adhesion strength of the EN layer on AlN substrates. Studs of 2.54 mm diameter were firmly attached onto the specimens using epoxy resin and then sent to a SeBastian Five-A pull-off tester for adhesion measurement.

3-2.4 Shear test

Ni bumps of 100 μm in diameter and 30 μm in height were formed on the AlN substrate. The shear test was carried out with a DAGE 2400 shear tester.

3-2.5 Resistance measurement

The sheet resistance (R_s) of the plated metal layer was measured using Changmin Tech's CMT-SR 2000N four-point probe. The resistivity (ρ) of the metal layer was calculated according to the formula below within the known film thickness (t).

$$\rho = R_s \times t .$$

3-2.6 Flip chip bonding

Eutectic lead-tin (37Pb/63Sn) solder was used to bond chips on substrates for electrical connection. The metallization on the pad of the chip was Cu/TiW/GaAs and that on the substrates was Cu(2μm)/Ni(5μm)/AlN. The apparatus for flip chip bonding was a semiautomatic flip chip bonder (Suss FC 150) with a 1μm bonding accuracy. The solder bumps were grown on GaAs PHEMT devices. The bumped ICs were then bonded onto the metallized AlN substrates prepared according to a previously described method. The specimens were annealed at 250°C for various times and the microstructure evolution of the bonding interface was evaluated by scanning electron microscope (SEM)/ energy-dispersive spectrometer (EDS).

3-3 Experimental Method for Electroless Cobalt-Phosphorous Layer and Its Diffusion Barrier Properties of Pb-Sn Solder

3-3.1. Specimen Preparation

After forming simulated Ti/Cu circuit layer on the Si substrate by e-beam evaporation and then processed by roughening/sensitization/activation, the specimens were subjected to electroless plating of different periods of times for depositing Co(P) layer. Table 3.2 lists the methods and solutions for roughening, sensitization and activation. After the catalytic layer being formed on specimens, a Co(P) layer was deposited thereon by means of the electroless plating solution defined by Table 3.3, the pH of which was regulated by 3M NaOH. In this experiment, the plating condition was controlled as follows: pH value = 7.8±0.3, temperature = 75±2°C, V/A (ml/cm^2) $\geq$ 20 while the plating time was adjustable with respect to the required thickness. A surface profiler (KLA-TENCOR P-10) measured the thickness of Co(P) layer on substrates subjected to different plating time, and the plating rate was obtained. After the specimens were washed by DI water and then blew dry by a nitrogen jet, a Cu wetting layer of 800 nm and eutectic PbSn solder layer were sequentially deposited on. The PbSn/Cu/Co(P)/Cu/Ti/Si specimens were then sent to a furnace for annealing at 250°C in forming gas ambient (5% H_2-95% N_2) for 0, 0.5, 6, 18, 24 hrs, respectively. The flow of specimen preparation is summarized in Fig. 3.3.

Table 3.2. Solution for roughening, sensitization, activation and the immerse time.

Steps	Composition	Concentration	Immerse time
Roughening	H_2SO_4	5 *wt.*%	10 min
Sensitization	$SnCl_2 \cdot 2H_2O$	10 g/L	10 min
	HCl	40 ml/L	
Activation	$PdCl_2$	0.1 g/L	45 sec
	HCl	8 ml/L	

Table 3.3. Compositions of electroless plating bath.

Ingredient	Chemical	Concentration
Co salt	$CoSO_4 \cdot 6H_2O$	35 g/L
Reducing Agent	$NaH_2PO_2 \cdot H_2O$	40 g/L
complexing reagent	Na citrate	35 g/L
stabilizer	$(NH_4)_2SO_4$	70 g/L
pH Value Adjustment	NaOH	3M

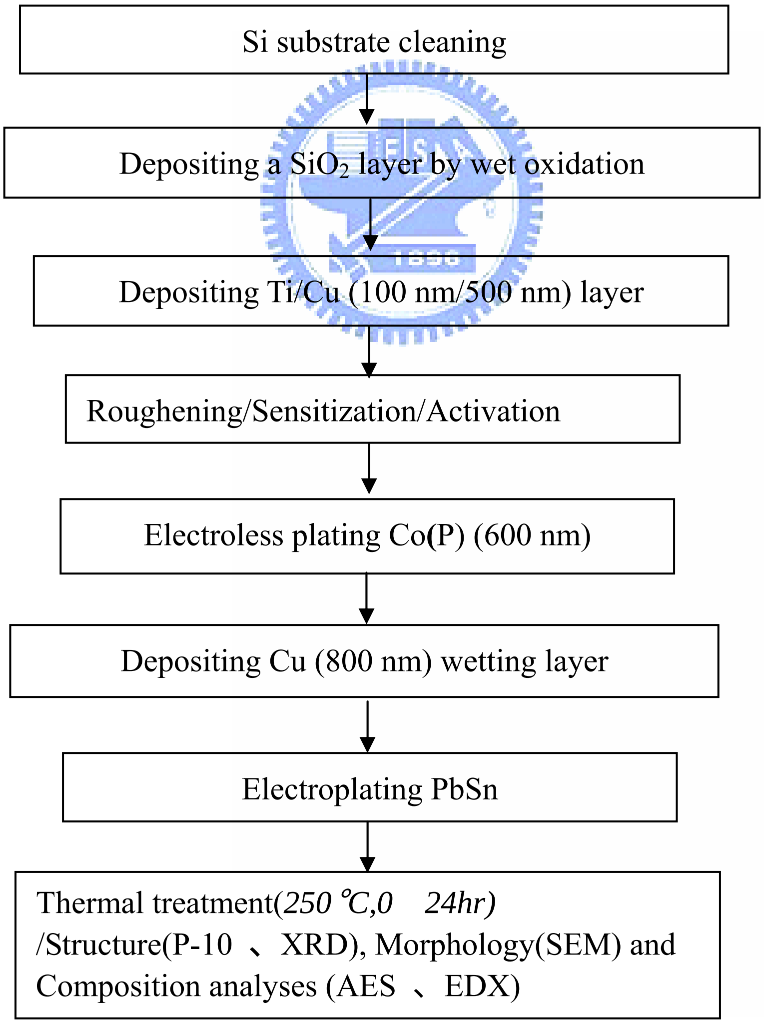


Fig. 3.3 Flow chart of Co(P) specimen preparation.

3-3.2. Structure, Morphology and Composition Characterization

The crystal structures of electroless Co(P) films were characterized by a *x*-ray diffractometer (M18 XHF, MacScience). The source of *x*-ray was Cu-K_α of 0.154 nm wavelength operated at 200 mA and 50 kV and the measurement was performed at a scanning rate of 4°/min.

Scanning electron microscopy (SEM, FE-SEM JSM-6500F or FE-SEM Hitachi S-4700) was adopted to examine the morphology and cross-sectional structures of each specimen. The composition analysis was performed using Auger electron spectroscopy (AES, VG350) and energy dispersive spectrometer (EDX, Oxford Inca Energy 300) attached to SEM. Further, the EDX line scan was adopted to analyze the composition change for cross-sectional specimens subjected to different durations of thermal treatment. The line scan start from the Cu layer of the substrate toward the PbSn solder while adopting at least four points of each specimen for analysis so as to obtain the average thereof for further discussion.

Chapter 4 Results and Discussion

4-1 Thin-Film Reactions during Diffusion Soldering of Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn Interlayers

The multi-layer thin-film systems of Cu/Ti/Si and Au/Cu/Al_2O_3 were bonded with Sn interlayers at various temperatures ranging from 250°C to 400°C. The typical morphology of the diffusion-soldered joints for the bonding of Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers is shown in Fig. 4.1. EPMA line profiles for Au, Sn, and Cu elements across the multi-layers of the diffusion-soldered specimen (see Fig. 4.1.) are plotted in Fig. 4.2. The Sn interlayer after diffusion soldering is eliminated and replaced by bilayered intermetallic compounds between Cu/Ti/Si and Au/Cu/Al_2O_3. The intermetallic compounds adjacent to the Cu layer have a chemical composition (at.%) of Cu:Au:Sn = 54.8:0.2:45.0, *i.e.*, $(Cu_{0.99}Au_{0.01})_6Sn_5$, which corresponds to the η-Cu_6Sn_5 phase on the Cu-Sn phase diagram. The η-Cu_6Sn_5 intermetallic phase has often been reported on in studies of Cu/Sn interfacial reactions [49]. During the Cu/Sn soldering reactions, η-Cu_6Sn_5 has been found to react further with Cu to form the ε-Cu_3Sn intermetallic compound, which might be too thin to be observed in this diffusion-soldering study.

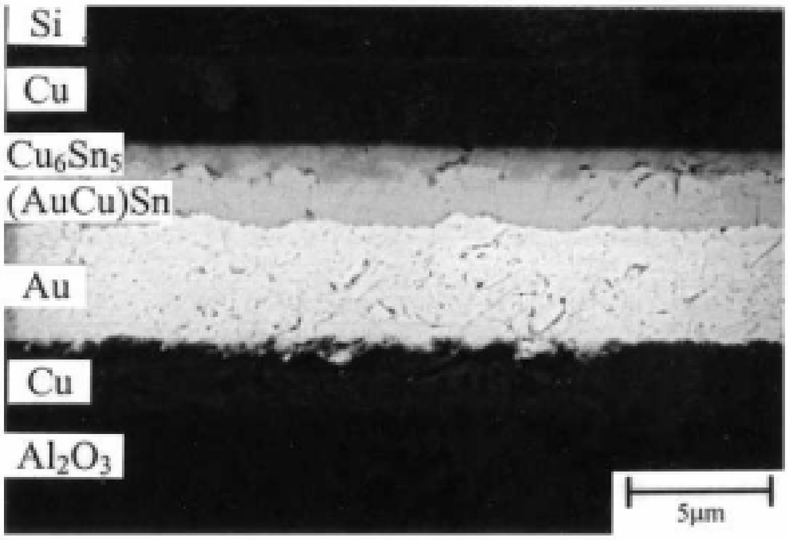


Fig. 4.1：The morphology of intermetallic compounds formed after diffusion soldering between Cu/Ti/Si and Au/Cu/Al_2O_3 at 300°C for 20 min with Sn interlayers.

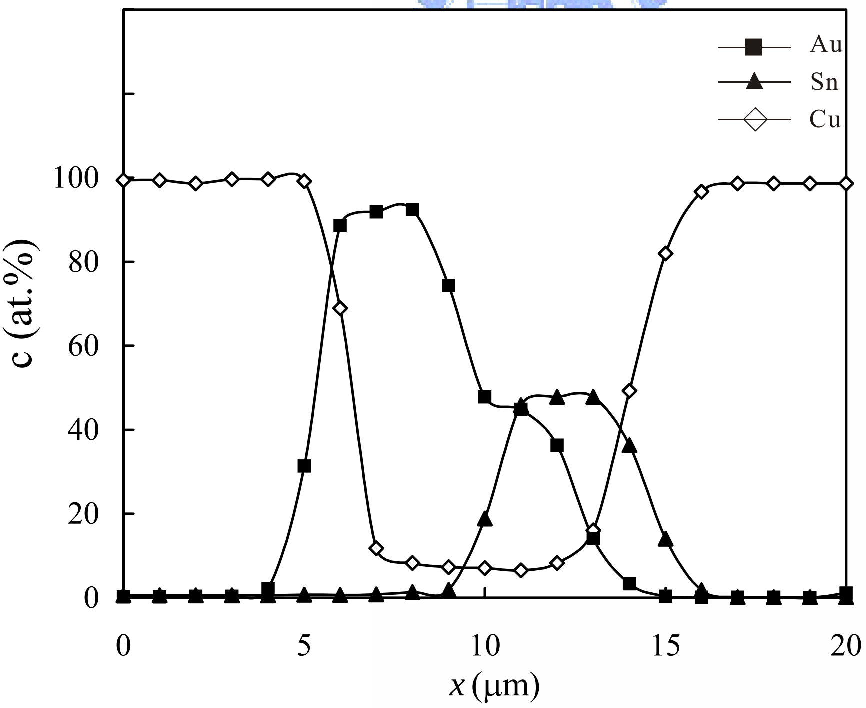


Fig. 4.2：The Au, Sn and Cu concentrations across the multi-layers of the diffusion soldered specimen (from Fig. 4.1).

The chemical composition of the intermetallic compound adjacent to the Au layer is Au:Cu:Sn = 44.4:6.9:48.7, *i.e.*, $(Au_{0.87}Cu_{0.13})Sn$, corresponding to the δ-AuSn phase on the Au-Sn phase diagram. The relatively high Cu content of this δ-AuSn intermetallic phase is attributed to the rapid diffusion of Cu into the Au layer in $Au/Cu/Al_2O_3$, which simultaneously participates in the interfacial reaction between Au and the Sn interlayer during the diffusion soldering process. For the soldering reaction between liquid Sn and the Au substrate, the interfacial intermetallic compound most commonly formed is the $AuSn_4$ phase [50]. The appearance of the δ-AuSn phase can be attributed to a further reaction of $AuSn_4$ with the Au layer following the exhaustion of the Sn interlayer.

The average thickness (Δx) of the intermetallic layers formed at the interface was measured and listed in Table 4.1. The data are plotted against the square root of reaction time (t) and shown in Figs. 4.3 and 4.4 for the $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ phases, respectively. In both cases, the growths of intermetallic compounds follow a parabolic rate law, implying that their reactions are diffusion-controlled. The growth rate constants ($k = \Delta x/t^{1/2}$) as calculated from Figs. 4.3 and 4.4 are given in Table 4.2. From the Arrhenius diagram of lnk *vs* $1/T$ as shown in Fig. 4.5, the activation energies (Q) for the growths of $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ intermetallic compounds can be determined as 16.9 kJ/mol and 53.7 kJ/mol, respectively. The former value (16.9 kJ/mol) is quite consistent with the activation energy for the diffusion of Cu in liquid Sn (19.5 kJ/mol), as reported by Ma and Swalin [51]. It implies that the rate-limiting step in the growth of the $(Cu_{0.99}Au_{0.01})_6Sn_5$ intermetallic is the diffusion of Cu dissolved near the intermetallic reaction front into the surrounding liquid Sn thin-film.

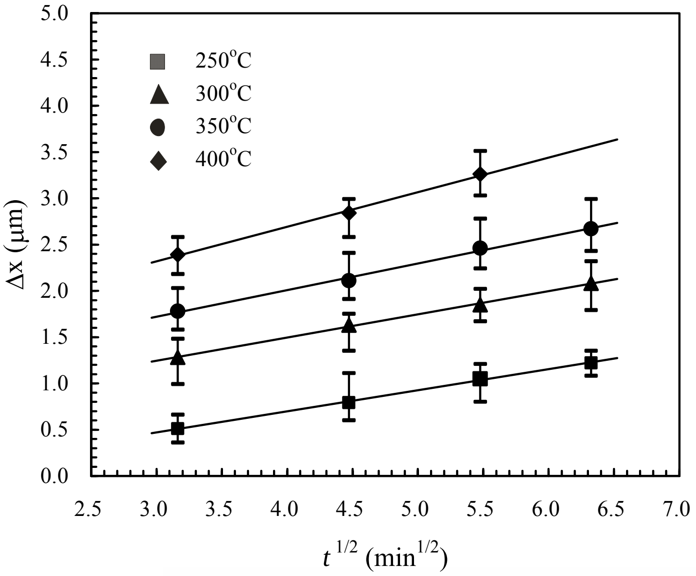


Fig. 4.3：The average thickness (Δ*x*) of $(Cu_{0.99}Au_{0.01})_6Sn_5$ intermetallic compounds formed during diffusion soldering between Cu/Ti/Si and $Au/Cu/Al_2O_3$ with Sn interlayers.

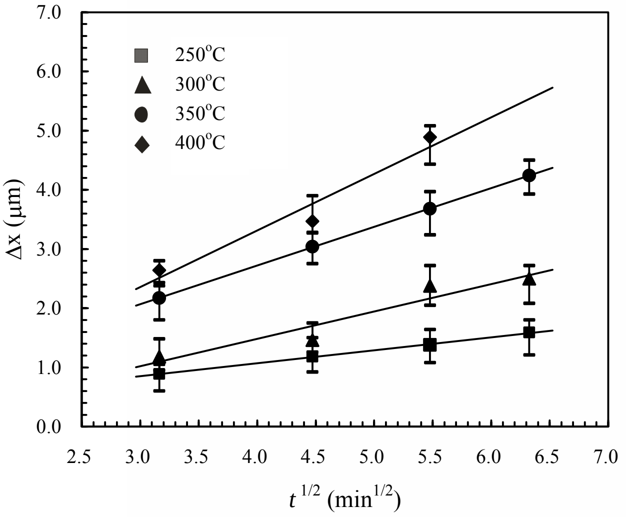


Fig. 4.4：The average thickness (Δ*x*) of $(Au_{0.87}Cu_{0.13})Sn$ intermetallic compounds formed during diffusion soldering between Cu/Ti/Si and $Au/Cu/Al_2O_3$ with Sn interlayers.

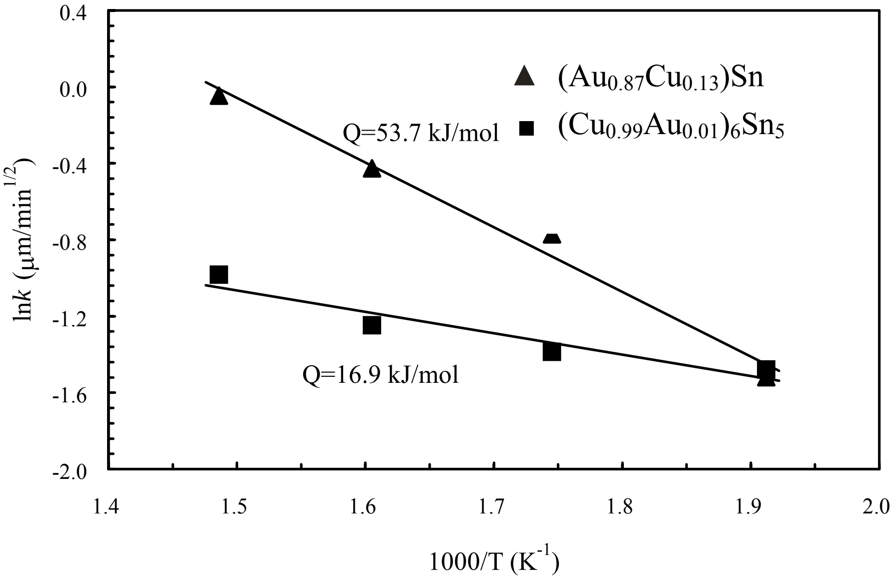


Fig. 4.5：The Arrhenius plots of growth rate constants (*k*) for $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ intermetallic compounds formed during diffusion soldering between Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers.

Table 4.1. Thicknesses of intermetallic compounds formed during diffusion soldering between Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers.

Temperature (°C)	Time (min)	$(Cu_{0.99}Au_{0.01})_6Sn_5$ (μm)	$(Au_{0.87}Cu_{0.13})Sn$ (μm)
250	10	0.51	0.89
	20	0.79	1.18
	30	1.05	1.38
	40	1.22	1.59
300	10	1.28	1.18
	20	1.63	1.46
	30	1.85	2.38
	40	2.08	2.50
350	10	1.78	2.17
	20	2.11	3.04
	30	2.46	3.68
	40	2.67	4.24
400	10	2.39	2.64
	20	2.84	3.47
	30	3.26	4.89

Table 4.2. Growth rate constants of intermetallic compounds formed during diffusion soldering between Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn interlayers.

Temperature (°C)	$(Cu_{0.99}Au_{0.01})_6Sn_5$ (μm/min$^{1/2}$)	$(Au_{0.87}Cu_{0.13})Sn$ (μm/min$^{1/2}$)
250	0.228	0.219
300	0.250	0.462
350	0.287	0.653
400	0.374	0.955

Tu and Thompson [52] reported that the growth of Cu_6Sn_5 intermetallic compound during the solid-state reaction between Cu and Sn thin films at room temperature exhibited a linear rate. According to their discussion, the rate-limiting step should be the release of Cu atoms from the Cu film, rather than the diffusion across Cu_6Sn_5. In contrast to the thin-film reaction discussed by Tu and Thompson, Vianco et al. [53] studied the solid-state interfacial reaction between Cu and hot-dipped Sn at temperatures ranging from 70℃ to 205℃. Parabolic growth kinetics for Cu_6Sn_5 intermetallic compounds was reported. The deviation of the reaction mechanism in Tu and Thompson's study [52] from the research of Vianco et al. [53], should be attributed to the ultra-thin film specimens (Sn thickness under 0.5 μm) and the quite low reaction temperature (room temperature) adopted by the former study. For the solid-liquid interdiffusion between Cu and Sn thin films at 240°C and 300°C, Bader et al. showed that the growth of Cu_6Sn_5 intermetallic compound did not follow the parabolic growth law [8]. As was explained by them, the deviation was attributed to the reduction of transport grooves resulting from the growth of the scallop-shaped Cu_6Sn_5 intermetallic compounds. Since the kinetic measurements obtained by Bader et al. were focused on the initial stage of reaction (reaction time: shorter than 2 mins; intermetallic thickness: thinner than 2μm), it is believed that once all the grooves along the interface have "closed" after a longer reaction time as similar for our study (reaction time: 10 mins to 40 mins), the reaction-controlling step in the growth of Cu_6Sn_5 should turn out to be the diffusion through the continuous Cu_6Sn_5 intermetallic layer. Hayashi et al. [54] studied the soldering reactions between Cu and liquid Sn saturated with Cu, and found that the growth of Cu_6Sn_5 intermetallic compound was diffusion-controlled with an activation energy of 29 kJ/mol, a value quite near our own kinetic measurement (16.9 kJ/mol). In summery of the above results, it can be implied that the solid-liquid interfacial reactions in the Cu/Sn thin film case are carried out similarly to a "normal" soldering reaction.

The calculated activation energy for the growth of the $(Au_{0.87}Cu_{0.13})Sn$ intermetallic (53.7 kJ/mol) is close to the activation energy for the lattice diffusion of Au in Sn ($\parallel$C: 46.1 kJ/mol, $\perp$C: 74.1 kJ/mol), as reported by Dyson [55]. The growth of the $(Au_{0.87}Cu_{0.13})Sn$ intermetallic is, therefore, believed to be controlled by the lattice diffusion of Au through the solid intermetallic compound. The discrepancy in growth rate-controlling mechanisms for $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ intermetallics may be attributed to the much quicker liquid/solid reaction for $Sn_{(l)}/Au_{(s)}$ than that for $Sn_{(l)}/Cu_{(s)}$. This explanation can be validated by the quite different wettability of liquid Sn on Au and Cu substrates. Figure4.6 shows that the contact angle of liquid Sn on the Au substrate decreases rapidly and vanishes at complete wetting (~0°), while the contact angle in the case of the Cu substrate remains at about 30°, implying that it is much easier for liquid Sn to react with Au than with Cu. In other words, $Au_{0.87}Cu_{0.13}$ reacts rapidly during diffusion-soldering with Sn to form $(Au_{0.87}Cu_{0.13})Sn_4$. After the thin-film Sn is exhausted, a further solid/solid interfacial reaction takes place: $(Au_{0.87}Cu_{0.13})Sn_4 + 3(Au_{0.87}Cu_{0.13}) \rightarrow 4(Au_{0.87}Cu_{0.13})Sn$. Since the reaction efficiency is governed by the slow mode of the latter reaction, the rate-controlling mechanism for the growth of $(Au_{0.87}Cu_{0.13})Sn$ is therefore the diffusion of Au in this solid intermetallic phase. The solid/solid interfacial reaction in the Au/Pb-Sn solder system has been studied by Hannech and Hall [56]. They found that an $AuSn_4$ intermetallic compound was formed under diffusion control during reaction. The activation energy was 40 kJ/mol, similar to the value of our measurement for the solid/liquid thin film reaction of the Au/Sn system (53.7 kJ/mol). Their results sustain the view held by this present study, that the growth of $(Au_{0.87}Cu_{0.13})Sn$ is controlled by a solid/solid interfacial reaction as discussed previously.

Tensile strengths of the specimens after diffusion soldering at various temperatures for 20 min are shown in Fig. 4.7. A maximum value of 132 kg/cm^2 is attained at the bonding temperature of 300°C. As Table 4.1 indicates, such an optimized bonding condition (300°C, 20min) is conducive to the growth of $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ intermetallic layers to the thicknesses of 1.63 μm and 1.46 μm, respectively. This thesis proposed a novel joining technique using diffusion soldering technique for die attachment to bond different materials, which has less defects at bonding parts such as coagulation cracks or gas cavities.

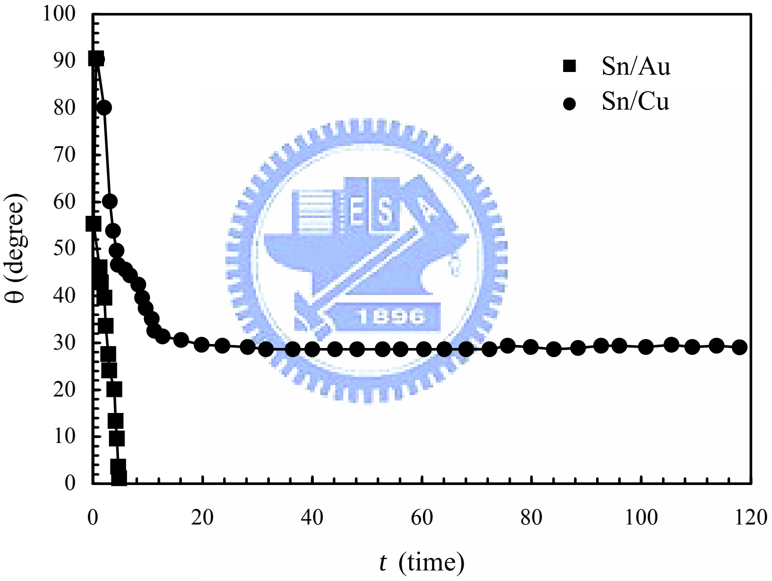


Fig. 4.6：The contact angles (θ) of liquid Sn on the surfaces of Au and Cu substrates at 350°C. $Sn_{(l)}/Au_{(s)}$ reacts much more quickly than $Sn_{(l)}/Cu_{(s)}$.

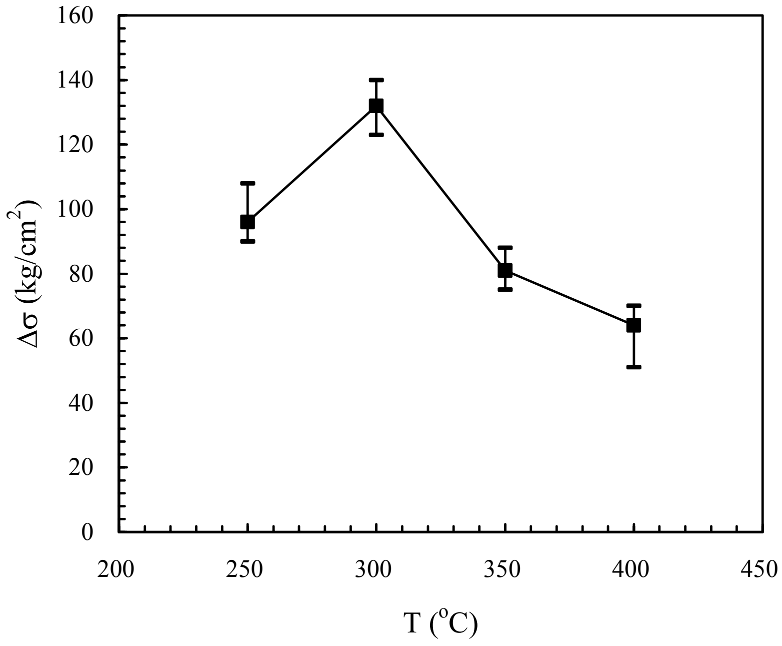


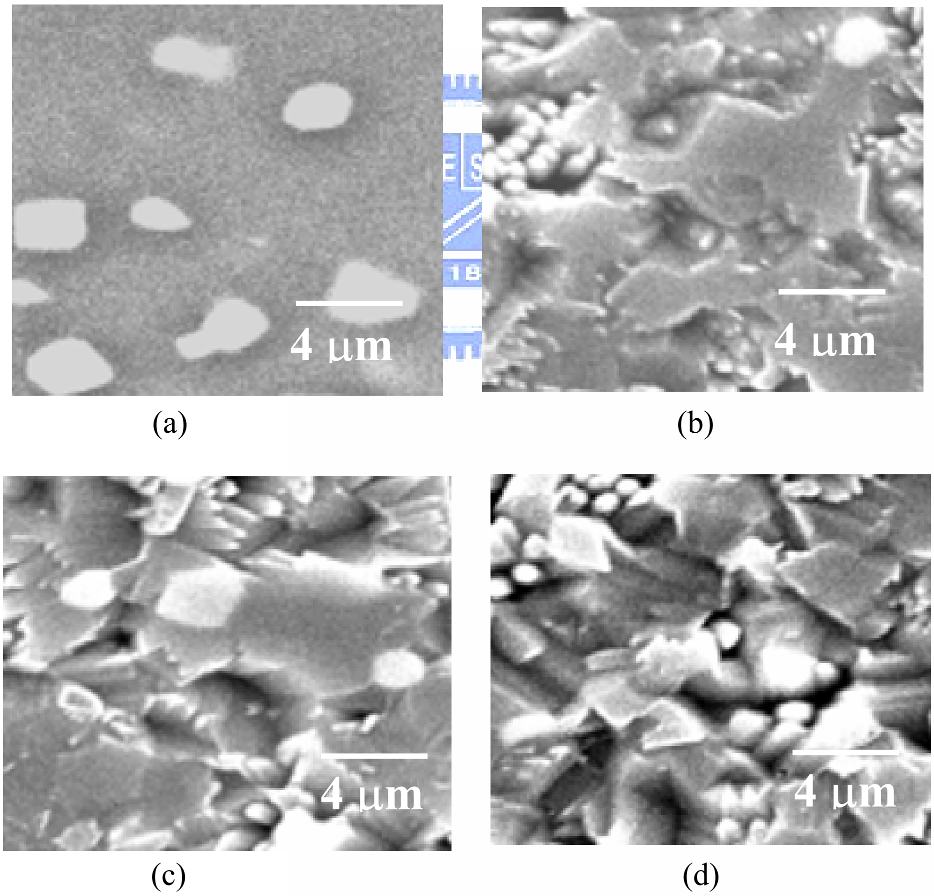
Fig. 4.7：The tensile strengths (σ) of Cu/Ti/Si wafer diffusion-soldered with Au/Cu/Al_2O_3 substrates at various temperatures for 20 min using an Sn thin-film interlayer.

4-2 Electroless Copper/Nickel Films Deposited on AlN Substrates

4-2.1 Surface morphology of AlN substrates

Figure 4.8 is a SEM image of the polished AlN substrate surface. After being etched by the NaOH solution, the surface became rougher and rougher with increasing etching time. The white granules in Fig. 4.8(a) should be the Al-Y-O compounds reported in previous studies. [57,58] Figure 4.9 shows the SEM image of the unpolished substrate surface in which AlN grains are clearly visible. The etching removed the small grains, and with increasing etching time, various column-like holes were generated. Figure 4.10 shows the variation in AlN surface roughness with etching times measured by atom force microscopy

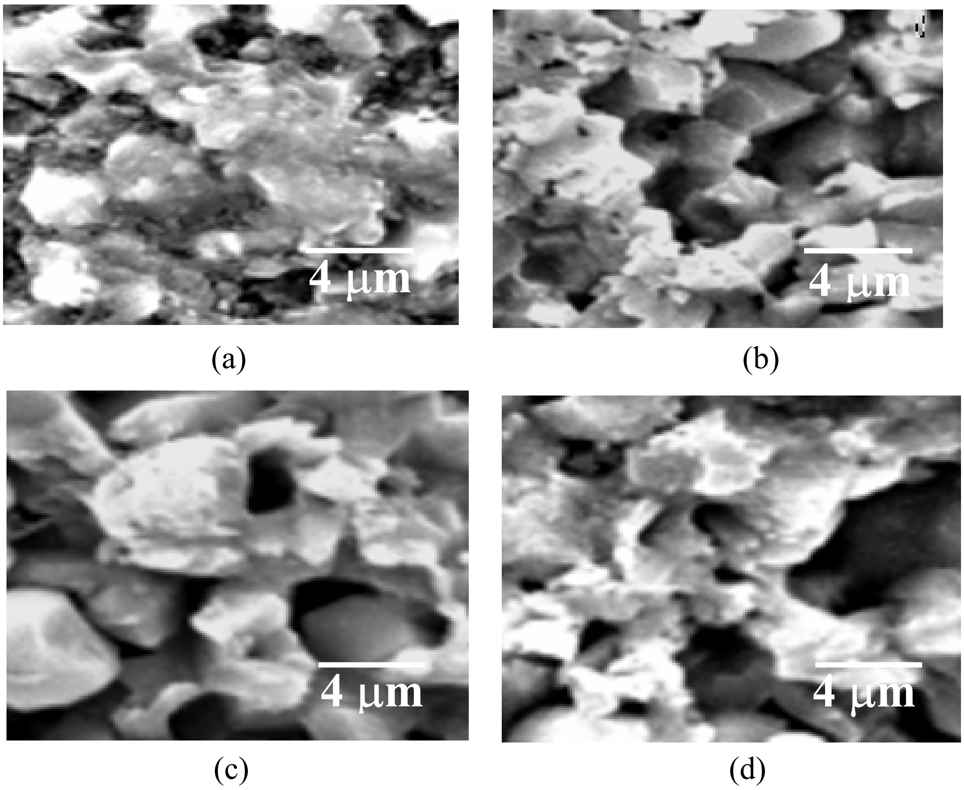
(AFM). As shown in Fig. 4.10, the roughness of unpolished AlN substrates is always higher than that of polished AlN substrates regardless of the duration of etching time. Furthermore, the roughness of the polished AlN substrate increases with increasing etching time, while the roughness of the unpolished AlN surface reaches a peak value of 0.45 μm after 60 min etching and further etching does not seem to exacerbate the roughness. We believe that the etched, unpolished AlN substrates should possess a higher roughness since the tip of the AFM probe might not be able to reach the bottom of the holes on the sample surface hence the true surface roughness could not be totally revealed.



(a) (b)

(c) (d)

Fig. 4.8： Surface morphology of polished AlN surface after etching for (a) 0 min, (b) 30 min, (c) 60 min, and (d) 120 min



(a) (b)

(c) (d)

Fig. 4.9：Surface morphology of unpolished AlN surface after etching for (a) 0 min, (b) 30 min, (c) 60 min, and (d) 120 min.

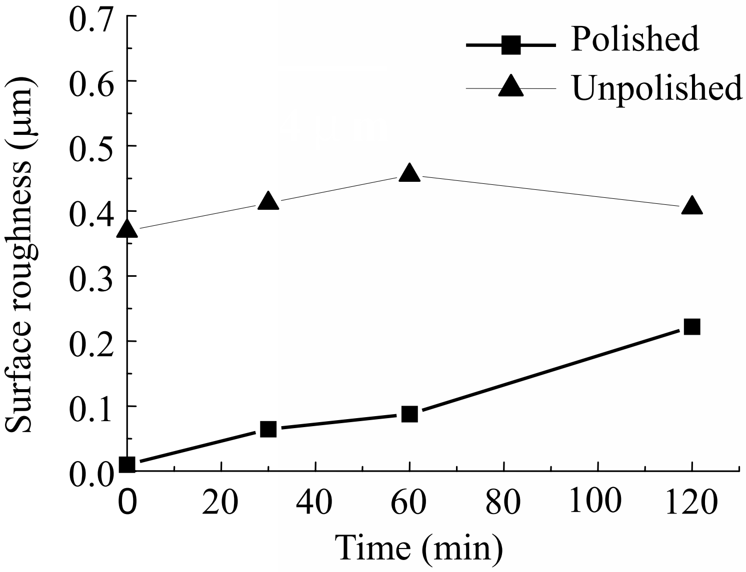
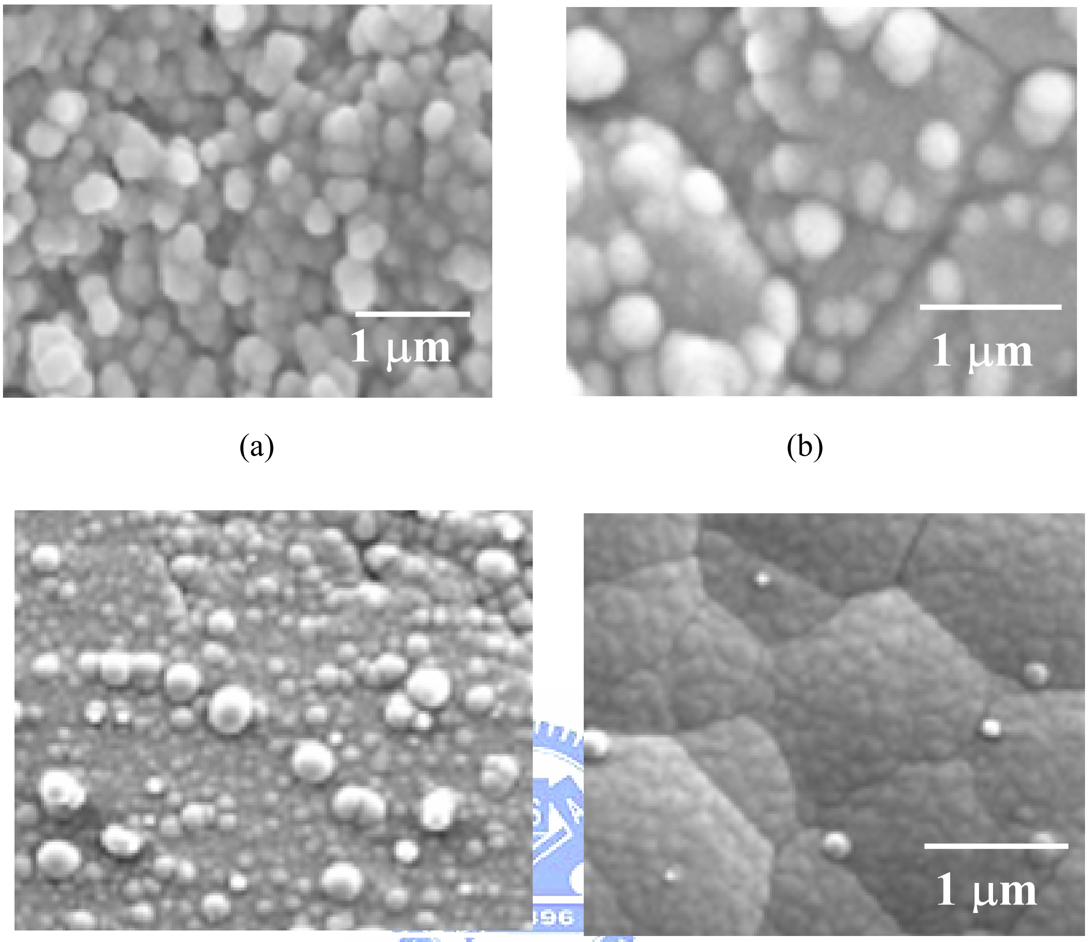


Fig.4.10：Variation in AlN surface roughness with etching time.



(a) (b)

(c) (d)

Fig.4.11： Surface morphologies of electroless Ni plated on polished AlN substrates for (a) 0.5 min, (b) 1 min, (c) 4.5 min, and (d) 26.5 min.

4-2.2 Surface morphology of electroless-plated metal layers

Figures 4.11 and 4.12 show the surface morphologies of the EN plated on polished and unpolished AlN substrates etched for 30 min, respectively. It can be clearly seen that the EN films plated on the polished surface possess a finer grain structure than those on the unpolished surface, however, the EN films on the unpolished substrate are rugged and void-embedded. In both types of AlN substrates, the Ni grains should initiate from the Pd seeds formed during the surface activation. On the polished AlN substrate, the Ni granules grew and soon coalesced with each other to form the fine grain structure as shown in Fig. 4.11 [see illustration in Fig. 4.13(a)]. On the unpolished AlN substrate, even though the rougher surface might offer more nucleation sites as predicted by the heterogeneous nucleation theory, our experimental observation indicated that this could not be applied to electroless plating of the unpolished AlN substrate. As shown in Fig. 4.14(b), cross-sectional view of the Ni/AlN interface reveals that in fact the Ni does not fill up the etched holes in an unpolished AlN substrate. Probably the capillarity effects prevented the activation solution from reaching the bottom of the holes that metallization could only proceed on the top region of the unpolished surface [see illustration in Fig. 4.13(b)]. Another possible cause of this was the gaseous bubbles generated during plating, which inhibited the full coverage of metallization. Since the Ni granules located at the tops of the column-like grains must grow to a certain size to coalescence with each other, the Ni layer thus exhibits a coarse grain structure as shown in Fig. 4.12. Furthermore, if the coalescence fails, voids form in the Ni layer, as shown in Fig. 4.12(d).

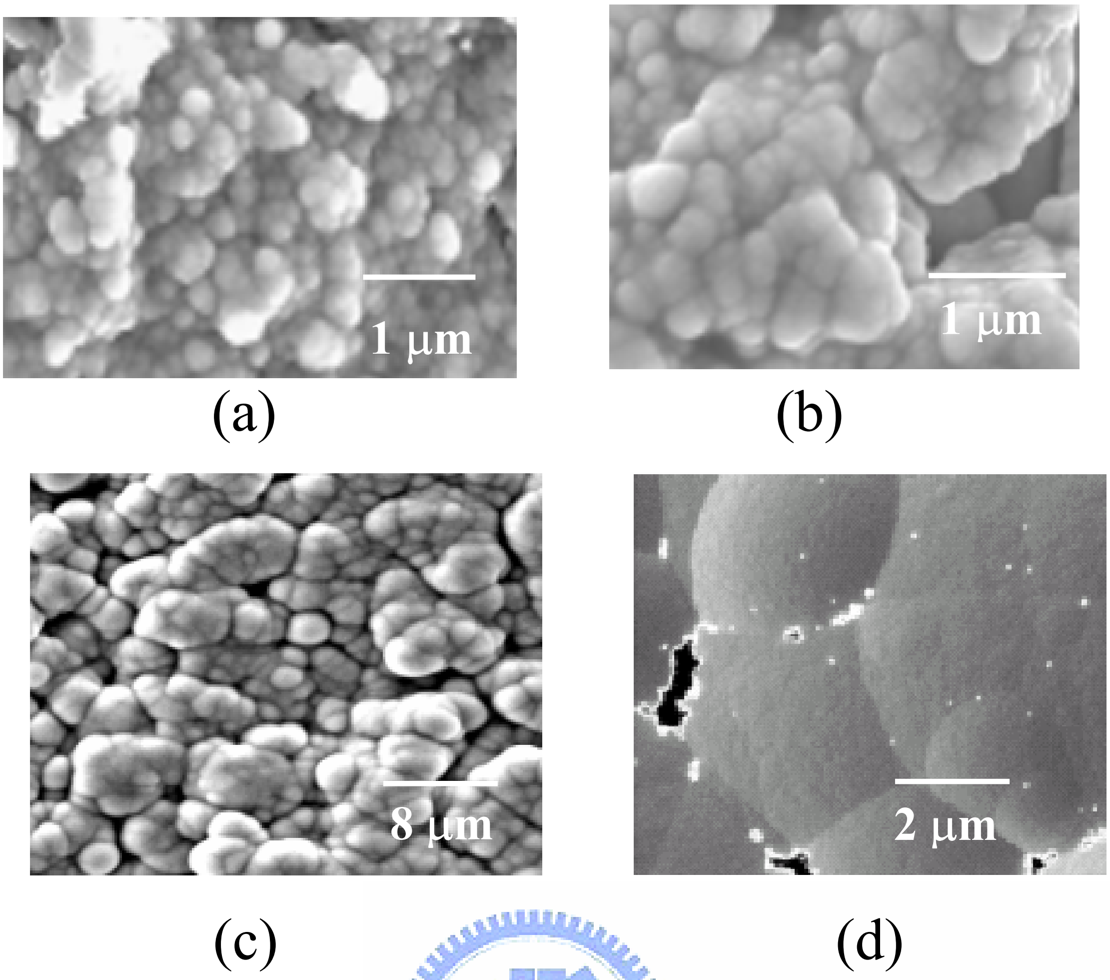


Fig.4.12：Surface morphologies of electroless Ni plated on unpolished AlN substrates for (a) 0.5 min, (b) 1 min, (c) 4 min, and (d) 30 min.

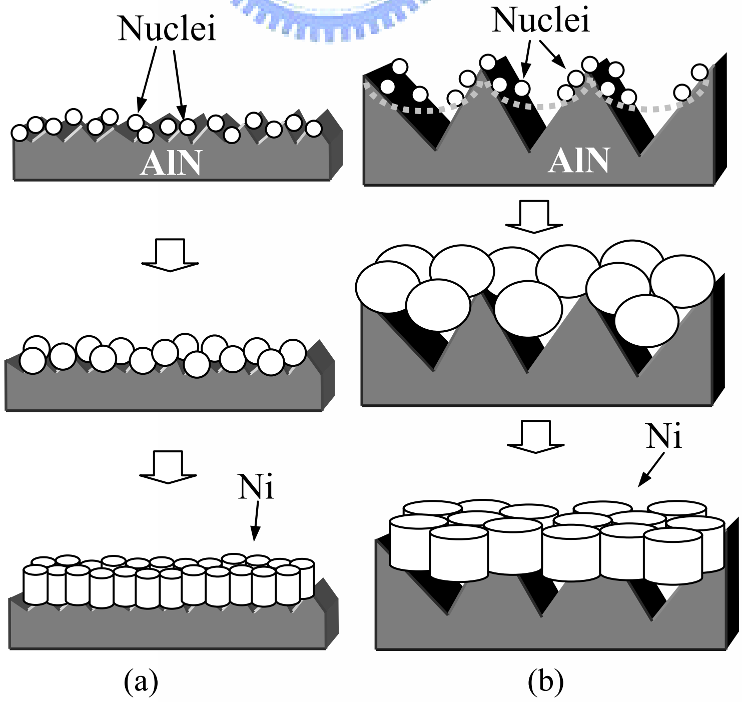
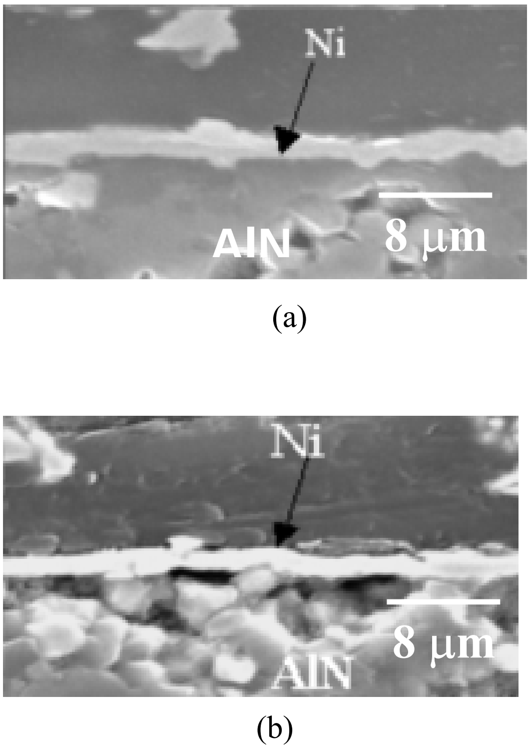


Fig. 4.13：Illustration of grain growth on (a) polished and (b) unpolished AlN substrates.



(a)

(b)

Fig. 4.14： Cross-sectional view of EN layer plated for 3 min on (a) polished and (b) unpolished AlN substrates.

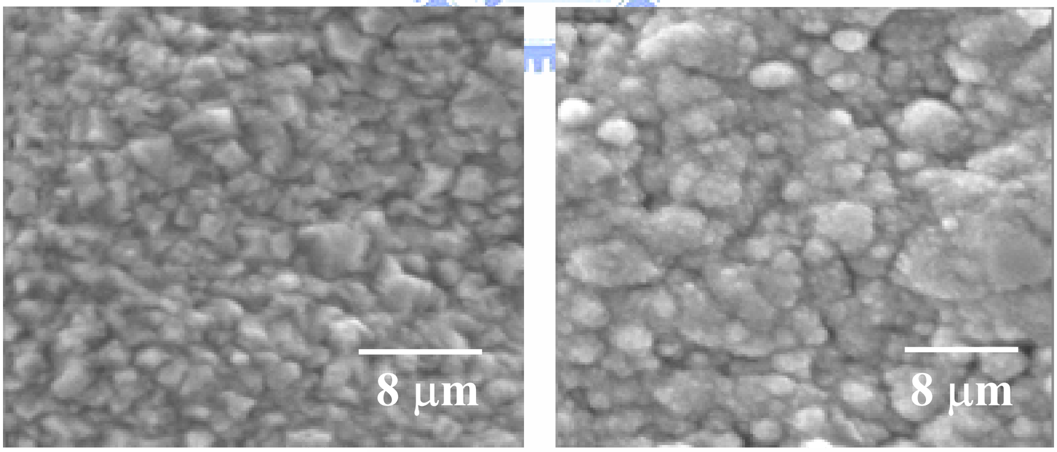


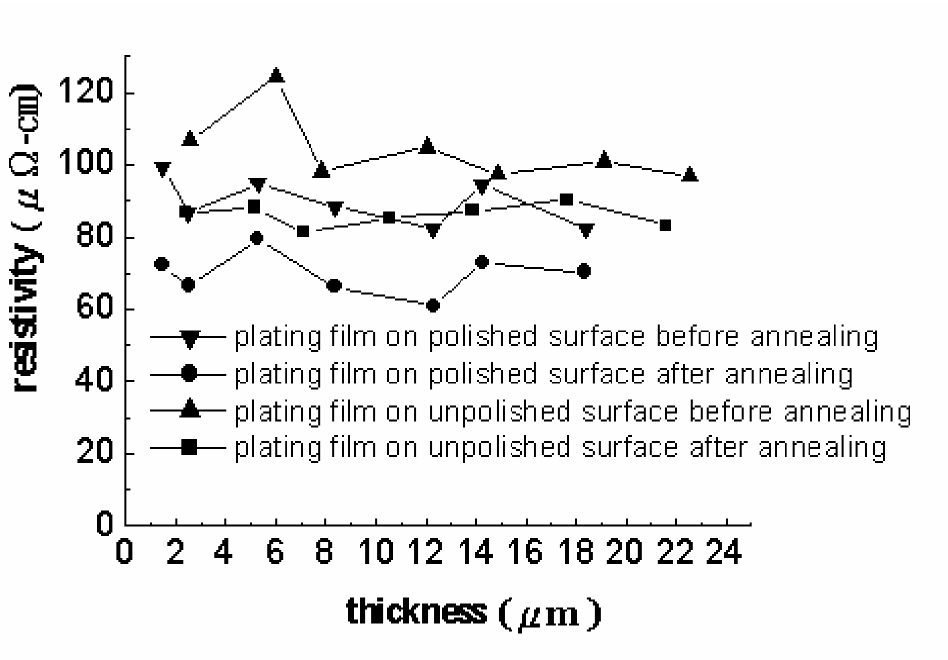
Fig. 4.15： Surface morphologies of electroless Cu plated on (a) polished and (b) unpolished AlN substrates plating for 90 min.

Figures 4.15(a) and 4.15(b) show the surface morphologies of the electroless Cu plated on polished and unpolished AlN substrates, respectively. The differences in surface roughness and grain size clearly indicate that the surface roughness of the AlN substrate affects the morphology of the subsequently plated film. The flat AlN substrate can generate a flat Cu layer with a fine grain structure.

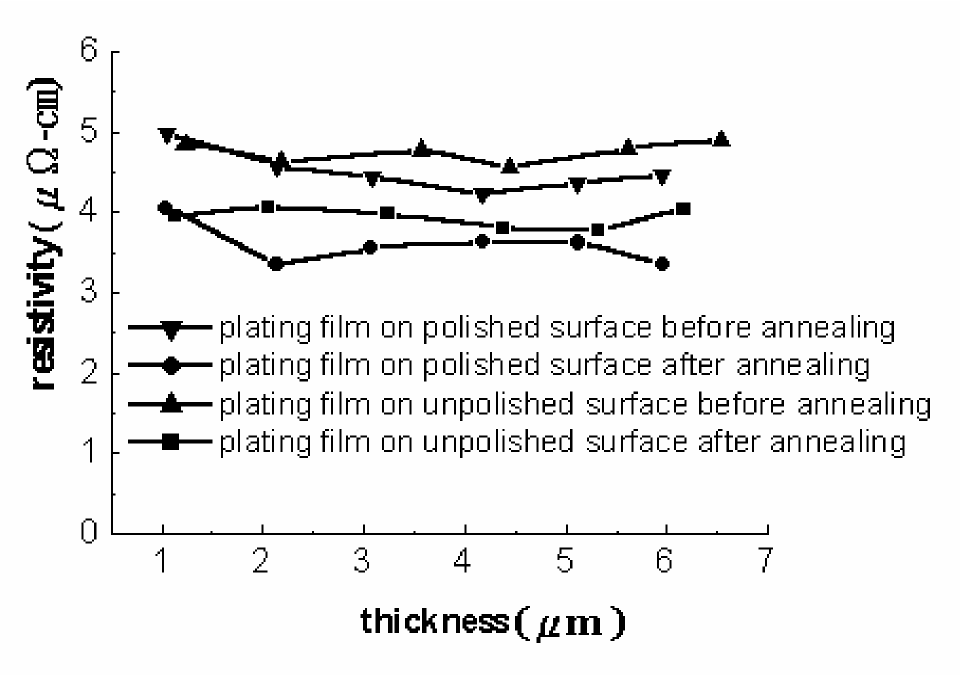
4-2.3 Resistivity measurement

Figures 4.16(a) and 4.16(b) depict the resistivities of Ni and Cu layers on the polished and unpolished AlN substrates, respectively. In both cases, the resistivities of deposited films on the polished AlN surface are always lower than those on the unpolished AlN surface. Apparently, the rougher, unpolished AlN substrate surface induced defects in the film interface during grain clustering and thereby deteriorated the electrical conductivity of the deposited layers.

The specimens were also annealed at 250°C for 1 h under inert ambient. Even though a decrease in resistivity was observed, subsequent XRD analysis revealed that no marked structure change occurred in the deposited layers. The decrease in resistivity might be a result of the annihilation of point defects and dislocations, rather than of the recrystallization and grain growth phenomena in the Ni and Cu layers. There was no obvious change in the microstructures of metal films subjected to a 250°C–1 h annealing.



(a)

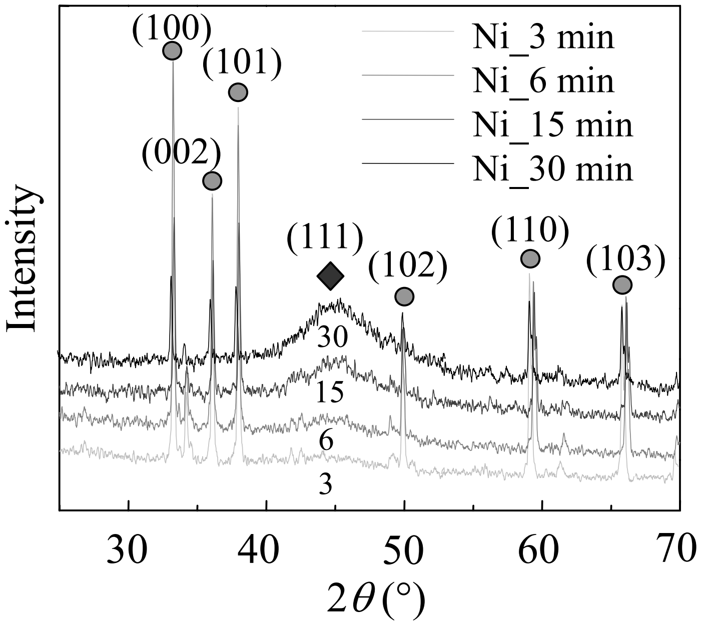


(b)

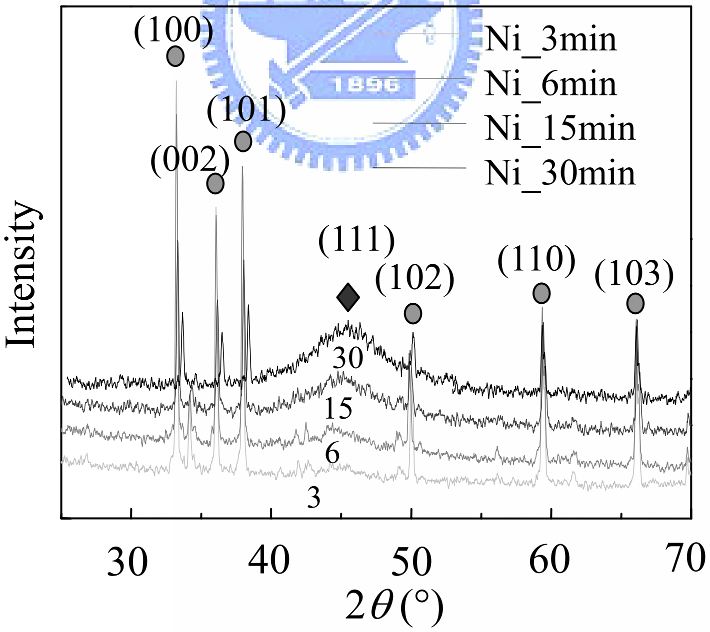
Fig. 4.16： Resistivities of electroless (a) Ni and (b) Cu deposited on polished and unpolished AlN substrates.

4-2.4 Structure and composition analyses of plated Ni and Cu layers

The amorphous feature of EN films indicates that they are in a non-equilibrium state. [57] Figures 4.17(a) and 4.17(b) show the XRD patterns of EN films before and after 250°C–1 h annealing. It can be seen that the thin EN film was amorphous and, with the increase in plating time, the crystallinity of the EN film gradually improved. Nevertheless, the EN film plated over 15 min (or film thickness > 5µm) still has a wide peak distributed over the diffracted angle range of 37° to 55°. This is due to the fact that during plating, the phosphorus atoms were incorporated in the Ni deposition reducing its crystallization. Figures 4.17(a) and 4.17(b) further indicate that the structure of the EN films did not change markedly with the 250°C–1 h annealing. Figures 4.18(a) and 4.18(b) show the XRD patterns of Cu films before and after the 250°C–1 h annealing. The Cu films were polycrystalline, evidenced by the sharp (111) and (200) diffraction peaks appearing at 43.3° and 50.4°, respectively.

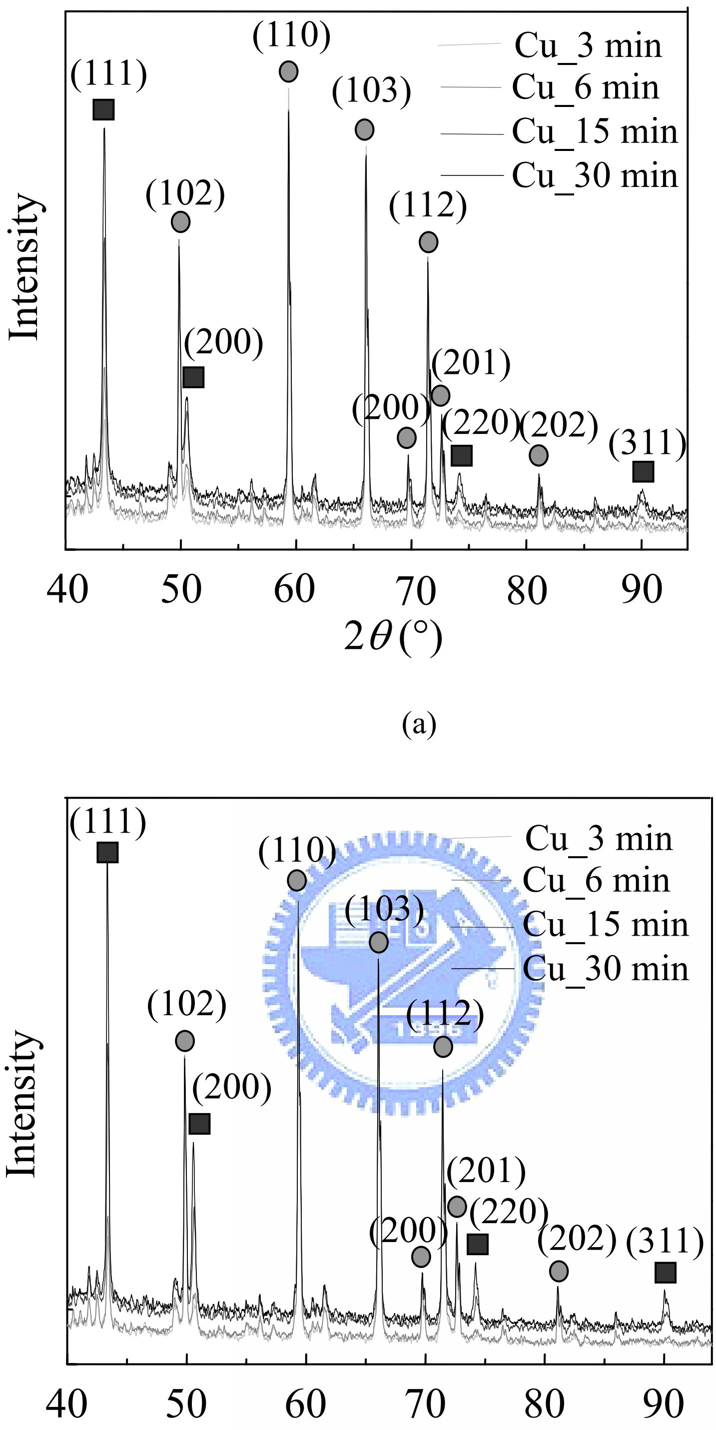


(a)



(b)

Fig. 4.17 XRD pattern of Ni/AlN (a) before and (b) after 250°C 1 h annealing (●: AlN; ◆:Ni)



(a)

(b)

Fig. 4.18：XRD pattern of Cu/Ni/AlN (a) before and (b) after 250°C–1 h annealing.

(●: AlN; ■ :Cu)

Tables 4.3 and 4.4 show the composition of Ni on the polished and unpolished AlN substrates analyzed by SEM/EDS. It was found that after 2 min of deposition, the AlN substrates were completely covered by Ni film whose thickness was approximately equal to 0.7μm. As the plating time increases to 5 min, the content of phosphorous in Ni reached a steady value of 9.7 wt%. The composition variations of Ni films were similar regardless of the difference in roughness of AlN substrates. Previous studies[7,59] pointed out that when the phosphorous content of Ni is 7~10 wt%, its structure is a mixture of amorphous and microcrystalline grains. When the phosphorous content of Ni is higher than 10 wt%, it becomes amorphous. The secondary-ion-mass spectrometry (SIMS) depth profile shown in Fig. 4.19 revealed that the phosphorous content is the highest at the Ni/AlN interface. This implies that the phosphorous content might exceed 10 wt% and the Ni film in the vicinity of Ni/AlN interface is amorphous. This provides the EN film as a good barrier since it contains no grain boundary for fast diffusion.

Table 4.3. Compositions of electroless Ni on polished AlN surface. (unit : wt%)

Plating time	Al	P	Ni
15 sec	77.58	6.14	16.29
30 sec	52.96	7.78	39.24
45 sec	36.33	8.95	54.72
120 sec	0	9.81	90.19
300 sec	0	9.69	90.31

Table 4.4. Compositions of electroless Ni on unpolished AlN surface. (unit : wt%)

Plating time	Al	P	Ni
15 sec	54.29	6.76	38.95
30 sec	38.56	7.33	54.11
45 sec	18.71	8.15	73.14
120 sec	0	9.78	90.22
300 sec	0	9.72	90.28

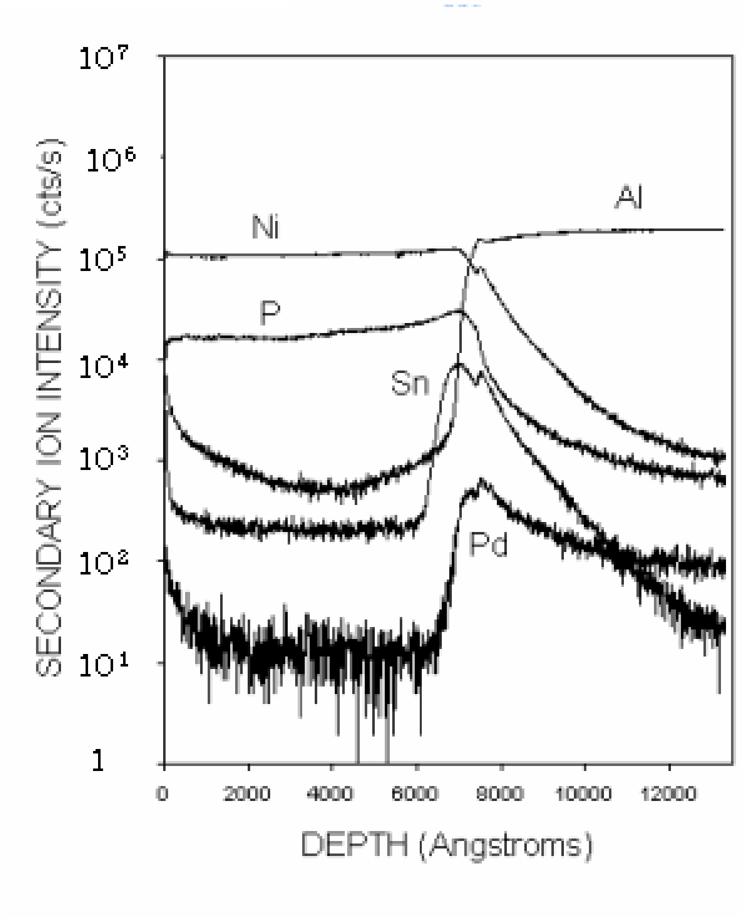


Fig. 4.19： SIMS depth profile of EN layer plated on polished AlN substrate for 2 min.

4-2.5 Pull-off and shear tests

Table 4.5 shows the results of pull-off test for EN layers deposited on polished AlN substrates. During the test, it was found that all specimens broke at the stud/epoxy resin interface, rather than at the Ni/AlN interface. Hence the test results shown in Table 4.5 do not represent the true adhesion strength of the EN/AlN interface. The high adhesion strength of EN film on AlN should result from the mechanical interlock effects on rough substrate surface generated by the etching using the 4 wt% NaOH solution for 30 min.

Table 4.5. Pull-off test results of electroless Ni on polished AlN substrate.

Pull-off stress (kg/cm^2)	Location of breakage
889.20	Stud/epoxy resin interface
892.81	Stud/epoxy resin interface
923.07	Stud/epoxy resin interface
846.95	Stud/epoxy resin interface
913.14	Stud/epoxy resin interface

Since we also plated Cu on the Ni film and then carried out the pull-off test, the similar result was obtained compared to those of Ni film (see Table 4.6). This result not only indicates that the electroless Cu is able to form a relatively strong bonding with Ni, but also ensures that the adhesion property of the Cu/Ni interconnection formed on the AlN substrate fulfills the mechanical demands of subsequent processing.

Table 4.6 Pull-off test results of electroless Ni/Cu on polished AlN substrate.

Stress (kg/cm^2)	Location of breakage
761.57	Stud/epoxy resin interface
937.78	Stud/epoxy resin interface
932.68	Stud/epoxy resin interface
833.22	Stud/epoxy resin interface
924.42	Stud/epoxy resin interface

The shear test results indicated that the 30-μm-high Ni lug deposited on AlN surface had a higher shear strength than the machine test limit. The upper thrust limitation of the shear tester is 100 g, so we could only conclude that the shear strength of EN on AlN was higher than 100 g.

The above results indicate that etching on the surface of AlN substrates provides a strong mechanical interlocking effect to ensure good adhesion of EN films. However, the etching must be appropriate otherwise the rough surface would induce voids in the metal overlayer and hence deteriorate its electrical property. From the measured results of surface roughness, resistivity, and adhesion tests, we concluded that a satisfactory substrate could be obtained by etching on polished AlN surface using 4 wt% NaOH solution for approximately 30 min. The EN film plated on such a substrate surface not only possesses a compact and nearly void-free structure, it also exhibits a low electrical resistivity that meets the requirement of subsequent flip chip interconnection.

4-2.6. Flip chip bumping

In this study, we also investigated the flip chip bonding of GaAs PHEMT devices on the metallized AlN substrates, as shown in Fig. 4.20. From the SEM observation shown in Fig. 4.21, it was found that the thickness of intermetallic compounds (IMCs) increased with the time of thermal treatment at 250°C. The IMCs mainly consisted of Ni_3Sn_4 and Cu_6Sn_5, as revealed by XRD and SEM/EDS analyses. In Fig. 4.21(b), the hemispherical scallop-like IMCs[60] formed after 2 h annealing can be clearly seen. The SEM/EDS revealed that the IMCs possess the composition of Cu:Sn = 54.5:45.5 so they should consist of the Cu_6Sn_5 phase. Finally, the EDS element linear scanning analysis, shown in Fig. 3-15, reveals rather weak Sn signal amplitude inside the Ni layer. This is consistent with previous studies that the amorphous EN film was a good diffusion barrier layer for UBM construction.

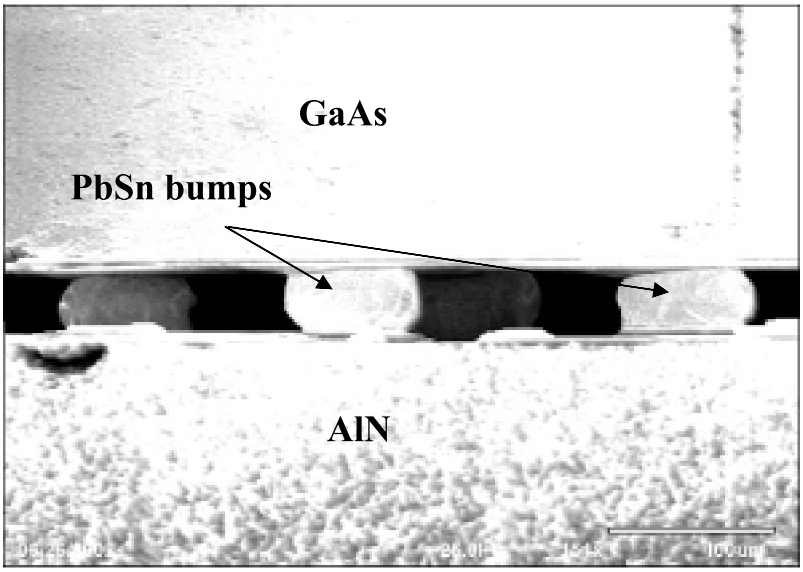
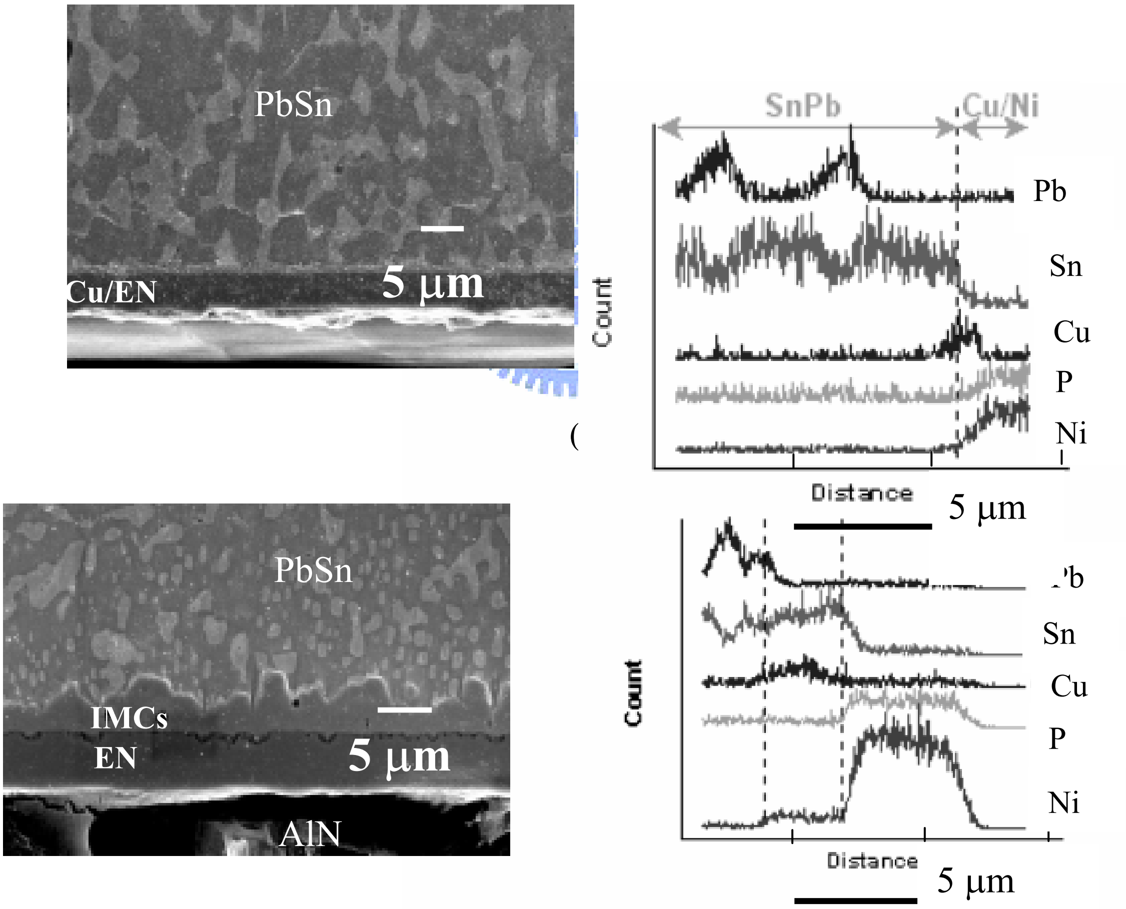


Fig. 4.20： Flip chip bonding of GaAs PHEMT IC on AlN substrate.



(b)

Fig. 4.21： SEM cross-sectional view of EN/AlN interfaces and corresponding line scanning EDS analysis (a) before 250°C annealing and (b) after 250°C 2 h annealing.

4-3 Electroless Cobalt Layer and Its Diffusion Barrier Properties of Pb-Sn Solder

4-3.1. The Deposition Rate of Electroless Co(P) Layer

Figure 4.22 is a profile showing plating time *vs*. thickness of electroless Co(P). At the beginning of the plating process, the deposition rate was faster since the concentration of plating bath is higher so that the thickness reaches 100 nm during the first 30 sec while the average plating rate is 130 nm/min. The chemical reaction formula of electroless plating Co(P) indicates that the deposition rate increase with the increase of pH value since the alkaline environment is preferred for electron releasing[26]. Table 4.7 shows the average thickness of plated layers under conditions of different pH values at 75°C. It is noted that the thickness of plated layer increases with the increase of pH value, which reveals that the alkaline environment is beneficial for the increase of deposition rate. In addition, since chemical reaction can be enhanced by the raise of temperature so that the higher the temperature, the faster the deposition rate.

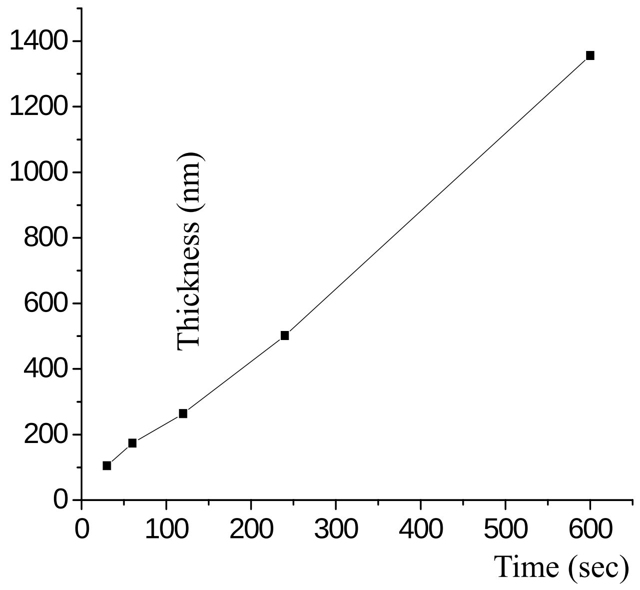


Fig. 4.22：Thickness of electroless plating Co(P) layer *vs*. deposition time.

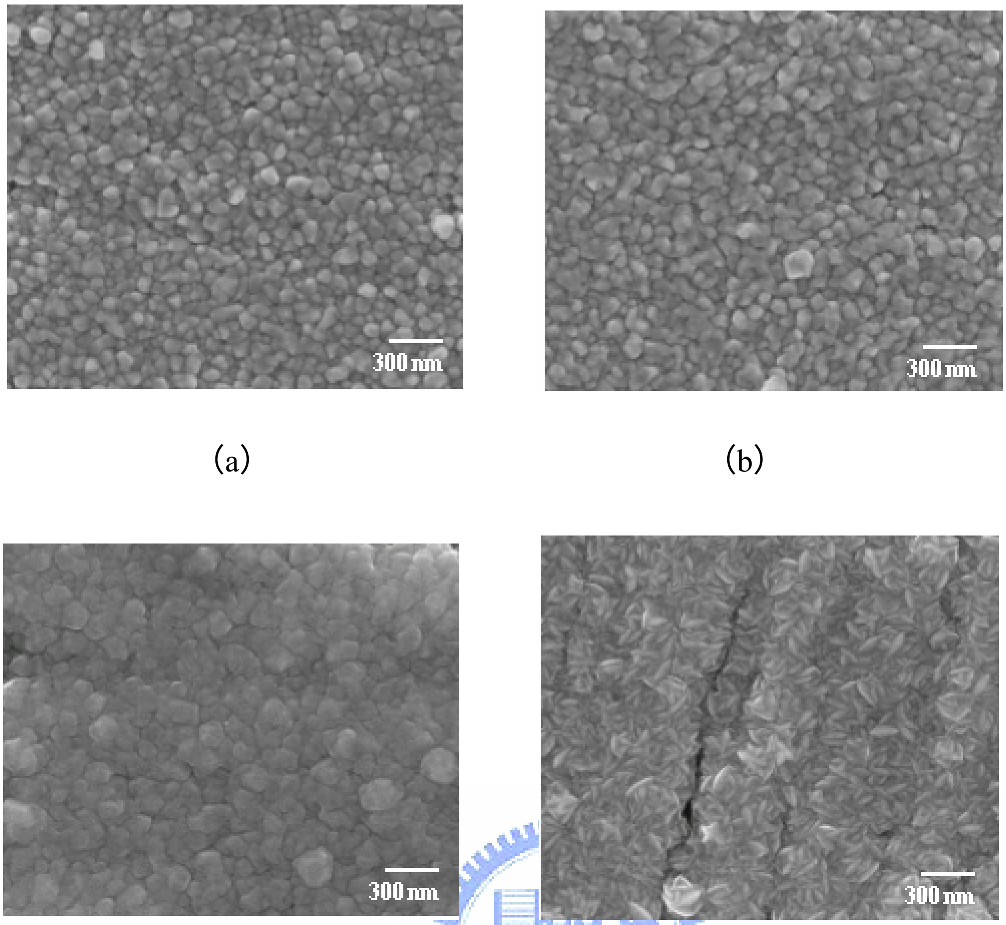
Table 4.7. Average thickness of plated Co(P) layer.

pH value	Average thickness for 30 sec (nm)
7.5	100
8.0	160
8.5	250

4-3.2. Morphologies of Electroless Co(P) Layer

The number and size of palladium (Pd) granules formed on the sample were affected by the time that the sample was immersed in the activation solution. If the activation time was too short, the Pd granules was insufficient to cover the sample completely. If the activation time was too long, the size of each Pd grain might exceed 100 nm and there might be too many Pd precipitates being formed and left in the plating bath. It was found that the activation time of the experiment set at about 45 sec may produce 20 to 30 nm Pd granules uniformly covering the substrate surface.

In addition to the phosphorous content of the plated layer, variation of pH values also affects the clustering of Co(P) nucleation. Figure 4.23 shows the morphologies of Co(P) layer deposited on the polished Cu plate after being immersed in plating baths of different pH values for 60 sec each. It is noted that the size of Co(P) clusters increases with the increase of pH value, whereas the surface coverage is the best at pH = 8.5. The structure of Co(P) clusters changes into conifer-leaf shape at the pH = 9.0. Since the Co(P) layer was formed by replacing the activated Pd atoms, the density and the continuity of the electroless Co(P) layer were affected by the cluster condition of Pd atoms and the condition of the substrate surface. As revealed by subsequent SEM and XRD analyses, the plural particles formed on the specimen surface were not caused by the crystallization during electroless plating, instead it was caused by clustering effect. Clusters grew with the increase of deposition time and eventually became a large particle.



(a) (b)

(c) (d)

Fig. 4.23： Surface morphologies of Co layers deposited at different pH values: (a) pH = 7.5; (b) pH = 8.0; (c) pH = 8.5; (d) pH = 9.0.

4-3.3. Composition Analysis of Electroless Co(P) Layer

It is known that the amount of phosphorous content in Co(P) film affects the structure and surface morphology of the plated films. When the phosphorous content in Co(P) film is within the range of 8 *at.*% to 10 *at.*%, the formed crystal grain is nanocrystalline. When the phosphorous content in Co(P) film is within the range of 10 *at.*% to 12 *at.*%, the electroless Co(P) layers are the mixture of amorphous and nanocrystalline structures.

When the phosphorous content in Co(P) film exceeds 12 *at.*%, the electroless Co(P) layers are amorphous structure[61]. The amorphous structure starts to crystallize into α-Co at about 290°C, and the Co_2P of orthorhombic crystal appears at 420°C[31]. The thermal treatment of the present experiment was at 250°C, so that the two types of Co crystals would not appear in the experiment. According to the composition analysis of Co(P) thin film, the phosphorous content in Co(P) film varied with the change of deposition time. As seen in Table 4.8, the phosphorous content in Co(P) film decreases with the increase of deposition time, but the minimum amount is still larger than 8.68 *at.*% at any deposition time. Therefore, the specimens of this experiment were of nanocrystalline and amorphous structures, which was proven by subsequent XRD analysis.

Table 4.8. EDX phosphorous contents with respect to different deposition times.

Deposition time (sec)	Co (*at.*%)	P (*at.*%)
30	85.02	14.98
60	85.97	14.03
120	86.66	13.34
240	89.68	10.32
600	91.32	8.68

Figure 4.24 shows an AES analysis depicting the depth profile of a 600 nm electroless

Co(P) layer with 5 min deposition time. The horizontal axis represent the depth of the Co(P) layer from surface down and the vertical axis represents the average phosphorous content of every 100 nm thickness Co(P) film. As seen in Fig. 4.24, the phosphorous content increase with the depth of the Co(P) layer and, at the interface between the Co(P) and the Ti/Cu layers, the phosphorous content reaches its maximum, *i.e.* nearly 18 *at.*%. To sum up, the phosphorous content is the highest at the beginning of the electroless plating and decreases gradually at the progress of deposition time. It was speculated that such that with the increase of deposition time, the electroless Co(P) structure is in transition from amorphous to nanocrystalline, or even poly-crystalline structure.

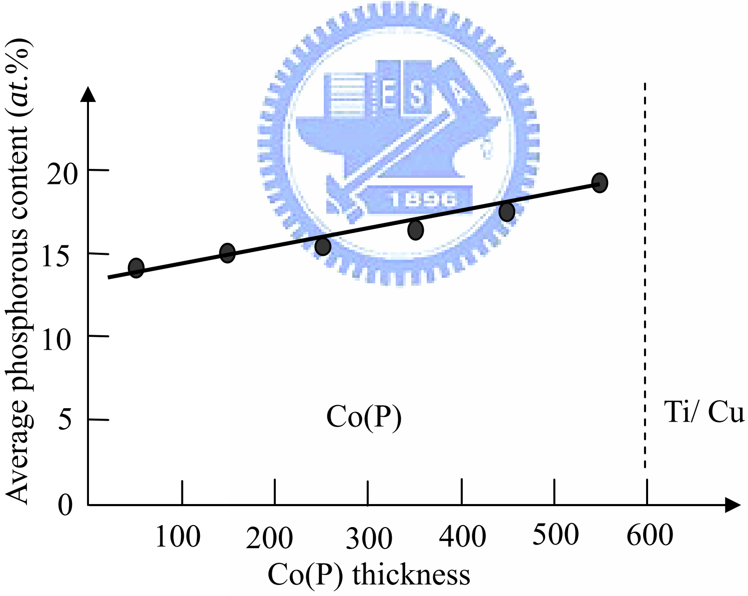


Fig. 4.24： Average phosphorous content of electroless Co(P) analyzed by AES.

4-3.4. XRD Analysis of the Plated Layer

As seen in Fig. 4.25, the 30-sec Co(P) layer has no obvious Co peak, but has only two Cu (111) and (200) peaks; therefore in conjunction with previous AES analysis, it is concluded that, at the early stage of the plating, the electroless Co(P) layer formed is amorphous. With the increase of deposition time, the height of Co peaks increases while that of the Cu peaks decreases relatively. For a specimen being plating for 600 sec, the peak corresponding to $(01\bar{1}0)$ is significant comparing to that of (0002) and $(01\bar{1}1)$. Therefore, the nanocrystalline structure grows with respect to the decreasing of phosphorous content. With the increase of deposition time, the nanocrystalline area gradually exemplified and thereby significant Co peaks were observed in the XRD pattern. Figure 4.26 shows the XRD pattern of Co(P) films deposited for 30 min, whose thickness is about 2.5 μm. As seen in Fig. 4-6, the pronounced Co peaks corresponding to $(01\bar{1}0)$, (0002) and $(01\bar{1}1)$ reveal that the 30 min Co(P) film is polycrystalline structure.

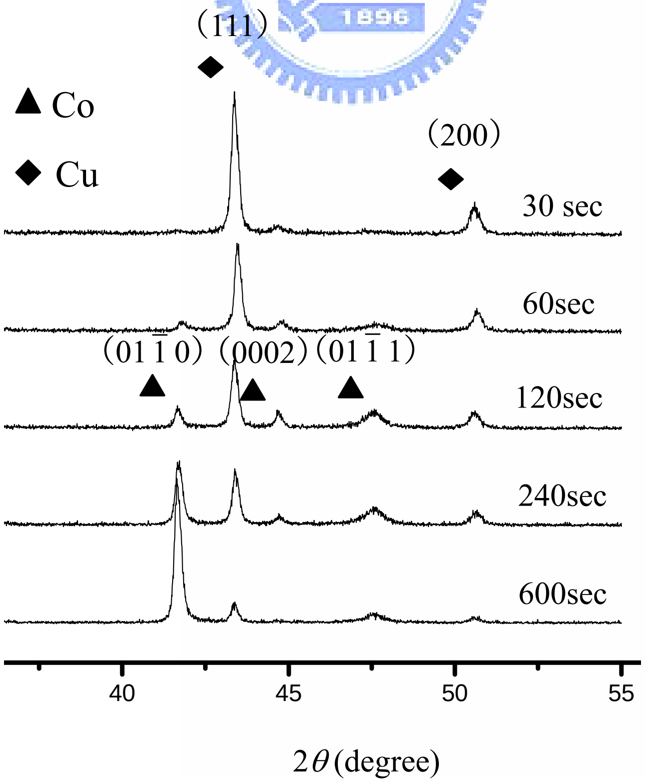


Fig. 4.25： XRD analysis performed on Co(P) films of different deposition times

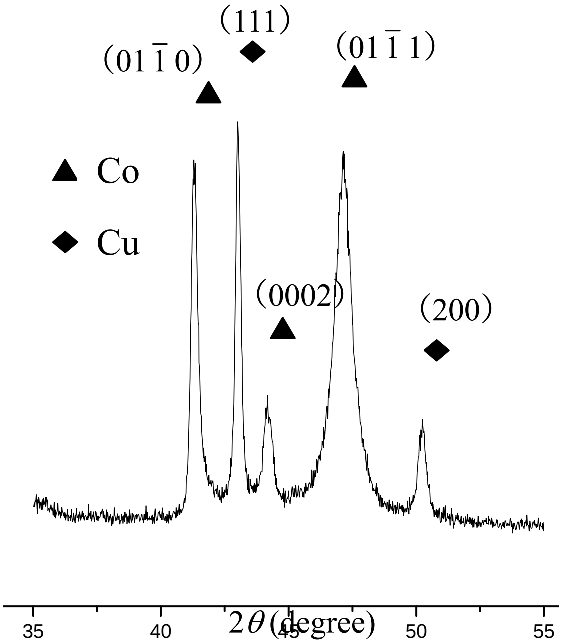


Fig. 4.26：XRD analysis performed on Co(P) films of 30 min deposition time

The grain sizes in Co(P) film can be estimated by using the Scherrer's formula[62] incorporating with the XRD peak information:

$$t = \frac{0.9\lambda}{B\cos\theta},$$

where t corresponds to the grain size of crystal, λ is wavelength of x-ray (= 0.154 nm), B represents half-height width of XRD peak, and θ represents the Bragg angle. The calculated grain sizes of the 60-sec and 30-min Co(P) layers were about 8.42 nm and 34 nm, respectively. Moreover, the 600-sec Co(P) layer formed a nanocrystalline structure with grain size of 20 to 30 nm. According to the EDX analysis (Table 4.8), the phosphorous content of the 30 sec disposition film reaches 14.98 *at.*%. As the phosphorous content decreases with the increase of disposition time, the structure of Co(P) film varied too. Because the concentration of $\left(HPO_2^-\right)_{ads}$ was at its maximum at the beginning of the electroless plating, the driving force for the reduction was also at its maximum and thus the amount of phosphorus being deposited was at its maximum in relative[26]. Since the plating process is a chemical reaction rather than a physical change, the phosphorous content in the plated film changes during the chemical reaction. The fact that the phosphorous content in the plated film decreases with the decrease of the concentration of $\left(HPO_2^-\right)_{ads}$ hence causes the microstructure change of the electroless plating film. It can thus be speculated that a Co(P) layer of amorphous structure formed at the beginning of the plating process is capable of retarding the diffusion of Sn and Cu atoms.

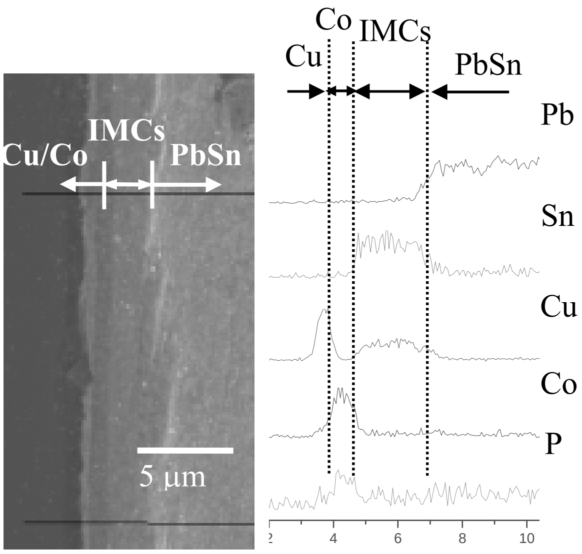
4-3.5. Interfacial Reactions of Electroless Co(P) Layer and Pb-Sn Solder

Since the specimens were treated at 250°C, which is higher than the eutectic temperature of Pb-Sn solder, thus the interfacial diffusion of present experiment was progressing in liquid state. The Cu wetting layer reacted with the Pb-Sn solder first and the intermetallic compounds (IMCs) produced. The IMCs produced under different duration of thermal treatment were subjected to EDX analysis and the result is shown in Table 4.9. It is noted that the ratio of Cu and Sn falls in the range of 1.5 to 2.0 such that the IMCs could be a mixture of Cu_6Sn_5 and Cu_3Sn. This emergence of Cu_3Sn phase should result from the prolonged thermal treatment at a temperature relatively higher than eutectic temperature of PbSn solder.

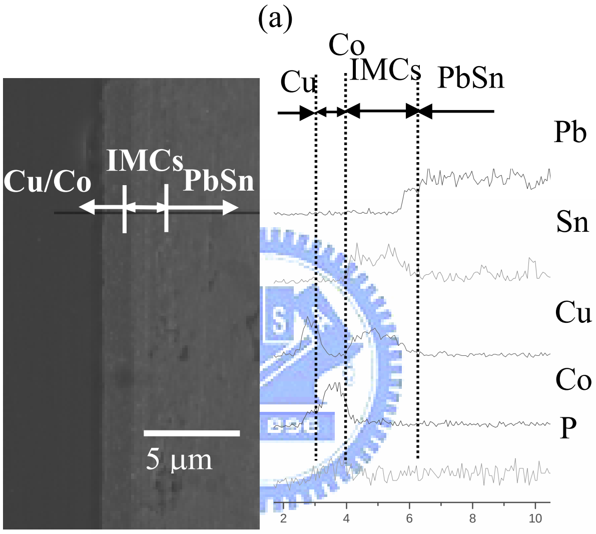
Table 4.9. EDX analysis of IMCs produced under different duration of thermal treatment.

Thermal duration (hrs)	Ratio (Cu/Sn)
0.5	2
6	1.65
18	1.73
24	1.56

Figures 4.27(a) and 4.27(b) present the cross-sectional SEM micrographs and results of EDX line scan for the 6-hr and 24-hr annealed specimens, respectively. In either case, the peak representing Sn abruptly decays when it reaches Co(P) layer. This evidences that Sn could not penetrate the Co(P) layer after such a liquid-state annealing and hence the Co(P) layer clearly serve as a good diffusion barrier of UBM structure. In the foregoing XRD analysis, it was speculated that the first formed Co(P) layer is high in phosphorous content and thus it should be amorphous. The fact that Sn could not penetrate Co(P) layer revealed in the EDX line scan analysis further proves the speculation. Moreover, it is noted that the peaks representing Co and Cu underlayer are separated without overlapping. Hence, the Cu cannot penetrate Co(P) layer too. Thus, the electroless Co(P) layer is able to serve as a good diffusion barrier of UBM structure for both Cu interconnects and solder bumping of flip-chip Cu-ICs.



(a)



(b)

Fig. 4.27： Cross-sectional SEM view of specimen interfaces and corresponding line scanning EDX analyses after 250°C (a) 6-hr and (b) 24-hr annealing.

Chapter 5 Conclusions

The intermetallic compounds formed after diffusion soldering as analyzed by EPMA are η-$(Cu_{0.99}Au_{0.01})_6Sn_5$ and δ-$(Au_{0.87}Cu_{0.13})Sn$ on the respective sides of Si and Al_2O_3. The activation energy for the $(Cu_{0.99}Au_{0.01})_6Sn_5$ intermetallic is 16.9 kJ/mol, which is near that for the diffusion of Cu in liquid Sn. The growth of $(Au_{0.87}Cu_{0.13})Sn$ presents an activation energy of 53.7 kJ/mol, a result in agreement with that for the lattice diffusion of Au in Sn, thus revealing that the rate-limiting step in the growth of $(Au_{0.87}Cu_{0.13})Sn$ is the diffusion of Au through the intermetallic compound. Tensile tests for the specimens diffusion-soldered at various temperatures for 20 min give a maximal value of 132 kg/cm^2 at the bonding temperature of 300°C, corresponding to the growth thicknesses of 1.63 μm and 1.46 μm for $(Cu_{0.99}Au_{0.01})_6Sn_5$ and $(Au_{0.87}Cu_{0.13})Sn$ intermetallic layers.

. Electroless plating films exhibited different grain morphologies on polished and unpolished AlN substrates. SEM observation revealed that on the polished AlN surface, plated metal films possessed less voids, finer grains, and better surface coverage than the films on the unpolished substrate. Also, their resistance was lower than that measured for the unpolished surface. SIMS analysis indicated that phosphorous content is the highest in the vicinity of the Ni/AlN interface and increases with increasing plating time. XRD characterization indicated the structure of the EN film should be a mixture of amorphous and microcrystalline grains. The pull-off test and shear test show that the adhesion strength and shear strength between the EN film and AlN substrate were higher than 761 kg/cm^2 and 100 g, respectively.

At the beginning of the plating process, the deposition rate of Co(P) layer was at its fastest since the concentration of plating bath was relatively high. The chemical reactions of electroless plating Co(P) indicates that the deposition rate increases with the increase of pH value. The AES and EDX analyses indicated that the phosphorous contents in Co(P) films decreases with the increase of film thickness and the average contents are no less than 8.68 *at.*% for the specimens. Though XRD in conjunction with composition analyses revealed that the electroless Co(P) layer prepared in this work was a mixture of amorphous and nanocrystalline structures. As revealed by the EDX line scan analysis, both Sn and Cu underlayer could not penetrate the electroless Co(P) layer in the PbSn/Cu/Co(P)/Cu/Ti/Si sample subjected to 250°C annealing in forming gas ambient for 24 hrs. The EDX analysis also indicated that, in addition to the formation of Cu_6Sn_5 and Cu_3Sn phases, diffusion of Co atoms into solder region was negligible.

The electroless Ni(P) or Co(P) layer has a step coverage and simultaneously serve as a diffusion barrier of Cu interconnects and UBM structure of flip-chip Cu-ICs. The excellent diffusion retardation ability of Ni(P) or Co(P) should result from the amorphous nature provided by the high-phosphorous content in electroless layer. Results in these experiments demonstrate that electroless plating and diffusion soldering are indeed excellent technology for UBM structure of flip-chip ICs.

Prospective research

From above discussion, we understand that electroless plating and diffusion soldering are indeed excellent technology for UBM structure of flip-chip ICs. However, to further strength the feasibility and enlarge the application of electroless plating and diffusion soldering, there are still some works had to do to make the technology more valuable. In order to make this paper to be more complete, there were related researches to be worth carrying on. The related suggestion are described as follows:

1 How to maintain electroless nickel or cobalt deposition constant?

I have a steady load on the electroless solution in surface area/volume and maintain the constant pH value. To get a constant plating rate, the plating system will use an automatic process controller for the future. One pump would remove some amount of the electroless bath, while the other adds components lost by chemical reaction. This should give a steady state in phosphorus content, breakdown products. To maintain a constant deposition we have to make sure that pH, temperature, nickel, cobalt and hypophosphite concentrations are kept within spec. Solution maintenance is performed by either continuous testing or by manual testing. Continuous testing allows for automatic replenishment of chemicals as needed. The cost of implemented and maintaining such a system can be high. Manual testing requires frequent testing, usually once an hour. The operator usually performs the testing and makes additions based on these results.

2 More microstructure details should be supplied by TEM.

Transmission Electron Microscopy (TEM) is a technique used for analyzing the morphology, crystallographic structure, and even composition of a specimen. TEM provides a much higher spatial resolution than SEM, and can facilitate the analysis of features at atomic scale (in the range of a few nanometers). For crystalline materials, the specimen diffracts the incident electron beam, producing local diffraction intensity variations that can be translated into contrast to form an image. So the more TEM data should be and discussed for the future research. Next, it was worth studying that Co-Ni-P alloy maybe can form a useful barrier layer too.

3 To integrate the application of electroless plating and diffusion soldering

To study thin-film reactions and reliability during diffusion soldering of electroless Cu/Ti/Si and Au/Cu/AlN with Sn interlayer, we can further integrate the process of electroless plating and diffusion soldering. The thermal-expansion coefficient of solder, wafer and substrate is different which the electroless layer caused cracks and Peeling, In addition the life time of the bath solutions is short in these experiment. The aluminum nitride substrate is carrying on the sensitization and activation so that causes its surface to form palladium adhesion. The palladium is easy to fall off from the aluminum nitride surface during the cleaning process. How to increase the adhesion of palladium and maintain electroless solutions will be worth studying diligently. Then, the application of sollar cell or flat panel display with different substrate may be a continuous research direction for electroless thin-film deposition.

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論文題目: 無電鍍沉積薄膜應用於銲錫擴散阻障層之研究

Investigation of Electroless Deposited Films as the Diffusion Barrier of Pb-Sn Solder

Publication Lists

A. Journal Papers

[1]. **M. W. Liang**, T. E. Hsieh, S. Y. Chang, and T. H. Chuang, "Thin-Film Reactions during Diffusion Soldering of Cu/Ti/Si and Au/Cu/Al_2O_3 with Sn Interlayers", J. Electron. Mater. , 32 (2003) 952.

[2]. **Muh-Wang Liang**, Tsung-Eong Hsieh, Chi-Chin Chen, and Yuan-Te Hung, "Electroless Copper/Nickel Films Deposited on AlN Substrates", Jpn. J. Appl. Phys. , 43 (2004) 8258.

[3]. **Muh-Wang Liang**, Hui-Ting Yen and Tsung-Eong Hsieh, "Investigation of Electroless Cobalt-Phosphorous Layer and Its Diffusion Barrier Properties of Pb-Sn Solder" , J. Electron. Mater. , 35 (2006) 1593.

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B. Conference Papers

[1]. Hui-Ting Yen, **Muh-Wang Liang** and Tsung-Eong Hsieh, "A Study of Electroless

Cobalt-Phosphorous Layer as the Barrier Layer in UBM for Flip-chip Cu-ICs", IMAPS-Taiwan 2006, pp.347-352 .