Analog Integr Circ Sig Process (2010) 62:9–15
DOI 10.1007/s10470-009-9321-y

CMOS voltage reference based on threshold voltage and thermal voltage

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Received: 19 April 2007 / Revised: 26 October 2007 / Accepted: 22 May 2009 / Published online: 11 June 2009

Abstract A fully CMOS based voltage reference circuit is presented in this paper. The voltage reference circuit uses the difference between gate-to-source voltages of two MOSFETs operating in the weak-inversion region to generate the voltage with positive temperature coefficient. The reference voltage can be obtained by combining this voltage difference and the extracted threshold voltage of a saturated MOSFET which has a negative temperature coefficient. This circuit, implemented in a standard 0.35-μm CMOS process, provides a nominal reference voltage of 1.361 V at 2-V supply voltage. Experimental results show that the temperature coefficient is 36.7 ppm/°C in the range from −20 to 100°C. It occupies 0.039 mm^2 of active area and dissipates 82 μW at room temperature. With a 0.5-μF load capacitor, the measured noise density at 100 Hz and 100 kHz is 3.6 and 25 $nV/\sqrt{Hz}$, respectively.

Keywords Voltage reference · Threshold voltage · Weak-inversion

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1 Introduction

The high-precision voltage reference circuit is one of most important components in mixed-mode applications. A stable reference circuit provides a reliable reference voltage, and low supply voltage makes the integration with low voltage digital circuits possible. Such reference circuits should exhibit little dependence on supply voltage, process parameters, and temperature. Many previous researches used BJT devices to implement reference circuits [1–4]. However, the BJT devices implemented in standard CMOS process occupy large chip area. Moreover, some of the reported solutions using non-standard CMOS processes require higher cost owing to extra process steps [5–9]. Thus, a novel voltage reference circuit that occupies small area in standard CMOS process would become very attractive. This paper discusses a voltage reference circuit by using MOSFETs. One part of the proposed circuit works in the weak-inversion region to provide the positive temperature coefficient current. The other part of the circuit, which works in the strong inversion region, is used to provide the negative temperature coefficient by extracting the threshold voltage. Thus, the positive and negative temperature coefficients would be summed to achieve a temperature independent reference parameter. The concept of the proposed voltage reference circuit will be illustrated and discussed in Sect. 2. Experimental results are presented in Sect. 3. Finally, Sect. 4 concludes the paper.

2 Proposed voltage reference circuit

2.1 V_{th} versus temperature for MOS transistors in the saturation region

The concept of our circuit starts from the fact that the threshold voltage varies with temperature. According to the

literatures [10–12], the magnitude of the threshold voltage V_{th} increases proportionally to the decrease of temperature. Therefore, we can model the relationship of the threshold voltage versus temperature as

$$|V_{th}(T)| = |V_{th}(T_0)| - \beta_{vth}(T - T_0) \quad (1)$$

where T_0 is the reference temperature and β_{vth} is a positive constant, i.e., the absolute temperature coefficient of the threshold voltage.

Figure 1(a) shows the negative temperature coefficient circuit, which extracts the threshold voltage of the MOSFET working in the saturation region. In the circuit, the transistor sizes of PMOS M1, M6, and M7 are the same. The transistor sizes of PMOS M4 and M5 are also the same, and their aspect ratio is set four times larger than that of M1, M6, and M7. The transistor sizes of NMOS transistors M2 and M3 are also equal to each other. M1, M2, and R_1 are used as the bias circuit to mirror the same drain current to M3, M4, M5, M6 and M7. The bulk and source terminals of transistors M4 and M6 are connected together to eliminate the body effect. From the square-law behavior of saturated MOSFETs,

$$V_{SG,M4} = V_{SG,M5} \quad (2)$$

In addition, when we neglect channel length modulation in a first approximation, we have:

$$V_{SG,M6} = 2V_{SG,M4} - |V_{th,p}| \quad (3)$$

where $|V_{th,p}|$ is the threshold voltage of the PMOS transistor. Thus, we can obtain the output voltage V_{outp} as

$$V_{outp} = V_{DD} - V_{SG,M5} - V_{SG,M4} + V_{SG,M6} \quad (4)$$

when we substitute (2) and (3) in (4), we obtain

$$V_{outp} = V_{DD} - |V_{th,p}| \quad (5)$$

Then, a unity gain buffer cascaded to the output node (source of M6) is used to provide the current with negative temperature coefficient. Thus, the output current of the circuit can be expressed as

$$I_{D8} = \frac{|V_{th,p}|}{R_2} \quad (6)$$

In practice, due to the temperature coefficient of R_2, the variation of I_{D8} deviates from the ideal equation. The temperature coefficient caused by resistors would be minimized and discussed in Sect. 2 *D*. Besides, channel length modulation would be an important issue and it would make I_{D8} a function of supply voltage, thus degrading PSRR performance of the circuit. Therefore, the device length of 6 μm was used for transistors M1 to M7. The simulated threshold voltage $V_{th,p}$ as a function of temperature is shown in Fig. 2: the temperature coefficient of −1.87 mV/°C is obtained over the range from −20 to 100°C. We can find that the threshold voltage would have the same slope with respect to temperature as shown in (1) from slowest to fastest corner conditions. However, the variation of the threshold voltage from slowest to fastest corner condition

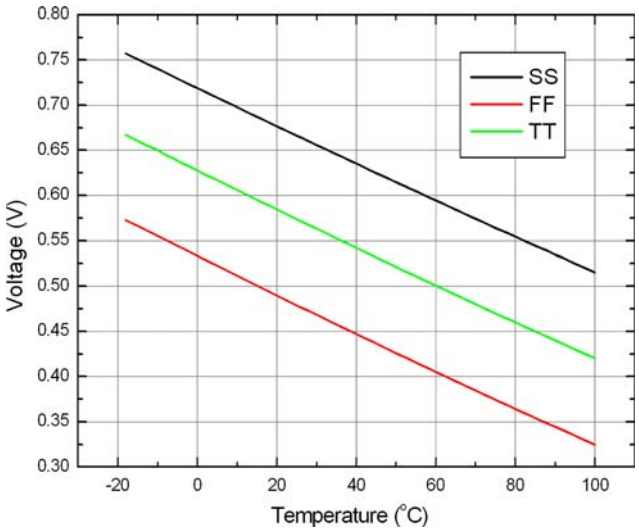

Fig. 2 Simulated PMOS threshold voltage versus temperature at different corner condition

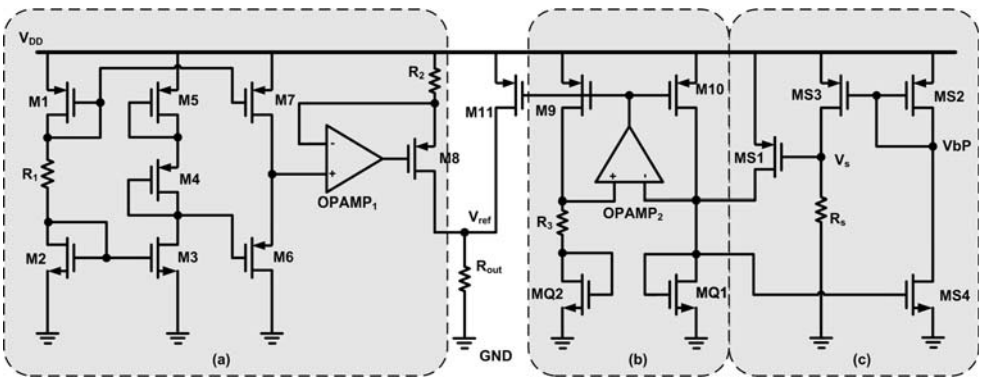

Fig. 1 Proposed voltage reference circuit

is about 0.2 V, which indicates a 16% variation for typical corner condition at room temperature. This variation would affect the output reference voltage, and the solution to the variation is addressed in Sect. 2.4.

2.2 PTAT current generation circuit

In order to generate a current with positive temperature coefficient, the circuit shown in Fig. 1(b) has been designed. The circuit works in the weak-inversion region. The drain current in the weak-inversion region can be expressed by [13]

$$I_D = I_{D0}\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}}{nV_t}\right) \quad \text{where} \quad V_t = \frac{kT}{q} \tag{7}$$

where the term n is the subthreshold slope factor and I_{D0} is a process-dependent parameter [13]. Very large aspect ratios of MQ1 and MQ2 are chosen to guarantee weak-inversion operation by ensuring

$$\frac{W_{Q1}}{L_{Q1}} > \frac{\mu_p C_{ox} W_{10}}{L_{10} I_{D0}} e^{\frac{-V_{th,n}}{nV_t}} \left(V_{DD} - \left|V_{th,p}\right|\right)^2 \tag{8}$$

where μ_p is the mobility of charge carriers of PMOS transistors, C_{ox} is the gate oxide capacitance per unit area, and W_{10}/L_{10} is the aspect ratio of M10. An operational amplifier with PMOS input stage is used owing to the low input common mode voltage of the PTAT current generation circuit under weak-inversion operation. The feedback loop formed in the circuit will force the gate voltage of MQ1 to be equal to the sum of the gate voltage of MQ2 and the voltage across resistor R_3. Therefore, the PTAT current can be obtained as

$$I_{D9} = I_{D10} = \frac{nV_t(\ln k)}{R_3} \tag{9}$$

where k is the ratio between the aspect ratios of MQ1 and MQ2.

2.3 Startup circuit

The proposed voltage reference circuit requires a startup circuit. The start up circuit shown in Fig. 1(c) provides the initial current until the voltage reference circuit reaches a suitable operating condition [14]. When the supply voltage is turned on, V_S voltage is equal to ground and thus turns MS1 on. The current provided by MS1 flows through MQ1 to start the operation of the voltage reference circuit and turn MS4 on, and then the current is mirrored by MS2 to MS3. The mirrored current will flow through R_4 to provide voltage larger than $V_{DD}-|V_{th,p}|$ to turn MS1 off. We should note that a weak startup current in the operational amplifier would introduce significant systematic offset, and this condition will affect correct operation of the voltage reference circuit. In order to solve this problem, we need to control the operational amplifier with the same reference current used in the voltage reference circuit. Thus, this tracking mechanism of currents in the input stage of operational amplifier and the PTAT current can eliminate the systematic effect at all of the operation phase. Since the startup circuit still works under nominal operation and consumes extra power, so a larger resistance value of R_S will be used. We should set the value of R_S as

$$R_S > \frac{V_{DD} - |V_{th,p}|}{C \times D \times I_{MQ1}} \tag{10}$$

where C is the current mirror ratio between the aspect ratios of MQ1 and MS4 and D is the current mirror ratio between the aspect ratios of MS2 to MS3. In addition, R_S was built by N-WELL, which has the property of large sheet resistance so as to reduce silicon area.

2.4 Circuit implementation

The complete schematic of the proposed voltage reference circuit is shown in Fig. 1, and the schematic of the OPAMPs is shown in Fig. 3. Currents proportional to positive and negative temperature coefficients are combined with current mirrors to obtain a temperature-insensitive voltage. From the circuit, the voltage reference is given by

$$V_{ref} = \left[\frac{|V_{th,p}|}{R_2} + B\left(\frac{nV_t(\ln k)}{R_3}\right)\right]R_{out} \tag{11}$$

where B is the current mirror ratio between the aspect ratios of M9 to M11. The reference voltage can be arbitrarily set to the desired value by choosing the value of Rout. The resistors R_2, R_3, R_{out} were fabricated by the same material, the N+ poly resistor, and thus the temperature coefficient caused by R_2 and R_3 could be minimized by dividing the temperature coefficient of R_{out}. Long channel devices are used for current mirrors to minimize channel length modulation. The temperature dependence of the voltage reference can be obtained by differentiating (11) with respect to temperature. Therefore, the proposed voltage reference circuit works at zero temperature coefficient operation under a first order approximation. The variation of threshold voltage under different corner conditions should be compensated. Since the output voltage is produced by combining the currents with positive and negative temperature coefficients, a simple trimming circuit composed by current mirror arrays can be used to solve this problem. Therefore, the number of the current mirrors can be designed by taking the 0.2 V voltage shift into consideration. The minimum supply voltage of the

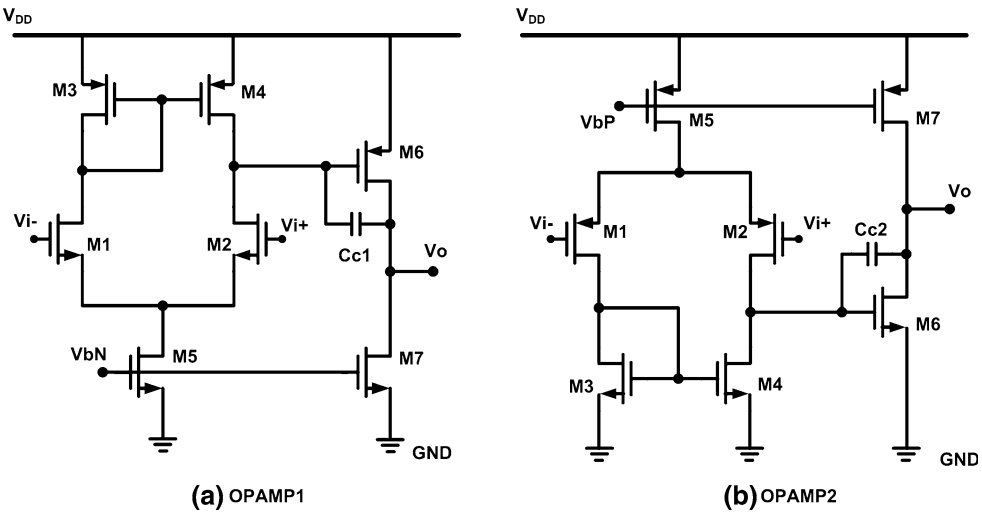

Fig. 3 The schematic of the OPAMPs

Table 1 Voltage reference component values

Component	Value
MQ1	5/0.35
MQ2	250/0.35
MS1	1/1
MS2	1/0.35
MS3	50/0.35
MS4	5/0.35
M1	12/6
M2	12/6
M3	12/6
M4	48/6
M5	48/6
M6	12/6
M7	12/6
M8	25/4
M9	20/4
M10	20/4
M11	200/4
R_1	350k
R_2	150k
R_3	114k
R_s	133k
R_{out}	75k

circuit would be limited by the threshold voltage extraction circuit, which is based on the saturated MOS operation. The largest threshold voltage would be obtained under the lowest temperature, and the minimum supply voltage could be expressed as

$$V_{DD,min} = 2V_{th,p} + 3V_{DS,Sat} \quad (12)$$

Thus, the supply voltage of the proposed voltage reference circuit can be down to 1.5 V with the considered 0.35-μm CMOS technology. Moreover, a low-threshold-voltage process can be used to achieve a lower power supply voltage.

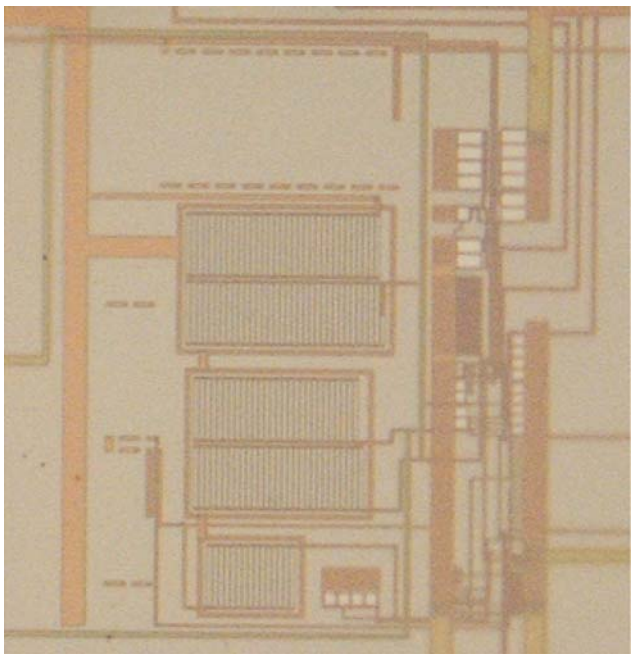

Fig. 4 Die microphotograph

3 Experimental results

The proposed voltage reference circuit has been implemented in TSMC 0.35-μm CMOS technology. The transistor aspect ratios and resistor values are reported in Table 1. The chip micrograph, which occupies an active area of 0.039 mm^2, is shown in Fig. 4. Careful layout is required to provide well matched circuits. Figure 5 shows

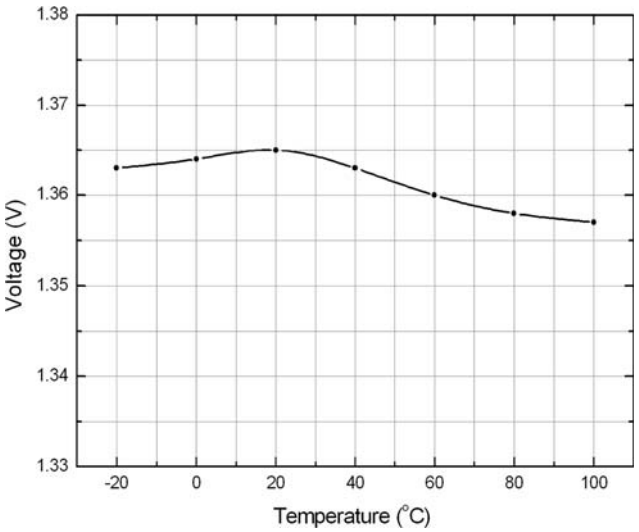

Fig. 5 Measured reference voltage versus temperature

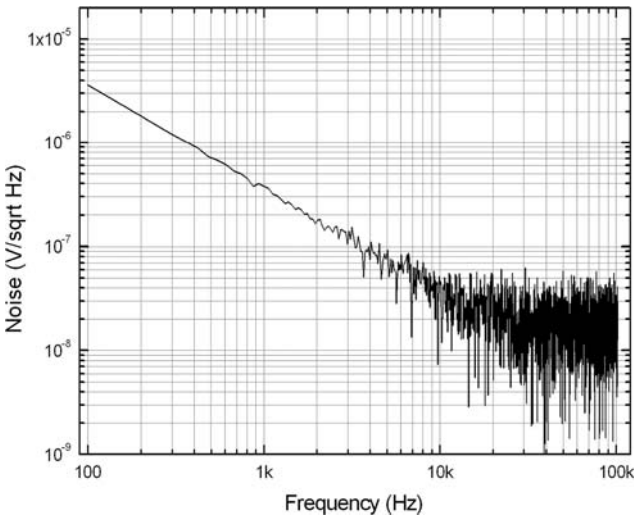

Fig. 6 Measured output noise spectral density of the proposed voltage reference circuit with 0.5 μF loading capacitance

the measured output voltage of the proposed voltage reference circuit as a function of temperature at 2 V supply voltage. In the figure, the measured mean value of the reference voltage is 1.361 V and the measured temperature coefficient is 36.7 ppm/°C in the range from −20 to 100°C. The current consumption of the circuit is 41 μA. The measured noise spectrum when connecting a 0.5-μF load capacitor is shown in Fig. 6. The measured noise density at 100 Hz and 100 kHz is 3.6 $\mu V/\sqrt{Hz}$ and 25 $nV/\sqrt{Hz}$, respectively. The noise produced in the voltage reference circuit is composed by two OPAMPs, the threshold voltage circuit, and the thermal voltage circuit. The complicated circuit introduces a good temperature effect, but suffers the problem of higher noise. As loading a capacitor at the output node, the output noise features a low-pass fashion. Then, the noise corner frequency would be dependent on the output impedance and the loading capacitance. The noise can be reduced by larger loading capacitance with the drawback of longer startup time. The measured performances of the voltage reference circuit, which are composed only by MOSFETs and resistors, are summarized in Table 2.

4 Conclusions

A voltage reference circuit based on CMOS technology has been presented. The threshold voltage of saturated MOSFET devices, which exhibits a negative temperature coefficient, can be obtained from the threshold voltage extraction circuit. On the other hand, the voltage difference between two gate-to-source voltages of MOSFET devices, which exhibits a positive temperature coefficient in weak-inversion, can be obtained from the PTAT current generation circuit. Currents having opposite temperature coefficients are provided and combined to obtain a voltage reference independent of temperature variation. This is done at the minimum cost of area and power consumption. The proposed voltage reference circuit can be easily

Table 2 Performance summary of the fabricated prototype

Parameter	[11]	[12]	[15]	[16]	[17]	[18]	This work
Technology (μm CMOS)	0.6	1.2	0.5	2	1.5	0.18	0.35
Supply voltage	1.4 V	1.2 V	2.8 V	5 V	3.3 V	0.85	2 V
Supply current (μA)	9.6	3.6	8	36	89	2.8	41
Reference voltage (V)	0.30931	0.2953	2.5	1.081	0.984	0.221	1.361
Temperature coefficient (ppm/°C)	36.9	119	360	92	57	271	36.7
PSRR	−47 dB @ 100 Hz	−40 dB @ 5 kHz	–	−34.5 dB @ 1 kHz	−43.2 dB @ 1 kHz	–	−43.5 dB @ 10 kHz
Active area (mm^2)	0.055	0.23	0.25	–	0.609	0.024	0.039

designed in CMOS technology and is suitable for many applications. The voltage reference circuit was fabricated in TSMC 0.35-μm CMOS technology. Experimental results report an output voltage of 1.361 V at 2 V supply voltage. A temperature coefficient of 36.7 ppm/°C is achieved over the range of −20–100°C, with a power consumption of 82 μW at room temperature.

Acknowledgments The authors would like to thank the National Chip Implementation Center of Taiwan for supporting the chip fabrication.

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