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Design of 2xVDD-tolerant mixed-voltage I/O buffer against gate-oxide reliability and hot-carrier degradation

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ABSTRACT

A new 2xVDD-tolerant mixed-voltage I/O buffer circuit, realized with only 1xVDD devices in deep-submicron CMOS technology, to prevent transistors against gate-oxide reliability and hot-carrier degradation is proposed. The new proposed 2xVDD-tolerant I/O buffer has been designed and fabricated in a 0.13-μm CMOS process with only 1.2-V devices to serve a 2.5-V/1.2-V mixed-voltage interface, without using the additional thick gate-oxide (2.5-V) devices. This 2xVDD-tolerant I/O buffer has been successfully confirmed by simulation and experimental results with operating speed up to 133 MHz for PCI-X compatible applications.

1. Introduction

With rapid development of complementary-metal-oxide-semiconductor (CMOS) techniques, the transistor dimension and core supply voltage have been continually scaled down to reduce chip area, to increase operating speed, and to reduce power consumption. Nonetheless, the scaled-down transistors also have the limitation of lower maximum tolerable voltage across the transistor terminals (drain, source, gate, and bulk) under vulnerable circuit operating conditions for lifetime concern. In the mixed-voltage I/O buffers, that interface the high-VDD signal environment of the old I/O specifications to low-VDD environment for low power consumption of core circuits, the voltages across transistor terminals should be managed carefully to overcome reliability problems, such as gate-oxide overstress [1,2], hot-carrier degradation [3–10], and the undesired circuit leakage paths (for the conduction of the parasitic drain-to-well pn-junction diode in the main pull-up PMOS device) [11,12,14].

The expected normal lifetime for IC products is generally specified as 5–10 years, which will be affected by different processes and overstress conditions. To ensure the circuits at least alive after continually overstress under certain worst-case circuit operating condition [13], transistors operating within 1–1.1 times of normal supply voltage in the I/O or driver circuits become a practical and common design principle [13–15]. Degradations caused by hot carriers and gate-oxide overstress are actually time dependent issues as discussed in [16–19], which are also functions of the probability for the happening of overstress condition during circuit operations. When the drain voltage of NMOS device is larger than its gate voltage (for the overstress condition in the following circuits under discussion), the drain avalanche hot carrier injection (DAHC) becomes an important mechanism [5]. For digital logic circuits, AC stress problems due to hot-carrier degradation and overstress in transition are also important to lifetime concern since barely transistors under turn-on state were with large DC drain-to-source stress on them [20,21]. For ensuring IC products to meet normal lifetime expectation, reliability problems in both of steady state and transition period should be considered.

The I/O circuits of prior arts those attempted to avoid reliability problems due to gate-oxide overstress and hot-carrier degradation have been reported in [13,14] and [22–26]. To realize the I/O buffer with 1.8/3.3/5-V mix-voltage tolerance without gate-oxide reliability issue, one prior design implemented with 3.3-V devices in a 0.35-μm CMOS process was reported in [22]. Besides, the dual-oxide (thick-oxide and thin-oxide) process [23–25] was also provided by foundry, that can be used to prevent the reliability anxiety in mixed-voltage interface against gate-oxide overstress and hot-carrier degradation. Two kinds of devices (such as 1-V and 2.5-V transistors) were also adapted to output 3.3-V signals without aforementioned reliability anxiety [26]. However, the chip fabrication cost is also increased by using the dual-oxide process with the additional mask layer and the corresponding process steps. In [14], an I/O buffer implemented with only thin-oxide devices was reported. However, some overstress problems still exist in the prior design [14] under some specified transitions, which will be further discussed in Section 2 of this paper.

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To alleviate the aforementioned reliability problems during both steady state and transition period in the mixed-voltage I/O buffer with only 1xVDD devices, a new 2xVDD-tolerant I/O buffer with novel transmitting circuit and new gate control circuit is proposed in this work [27] and successfully verified in a 0.13-μm CMOS process.

2. Hot-carrier degradation and gate-oxide reliability in the prior I/O circuits realized with thin-oxide devices

A conventional mixed-voltage I/O buffer with the gate-tracking circuit and the dynamic n-well bias circuit is shown in Fig. 1 [14]. The limitations of voltage difference within 1.1xVDD across the terminals of each transistor can be satisfied by the circuit in Fig. 1 under steady state. However, during the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the V_{ds} of transistors MN0 and MN3 will be much higher than VDD. The drain-to-source voltages of MN0 or MN3 start to increase from VDD, since the source terminal is pulled down faster than the drain terminal at the beginning of this transition period. The transistor MP5 also has larger V_{gs}, since its source and gate are connected to the drain and source of transistor MN0, respectively. Moreover, the transistors MN2 and MN3 also suffer similar problem during the transition from receiving 2xVDD input signal to transmitting VDD output signal. While PU signal is suddenly pulled down from VDD to 0, the drain terminal of MN2 is pulled down much slower since the transistors are turned on accordingly and it also takes time for the gate terminal of transistor MP2 to be pulled down from 2xVDD to turn on transistor MP2.

To solve the hot-carrier degradation problems happened in some prior arts in Fig. 1, a technique with three or more stacked NMOS transistors has been reported in [13]. A modified 2xVDD-tolerant I/O buffer circuit with this technique to eliminate hot-carrier issue is shown in Fig. 2. When the I/O buffer receives 2xVDD input signal, the gate terminals of transistor MN5 and MN6 are biased at 2xVDD through the transistor MPT1 and MPT3, respectively. Besides, the gate terminals of transistor MN5 and MN6 are biased at VDD if a VDD signal is transmitted or a 0-V signal appears on the output pad whether received or transmitted. During the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the source terminals of transistor MN5 and MN6

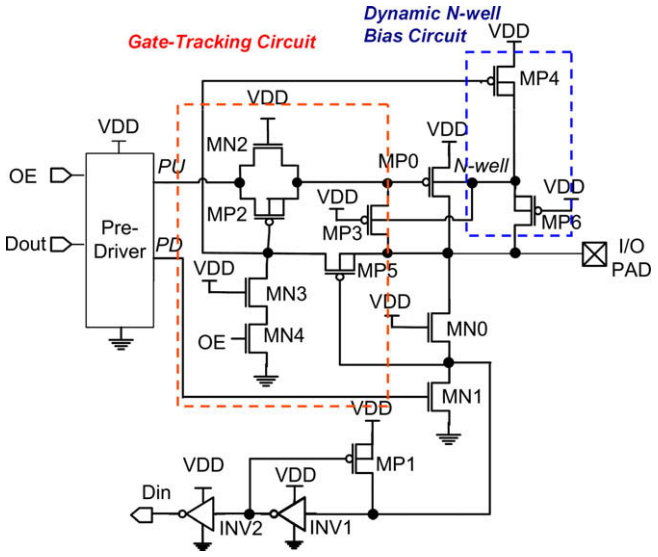

Fig. 1. The conventional mixed-voltage I/O buffer designed with gate-tracking circuit and dynamic n-well bias circuit to solve gate-oxide reliability issue [14].

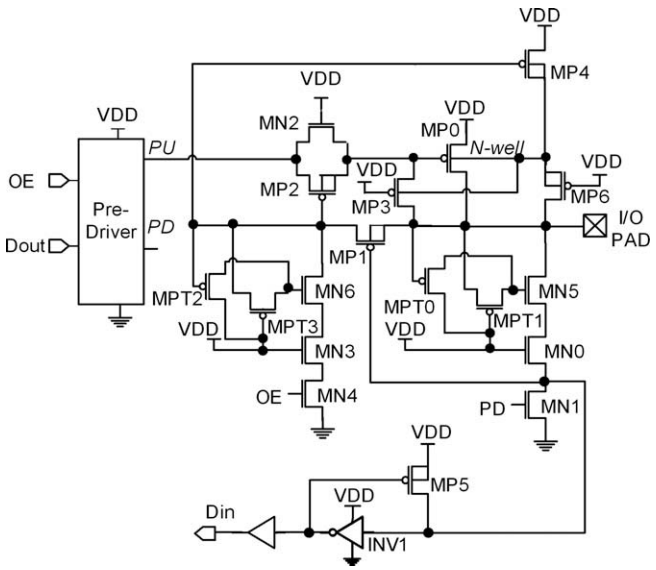

Fig. 2. The modified mixed-voltage I/O buffer designed with three-stacked transistors to prevent hot-carrier degradation [13].

are biased at 2xVDD-ΔV initially (where ΔV is the V_{ds} of the diode-connected transistors) since their diode connected structure due to same drain and gate voltage. In the meanwhile, the source

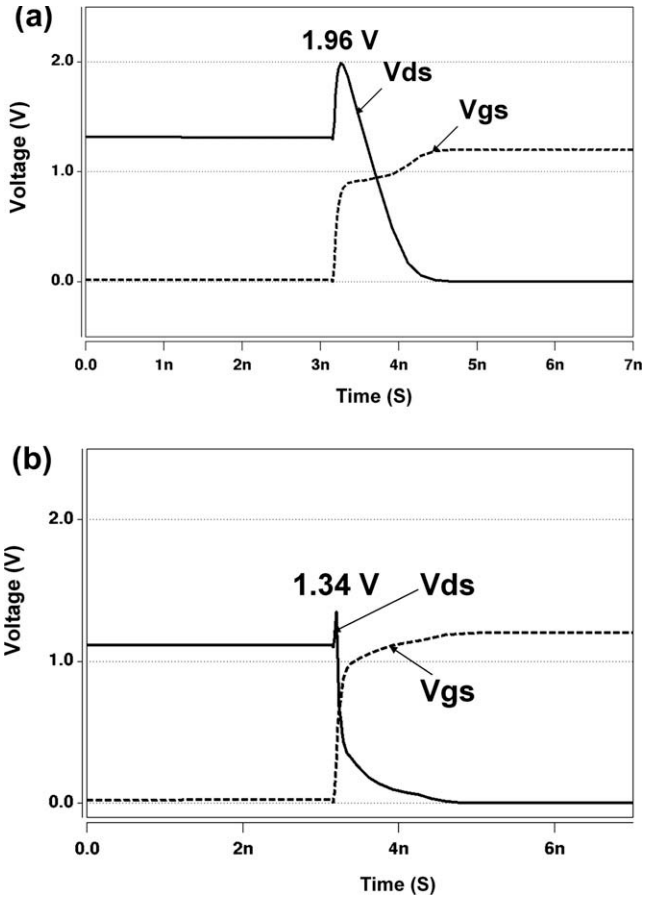

Fig. 3. (a) The simulated drain-to-source voltage (V_{ds}) of transistor MN0 (also the source-to-gate voltage (V_{sg}) of transistor MP5 in Fig. 1) and gate-to-source voltage (V_{gs}) of transistor MN0 during the transition from receiving 2xVDD input signal to transmitting 0-V output signal. (b) The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of transistor MN0 in Fig. 2 during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

terminals of transistor MN0 and MN3 are pulled down by transistor MN1 and MN4 in a 0.13-μm technology, respectively. Comparing the transistor MN0 and MN3 in Fig. 1 with the same transistors in Fig. 2 during this transient time, the transistors in Fig. 2 have smaller V_{ds} since the drain voltage is initially smaller by $-\Delta V$.

The above mentioned transient situations for transistors MN0, MN3, MP5, MN2 with high voltage across drain and source terminals or high gate-to-source voltage are verified by the HSPICE simulations in a 0.13-μm CMOS technology with VDD of 1.2 V and 2xVDD of 2.5 V. The model used in the simulation is BSIM3 (V3.2) provided by foundry, and that has been widely used for customers to design and produce of IC products. The corresponding HSPICE simulation results for the prior arts of Figs. 1 and 2 in a 0.13-m CMOS process with VDD of 1.2 V are shown in Figs. 3–7 .

As shown in Figs. 3a, 4a, 5a, and 6a, V_{ds} of transistor MN0 (also the V_{sg} of transistor MP1), MN3, MN2 in Fig. 1 are much larger than VDD with device operated in saturation mode during this period. The peak values are 1.96 V, 2.11 V, 2.09 V and 2.07 V, respectively. Thereby, it results in serious hot-carrier degradation or gate-oxide overstress in the transition from receiving 2.5-V input signal to transmitting 0-V or 1.2-V output signal.

With smaller overshooting voltage of V_{ds}, the I/O buffer in Fig. 2 can almost eliminate serious hot-carrier degradation happened in previous arts as shown in Figs. 3b, 4b, and 5b. However, the gate-oxide overstress still happens in the transistor MP1 in Fig. 2 during the transition from receiving 2xVDD to transmitting 0 V, as shown in Fig. 7. Also, transistor MN2 of the transmission circuit in Fig. 2 still suffers the hot-carrier degradation, as that shown in Fig. 6b.

3. New proposed mixed-voltage I/O buffer

The new proposed 2xVDD-tolerant I/O buffer realized with only 1xVDD devices to prevent transistors against gate-oxide reliability and hot-carrier degradation is shown in Fig. 8, which keeps the major design advantages of the prior arts with three additional new modifications. The design concepts of the major parts in this new proposed I/O buffer are introduced in the following.

3.1. Circuit operation

The basic structure for this mixed-voltage I/O buffer typically includes a pre-driver, a dynamic n-well bias circuit, two or three-stacked transistors, gate-tracking circuit, and an input stage unit, which is controlled by an enable signal OE. The circuit operating modes include a receive mode (for receiving input signal from I/O pad) and a transmit mode (for transmitting output signal to I/O pad). The corresponding circuit operating voltages in the proposed 2xVDD-tolerant I/O buffer circuit in Fig. 8 are listed in Table 1.

3.2. Gate control circuit

Dynamic floating n-well technique is applied to the mixed-voltage I/O circuit to prevent the possible leakage current path in the PMOS transistors of the pull-up network. By surveying the voltage waveform of the floating n-well, the floating n-well voltage is kept at VDD on one hand in receiving 0-V input signal from I/O pad and

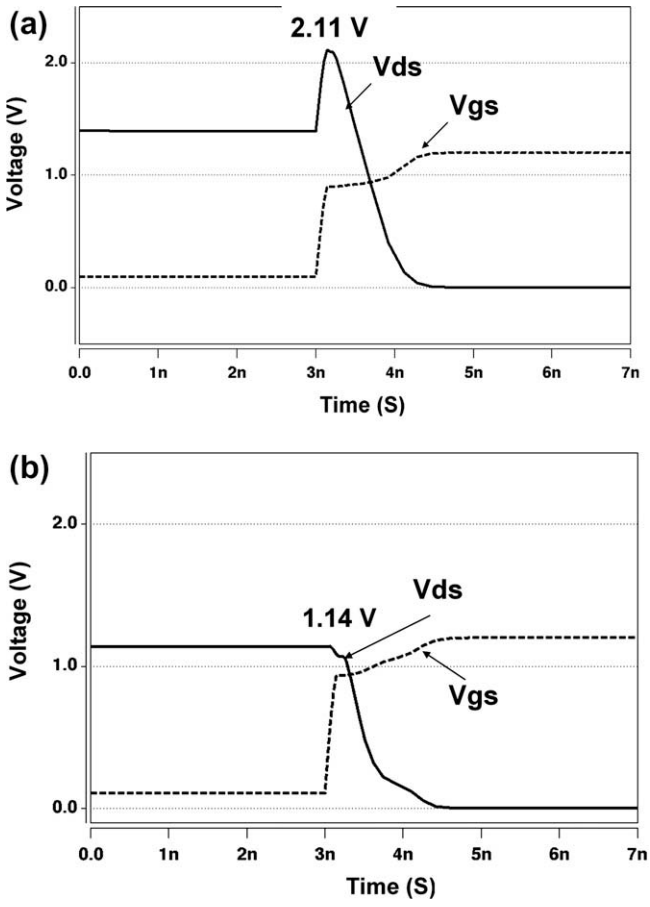

Fig. 4. The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of transistor MN3 in (a) Fig. 1, and (b) Fig. 2, during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

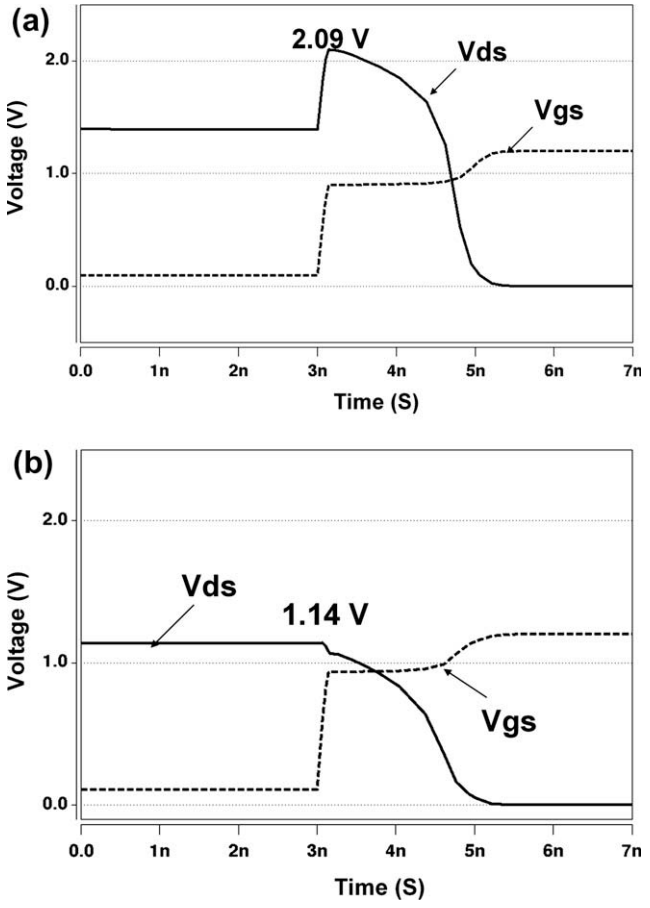

Fig. 5. The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of transistor MN3 in (a) Fig. 1, and (b) Fig. 2, during the transition from receiving 2xVDD input signal to transmitting VDD output signal.

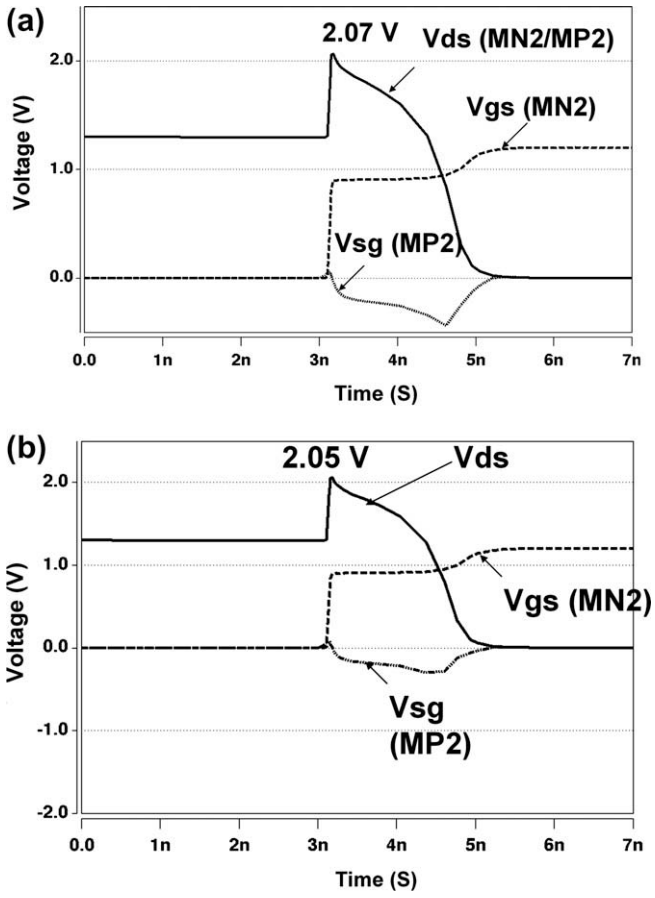

Fig. 6. The simulated drain-to-source voltage (V_{ds}) of transistor MN2/MP2 and the gate-to-source (V_{gs}) or source-to-gate voltage (V_{sg}) of MN2/MP2 in (a) Fig. 1, and (b) Fig. 2, during the transition from receiving 2xVDD input signal to transmitting VDD output signal.

in transmit mode. On the other hand, it is kept at 2xVDD for receiving input signal of 2xVDD from the I/O pad. Such a voltage level at the floating n-well presents a similar function to the gate control signal for the top transistor (MN5 and MN6) of the three-stacked NMOS structures in Fig. 2. Therefore, the new gate control circuit of these transistors can be directly implemented by the dynamic floating n-well self-biased circuit to save silicon area.

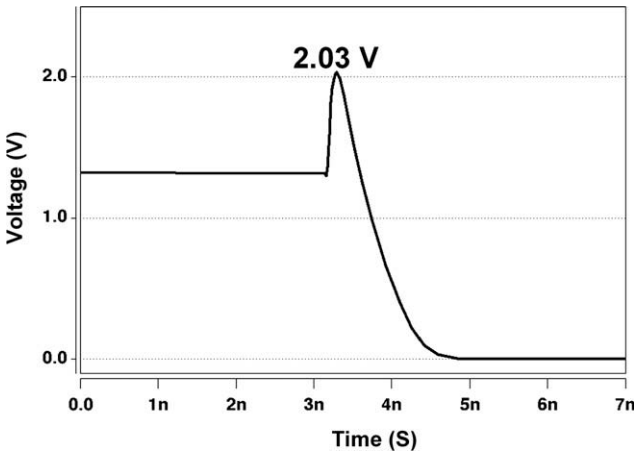

Fig. 7. The simulated source-to-gate voltage (V_{sg}) of transistor MP1 in Fig. 2 during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

3.3. Transmitting circuit

The new transmitting circuit applies the "stacked" concept in both PMOS and NMOS transistors appropriately to create a new "stacked transmission gate." As shown in Fig. 8, the gate terminal of MN2 is connected to VDD and the gate terminal of MN7 is connected to the floating n-well terminal, so are MN5 and MN6. Aside from NMOS transistors, the gate terminals of other two PMOS transistors, MP2 and MP7, are connected together to the drain terminal of MN6. In the transmit mode, the transistors MN7 and MP7 serve as a transmission gate (similar to MN2 and MP2). When receiving an input signal of 2xVDD at I/O pad, transistors MP2 and MP7 are turned off and the transistors MN7 and MN2 prevent high drain-to-source voltage (V_{ds}). During the transition from receiving an input signal of 2xVDD to transmitting an output signal of VDD, the drain voltage of transistor MN2 keeps at 2xVDD-ΔV initially due to the diode-connected transistor MN7 (where ΔV is the V_{ds} of the diode-connected transistor MN7). Then, it keeps a lower V_{ds} across MN2 and MP2 when the source voltage of MN2 starts to be pulled down to 0 V. Due to the lower V_{ds} of the stacked structures, the mentioned hot-carrier degradation problem in the transmission gates of Figs. 1 and 2 does not happen in this new design. Moreover, since the gate voltage of MP2 and MP7, and the drain and source terminals of MN7 are pulled down to 0 V while the gate terminal of MP0 is pulled down to 0 V, the gate-to-source voltages

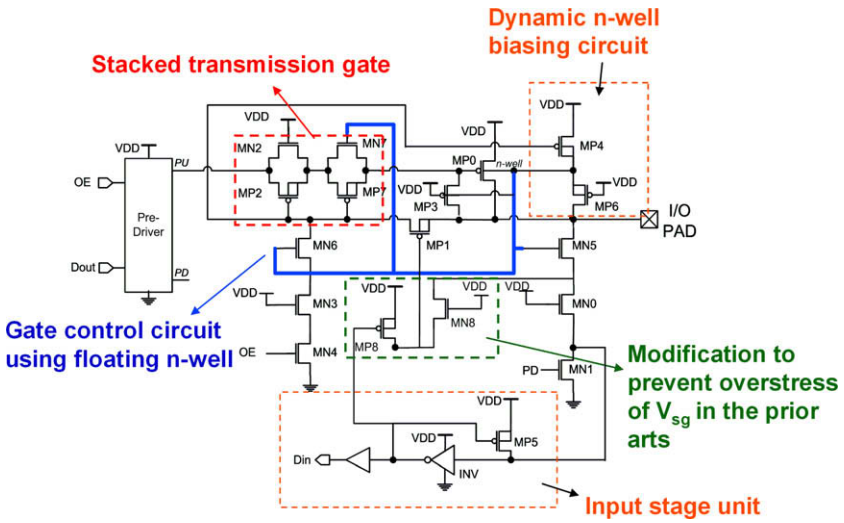

Fig. 8. The new proposed 2xVDD-tolerant I/O buffer realized with only 1xVDD devices to prevent transistors against gate-oxide overstress and hot-carrier degradation [27].

Table 1
Operations of the new proposed 2xVDD-tolerant I/O buffer in the receive/transmit states.

Operating modes	Signals at I/O pad	PU	PD	Voltage level of the floating n-well
Receive mode	Low (0 V)	VDD	0	VDD
Receive mode	High (2xVDD)	VDD	0	2xVDD
Transmit mode	Low (0 V)	VDD	VDD	VDD
Transmit mode	High (VDD)	0	0	VDD

and the gate-to-drain voltages of MN7, MP7, MN2 and MP2 keep in a safe region (around or lower than 1.1xVDD). Thus, the new transmitting circuit does not suffer hot-carrier degradation and gate-oxide overstress problems.

3.4. Modification to prevent gate-oxide overstress

In Fig. 1, the gate terminal and the source terminal of transistor MP5 are connected to the drain terminal and the source terminal of MN0, respectively. In Fig. 2, the gate terminal and the source terminal of the MP1 are connected to the source terminal of MN0 and the drain terminal of MN5, respectively. During the transition from receiving an input signal of 2xVDD to transmitting an output signal of 0 V, transistor MN0 in Fig. 1 suffers hot-carrier degradation and the voltage difference between the drain terminal of MN5 and the source terminal of MN0 in Fig. 2 is much larger than VDD, therefore transistor MP5 in Fig. 1 and transistor MP1 in Fig. 2 also suffer gate-oxide reliability problem.

To solve such a problem, the gate terminal of MOS transistor can be connected to an appropriate node instead of the original one, which is the source terminal of MN0 in Figs. 1 and 2. In Fig. 8, the appropriate point is realized by the additional connection of a PMOS transistor and an NMOS transistor. Transistor MN8 provides similar function as transistor MN0 with smaller size, and transistor MP8 works similarly as transistor MP5. With the similar structure, the gate terminal of transistor MP1 receives similar voltage as that of transistor MP1 in previous design. In the receive mode, the gate voltage of transistor MP1 is conducted to VDD (for 2xVDD input signal from I/O pad) or 0 V (for 0-V input signal from I/O pad) by transistor MN8 and MP8, respectively. In the transmit mode, the gate voltage is conducted to 0 V or VDD as the drain terminal of transistor MN1 does. However, since the gate terminal of transistor MP1 does not drop to ground as immediately as the drain terminal of transistor MN1 does, large V_{sg} value does not occur in transistor MP1. The gate voltage of transistor MP1 is pulled down gradually by MN8 and the other NMOS transistors when transition from receiving 2xVDD input signal to transmitting 0-V output signal. Thus, the new proposed design does not suffer gate-oxide reliability problem in both steady state and transient state. The ability to eliminating mentioned transient reliability problem, circuit complexity and area of this work and few prior arts are briefly compared in Table 2.

Table 2
Comparisons on reliability concerns and circuit complexity among the prior arts and this work.

Reliability performance	Hot-carrier degradation (in transient state)	Gate-oxide overstress (in transient state)	Circuit complexity	Area
Prior art in Fig. 1 [14]	Yes	Yes	Simple	Smaller
Modified I/O buffer in Fig. 2	Yes	Yes	Medium	Medium
Prior art with thick- oxide device	No	No	Simple	Larger
This work	No	No	Medium	Medium

4. Simulation results

4.1. Simulated waveforms for steady state operation and verification to new modifications

The simulated results of the new proposed 2xVDD-tolerant I/O buffer to prevent hot-carrier degradation and gate-oxide reliability have been verified by the HSPICE simulation in a 0.13-μm CMOS BSIM3 model (V3.2) with VDD of 1.2 V. The sizes for transistors

Table 3
Sizes of transistors used for the simulation in this work.

Transistors in this work	Device	Width (μm)/ length (μm)
Transistors for main pull-up and pull-down path	MN0, MN1, MN5	82/0.13
	MP0	180/0.13
Other PMOSs and NMOSs	MN3, MN4, MN6	0.68/0.13
	MN8	1/0.13
	MP8	0.45/0.13
	MP1, MP3, MP6	4.05/0.13
	MP4	36.45/0.13
	MP2, MP7	8.1/0.13
	MN4, MN8	2.7/0.13
	MP5	0.45/0.13

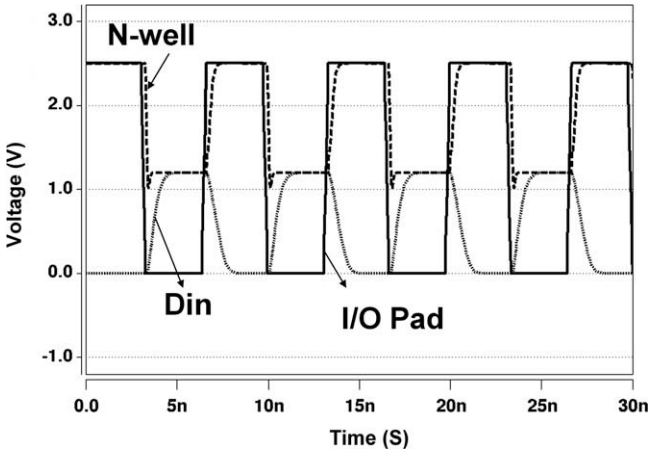

Fig. 9. Simulated waveforms of the proposed mixed I/O buffer (this invention) operating at 150 MHz when receiving 2.5–0-V input signals at I/O pad.

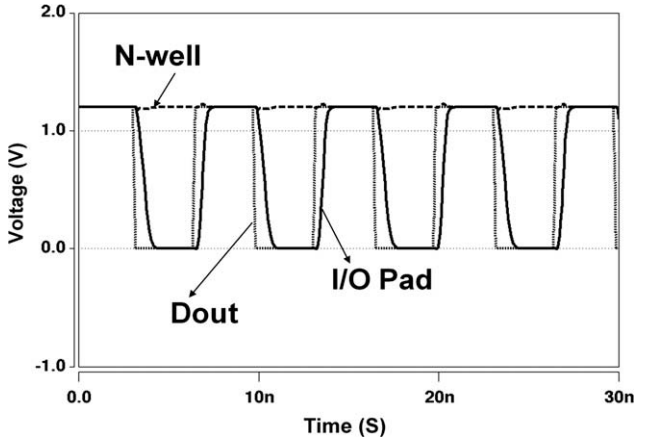

Fig. 10. Simulated waveforms of the proposed mixed I/O buffer (this invention) operating at 150 MHz when transmitting 1.2–0-V output signals at I/O pad.

are listed in Table 3. Figs. 9 and 10 show the simulated waveforms of the new proposed 2xVDD-tolerant I/O buffer well operating with speed of 150 MHz in the receive mode and transmit mode, respectively. As shown in Fig. 9, when new proposed mixed-voltage 2xVDD I/O buffer receives 0-V and 2.5-V signal from I/O pad, it successively outputs 1.2-V and 0-V Din signal with n-well voltage biased at 1.2 V and 2.5 V, respectively. In Fig. 10, as Dout signal varies between 1.2 V and 0 V, new proposed I/O buffer transmits similar swing to I/O pad accordingly and n-well voltage keeps near 1.2 V.

Fig. 11 shows the V_{ds} and V_{gs} of MN0 in the new proposed I/O buffer from receiving 2.5-V input signal to transmitting 0-V output signal. Fig. 12a and b shows the V_{ds} and V_{gs} of MN3 in the new proposed I/O buffer from receiving 2.5-V input signal to transmitting 0-V or VDD output signal, respectively. Comparing Figs. 11 and 12a and b with previous figures (Figs. 3a and b, 4a and b, and 5a

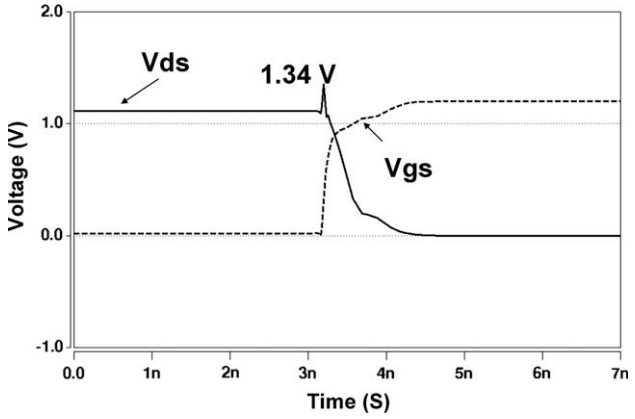

Fig. 11. The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of MN0 in the new proposed I/O buffer during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

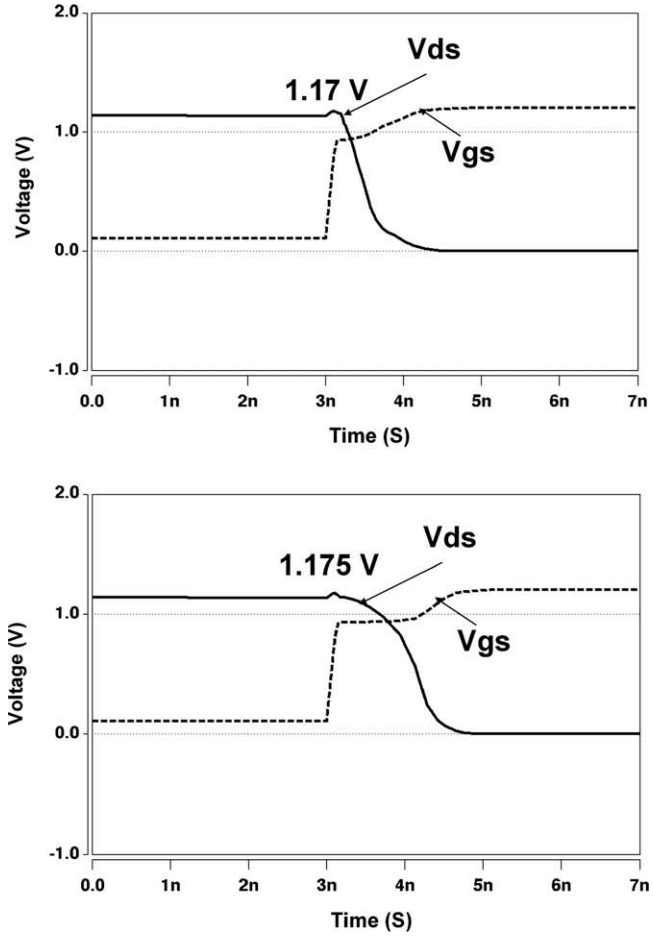

Fig. 12. The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) of MN3 in the new proposed I/O buffer during the transition from receiving 2xVDD input signal (a) to transmitting 0-V output signal and (b) to transmitting VDD output signal.

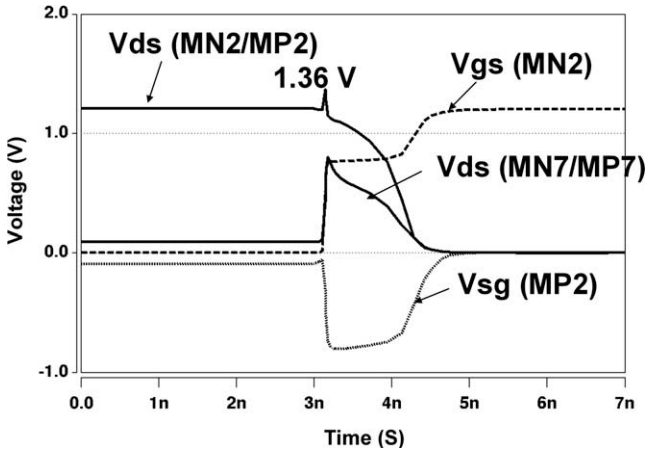

Fig. 13. The simulated drain-to-source voltage (V_{ds}) and gate-to-source voltage (V_{gs}) or source-to-gate voltage (V_{sg}) of transistors in the new transmitting circuits of new proposed buffer during the transition from receiving 2xVDD input signal to transmitting VDD output signal.

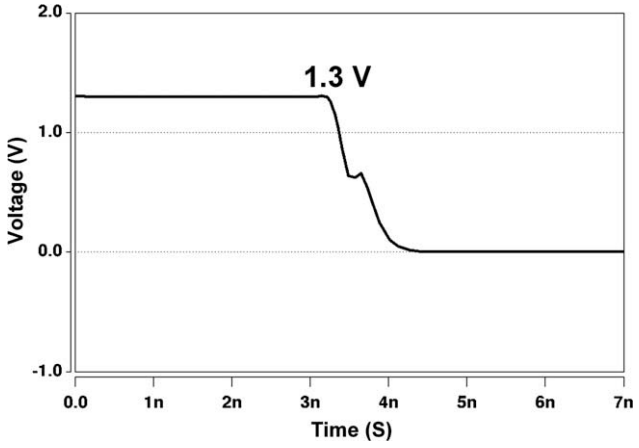

Fig. 14. The simulated gate-to-source (V_{gs}) voltage across transistor MP1 in the new proposed I/O buffer during the transition from receiving 2.5-V to transmitting 0-V output signals.

Table 4
Comparisons on transition times of receive/transmit operations among the prior arts and the new proposed I/O buffer with 150 MHz at 85 °C.

Mixed-voltage I/O buffer	Receive mode		Transmit mode	
	Rise time (ns)	Fall time (ns)	Rise time (ns)	Fall time (ns)
Prior art in Fig. 1 [14]	0.73	0.85	0.4	0.8
Modified I/O buffer in Fig. 2	0.71	0.88	0.4	1.38
This work	0.75	0.91	0.4	0.65

Table 5
Comparisons on propagation delay of receive/transmit operations among the prior arts and the new proposed I/O buffer with 150 MHz at 85 °C.

Mixed-voltage I/O buffer	Receive mode			Transmit mode		
	tphl (ns)	tplh (ns)	tp (ns)	tphl (ns)	tplh (ns)	tp (ns)
Prior art in Fig. 1 [14]	0.38	0.45	0.42	0.65	0.45	0.55
Modified I/O buffer in Fig. 2	0.42	0.47	0.45	1.1	0.46	0.78
This work	0.39	0.51	0.45	0.56	0.48	0.52

Table 6
Comparisons on the root-mean-square current of receive/transmit operations among the prior arts and the new proposed I/O buffer with 150 MHz at 85 °C.

Mixed-voltage I/O buffer	Receive mode (mA)	Transmit mode (mA)
Prior art in Fig. 1 [14]	0.88	7.56
Modified I/O buffer in Fig. 2	0.95	7.29
This work	1.17	7.28

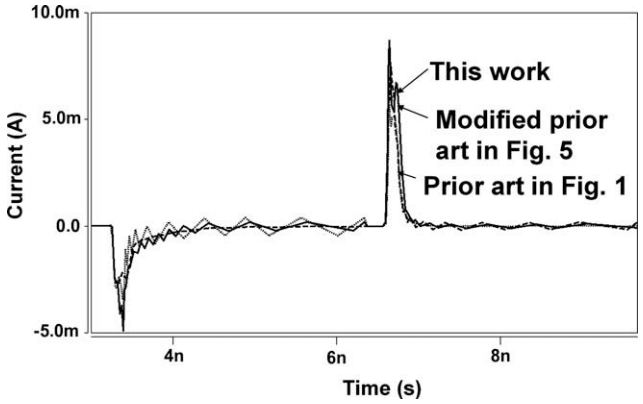

Fig. 15. Current of VDD in receive mode at 85 °C for one period of 150 MHz 0-to-2xVDD swing received at I/O pad.

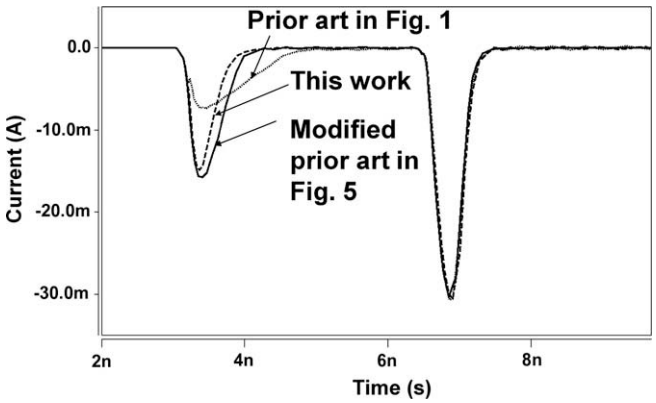

Fig. 16. Current of VDD in transmit mode at 85 °C for one period of 150 MHz 0-to-VDD swing transmitted at I/O pad.

and b) correspondingly, MN0 and MN3 in Fig. 1 suffer serious hot-carrier degradation problem due to the larger V_{ds}. Since the drain-to-source voltage of MN0 and MN3 are nearly the same for the new buffer shown in Fig. 8 and the buffer shown in Fig. 2, the capabilities of preventing hot-carrier degradation when receiving 2.5-V input signal are almost the same between these two buffers (Figs. 2 and 8). However, the new buffer is more efficient in area saving.

Fig. 13 shows the V_{ds} and V_{gs} (or V_{sg}) waveforms of the transistors in the transmitting circuit of the new proposed I/O buffer from receiving 2.5-V input signal to transmitting 1.2-V output signal. As shown in Fig. 13, the transistors in the new proposed I/O buffer have lower drain-to-source voltage, which is more robust to prevent hot-carrier degradation.

Fig. 14 shows the gate-to-source voltages of transistor MP1 in the new proposed I/O buffer. The peak V_{sg} value of similar PMOS in the prior designs is larger than VDD of 1.2 V as shown in Figs. 2 and 8. However, the V_{sg} of MP1 in the proposed I/O buffer is close to VDD, which is confirmed more robust than the previous designs in both hot-carrier degradation and gate-oxide reliability.

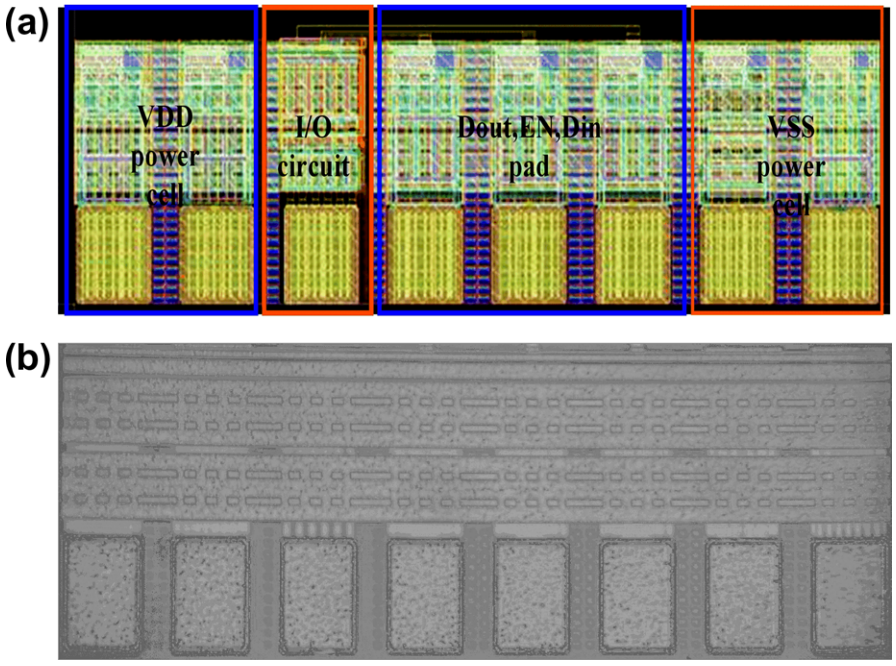

Fig. 17. (a) Layout-top-view of test chip to verify the new proposed 2xVDD-tolerant I/O buffer in a 0.13-m CMOS process. (b) Die photograph of the test chip for the new proposed I/O circuit fabricated with 0.13-m 1.2-V CMOS process.

4.2. Rise time, fall time and propagation delay in the new proposed I/O buffer and prior arts

The cost to maintain the driving ability is to size each main driving NMOS transistor of the prior art 2 and the new design to 1.5 times comparing with prior art 1 and size the transmission gate of the new design to 2 times of the other two prior arts. With such adjustment, the results of the rise time (tr), fall time (tf) and the propagation delay (from high to low: tphl, from low to high: tplh, and the average of tphl and tplh: tp) of the new proposed I/O buffer and the two prior arts are shown in Tables 4 and 5. The fall time and propagation delay of the modified I/O buffer in Fig. 2 are slightly longer than the new proposed design and the prior art in Fig. 1. The reason is attributed to the additional output loading due to MPT1 and MPT0 in Fig. 2. However, effective output loading at I/O pad of prior art in Fig. 1 is not significantly smaller than the new proposed buffer and the modified I/O buffer in Fig. 2, since the extra 10 pF capacitor at the I/O pad due to package is the dominant part in the simulation. The transition performance including rise time, fall time, and propagation delay have no obvious difference among the three circuits under proper sizing.

4.3. Power performance of the new proposed I/O and prior arts

The power consumption is compared in Table 6 with 0.13-μm CMOS model, and the root-mean-square (rms) current of the supply voltage is adopted as reference. The current of supply voltage in one period (6.68 ns for 150 MHz) for both receive and transmit modes are also shown in Figs. 15 and 16. According to the simulated results in transmit mode, the rms current of the supply voltage is similar among the three buffers, but the new buffer has slightly smaller value. In the receive mode, the rms power consumption of the new buffer is slightly larger than that of the two prior arts. The power consumption of I/O buffer in transmit mode is usually much larger than the current in receive mode because the whole buffer is required to drive large capacitance at I/O pad to deliver the swing signal. But in receive mode, besides the receiving path only few nodes is charged or discharged to prevent leakage problems, the power is mainly delivered to the core circuit from received signal at I/O pad. Thus, the new buffer has similar power performance in the receive mode.

5. Experimental results

The new proposed mixed-voltage 2xVDD-tolerant I/O buffer has been fabricated in a 0.13-μm 1.2-V CMOS process with only thin-oxide (1.2-V) devices. The layout-top-view and the die photograph of test chip are shown in Fig. 17a and b with the corresponding circuit blocks, including VDD power cell, I/O circuit, Dout pad, EN pad, Din pad, and VSS power cell.

The signals appear in the pins of fabricated chip are measured by the oscilloscope with the sampling rate of 5 GS/s and a bandwidth of 500 MHz. Fig. 18 shows the measured waveforms of the proposed 2xVDD-tolerant I/O buffer in the receive mode to receive the 1-MHz input signals with voltage swing of 0-to-2.5 V at I/O pad, where the input data has been successfully transmitted to Din with a voltage swing of 0-to-1.2 V. Fig. 19a and b shows the measured waveforms at the I/O pad in the transmit mode to transmit the 10-kHz and 133-MHz output signals with a voltage swing of 0-to-1.2 V given at Dout, respectively. Some imperfectness of the measured waveforms can be attributed to the buffer size in the I/O cell, parasitic and loading effect of the PCB board. Cable line, connections and impedance matching of the input and output of the PCB board, oscilloscope and wave generator also cause effects such as ripples or delay.

To measure reliability performance as lifetime is not an easy task especially for circuits required tens or hundreds of years to be failure. The setup and the maintenance of the experimental condition violate the results as well. One approach to test the

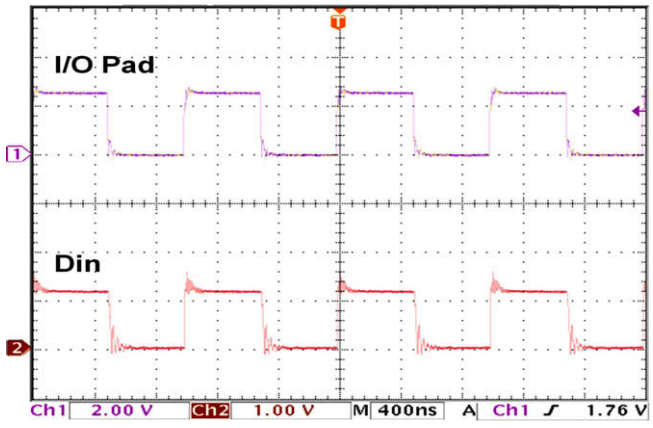

Fig. 18. Measured waveforms of the proposed 2xVDD-tolerant I/O buffer operating at VDD of 1.2 V when receiving 0–2.5-V input signals at I/O pad.

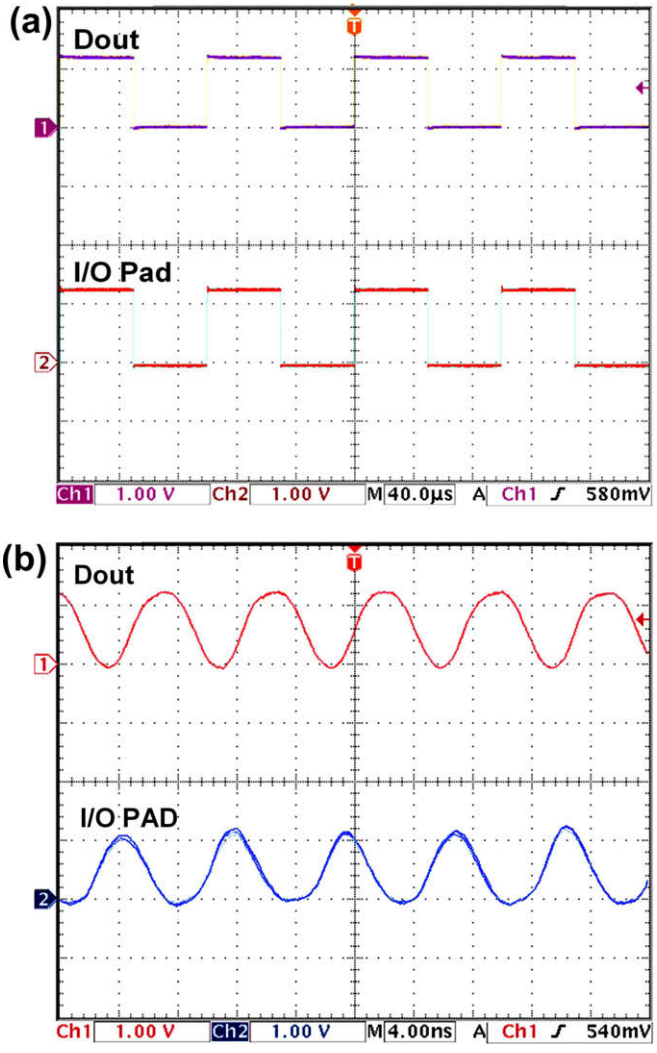

Fig. 19. Measured waveforms at I/O pad of the proposed 2xVDD-tolerant I/O buffer operating at VDD of 1.2 V when transmitting 0–1.2-V output signals at (a) 10 kHz and (b) 133 MHz.

reliability of a circuit is to find out critical transistors that attribute to the reduction of the lifetime or performance. Then, simplify the reliability test to device level with specified biasing condition and apply overstress method to predict lifetime based on measured results. For the impracticality to insert pads for measuring the real voltage difference for certain transistors in the I/O buffer, the help of simulation is necessary. Since the researches on device-level reliability problem have been done by many papers as [10,16–19], this work only provides simulated results, which are reasonable proofs to foresee that this work has better reliability performance with steady state and transient considerations.

6. Conclusion

A new 2xVDD-tolerant I/O buffer against gate-oxide overstress and hot-carrier degradation has been successfully verified in a 0.13-μm 1.2-V CMOS process with only thin-oxide devices. The gate-to-source, gate-to-drain, and drain-to-source voltages of the transistors in the new proposed 2xVDD-tolerant I/O buffer can be kept within the normal operating voltage (VDD) with simulated verification. The new proposed 2xVDD-tolerant I/O buffer can receive 1.2-V/2.5-V input signals or transmit 1.2-V output signals up to 133 MHz, which is compatible to the I/O specifications of PCI-X in the mixed-voltage I/O interfaces.

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