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Radio Frequency Power Performance Enhancement for Asymmetric Lightly Doped Drain Metal–Oxide–Semiconductor Field-Effect Transistors on SiC Substrate

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In this paper we report the DC characteristics and radio frequency (RF) power performance improvement as high as 6.6% of asymmetric lightly doped drain metal–oxide–semiconductor field-effect transistors (asymmetric LDD MOSFET, AMOSFET) with 50-µm-thick silicon substrates on SiC substrates. The self-heating and parasitic effects of large size AMOSFETs with 50-µm-thick silicon on SiC substrates are reduced owing to good heat dissipation and less lossy behaviors of thinned silicon substrates and SiC substrates. Therefore, the power gain, saturation output power, and power added efficiency of AMOSFETs with 50-µm-thick Si substrates mounted on SiC substrates is improved.
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1. Introduction

The Si radio frequency (RF) metal–oxide–semiconductor field-effect transistors (MOSFETs) are now widely used for wireless communications, owing to improvements larger RF gain, higher current-gain ($|H_{21}|^2$) cut-off frequency (f_t) and better power-gain (G_{max}) maximum oscillation frequency (f_{max}) with transistor down-scaling and technology evolution.[1–4] We previously developed an asymmetric-lightly doped drain (LDD) MOSFET (AMOSFET)[5] that met the requirement large RF output power and high-frequency performance. This new RF power device (AMOSFET) can be fabricated in standard foundry logic processes by blocking the n-drain extension using a LDD mask without extra processing steps.

Advanced complementary metal–oxide–semiconductor (CMOS) technology is one of the candidates for system-on-chip (SOC) due to integration and low cost. However, the decay factors of MOSFET performance are the self heating effect[6] and substrate loss.[7] The self heating effect is the heating of a device owing to its internal power dissipation, especially in high-current devices. It results in a reduction of the drain current and the negative output conductance effect. Additionally, a lossy Si-substrate causes the parasitic effect of the coupling capacitance and a loss of the RF signal to the substrate. In this study, we report that the DC characteristics and RF performance can be improved by about 6% for an AMOSFET with an ultrathin Si substrate (50 µm) bonded to a SiC substrate. The thermal conductivity is of the SiC substrate is 4.9 W cm^{-1} K^{-1} compared with 1.5 W cm^{-1} K^{-1} for the silicon substrate. The resistivity of very large-scale integrated circuit (VLSI)-standard Si substrates is 10 Ω cm lower than that of the semi-insulating SiC substrates is ∼10^5 Ω cm. The substrate is removed using chemical mechanical polishing (CMP) process after the CMOS IC processes. Active devices after thinning and transfer onto plastic have also been reported.[8–10] However, the self-heating effect in a high-current active device is serious because of the effect it has in terms of worsening the thermal conductivity. Therefore, the device with a SiC substrate base is a good candidate to improve DC characteristics and RF power performance.

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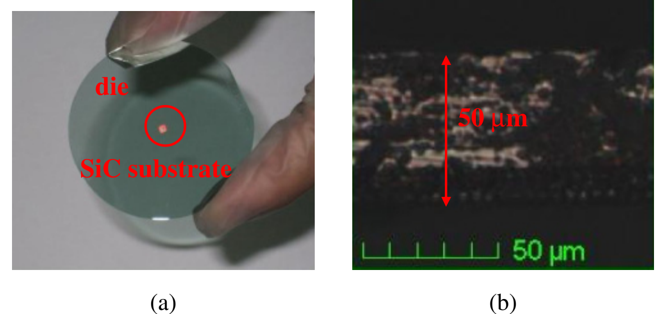

(a) (b)

Fig. 1. (Color online) (a) Image of a 50 µm thick die on a SiC substrate. (b) Substrate thickness measurement after the thinning procedure.

2. Experimental Methods

A foundry standard, 0.18 µm, 1-poly–6-metal (1P6M) logic process was used in this study. To increase the breakdown voltage, the drain LDD region was removed by an n ion-implantation blocking mask to form the AMOSFET.[5] The p-type region underneath the drain spacer forms a wider depletion region to allow larger applied drain voltage. A multiple gate finger layout was used, which has a 40-gate-finger AMOSFET with 0.18 µm gate length and 5 µm width for milli watt RF power application. To achieve integration onto a SiC substrate, we first thinned the Si substrate from 550 to 50 µm using a CMP procedure. The thinned die was then transferred onto a 275-µm-thick SiC substrate. Figure 1(a) shows an image of the fabricated die on the SiC substrate (background held by hand). The thickness of the 50-µm-thick Si substrate thinned-down based on the optical measurement is shown in Fig. 1(b). The semi-insulating SiC substrate had a resistivity of 10^5 Ω cm. The devices were fabricated on 8-in wafers at an IC foundry. The small signal S-parameters were measured up to 22 GHz CASCADE probe station and LRRM standard calibration procedure using an HP8510C network analyzer. The intrinsic device characteristics were obtained by open and short two-step de-embedding procedures.[11,12] The RF power characterization was carried out by on-wafer measurements at 2.4 GHz using an ATN load-pull system, where the input and output impedance matching conditions were selected to optimize the output power.

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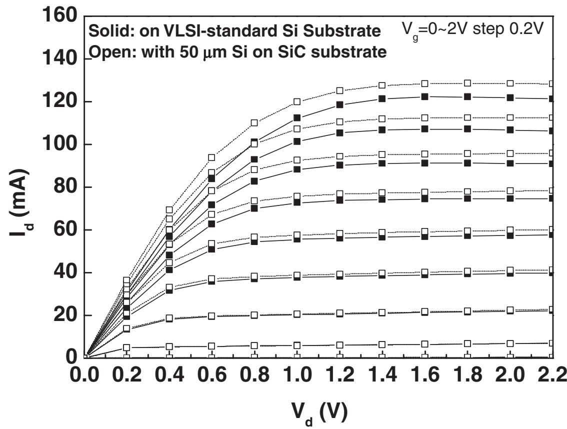

Fig. 2. Drive current of 0.18 μm AMOSFETs on VLSI-standard Si substrates and 50 μm Si substrates on SiC.

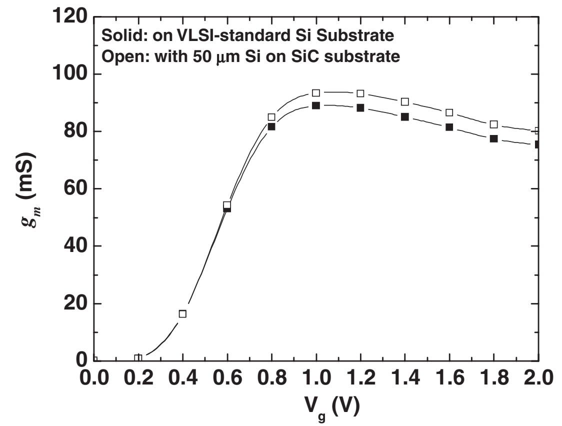

Fig. 4. DC transconductance g_m of 0.18 μm AMOSFETs on VLSI-standard Si substrates and 50 μm Si substrates on SiC.

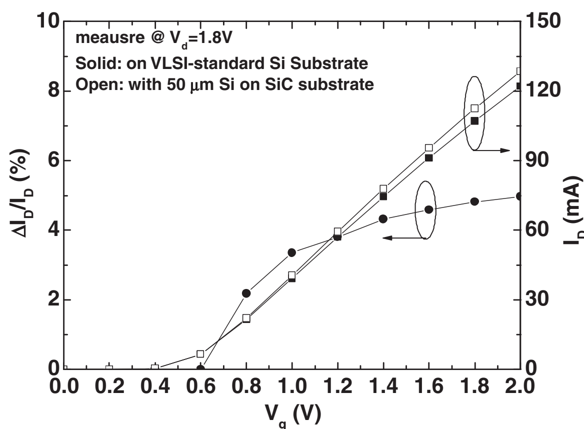

Fig. 3. Increasing rate of the drain current for 0.18 μm AMOSFETs on VLSI-standard Si substrates and 50 μm Si substrates on SiC at $V_d = 1.8$ V.

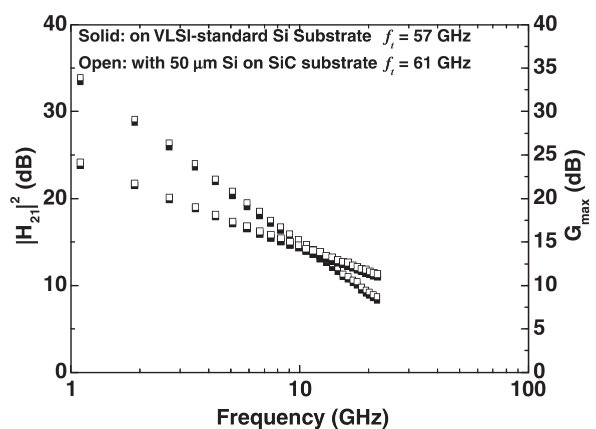

Fig. 5. Measured $|H_{21}|^2$ and G_{max} characteristics of 0.18 μm AMOSFETs on VLSI-standard Si substrates and 50 μm Si substrates on SiC.

3. Results and Discussion

3.1 DC characteristics

The drive current of AMOSFETs of 200 μm width and 0.18 μm length before and after a thinning-down process are shown Fig. 2. After the thinning and transfer procedures, the drain current increases at high V_g (> 0.6 V). However, the drain currents of these two devices are almost the same at small V_g (< 0.6 V). Because the SiC has good heat dissipation to reduce the self-heating effect. The self-heating effect could be verified from the pulse I–V measurement[13] owing to the "cold" device characteristics. Figure 3 shows the increasing percentage of the drain current at the $V_d =$ 1.8 V bias condition. The reduction of self-heating effect is significant at higher drain current I_d.

Figure 4 shows the transconductance enhancement of AMOSFET before and after thinning. The thinned AMOSFET on a SiC substrate shows a higher g_m characteristic than that on a VLSI-standard substrate. The g_m value increased from 88.95 to 93.4 mS, which is a 5% enhancement. The enhancement trend in DC performance is due to the good heat dissipation of 50 μm Si on a SiC substrate.

3.2 *S*-parameters

The RF *S*-parameters from 1.1 to 22 GHz of AMOSFETs before and after thinning were measured. Figure 5 shows the current gain ($|H_{21}|^2$) and G_{max} as a function of frequency for both AMOSFETs. A cutoff frequency f_t of 61 GHz was obtained from the measured *S*-parameters for the thinned AMOSFET device. This value is higher than the 57 GHz value found for the VLSI-standard Si substrate AMOSFET. This higher f_t in the thinning AMOSFET device is consistent with the g_m in Fig. 4. The f_t is given by

$$\omega_T = \frac{g_m}{C_g},$$

where C_g is input capacitance and $\omega_T = 2\pi f_T$. Therefore, the thinned-down AMOSFET has the higher f_t due to the higher g_m. The reduced self-heating effect improves the RF small signal characteristic.

The G_{max} that has a -10 dB/decade slope in the maximum stable gain (MSG) frequency region was obtained from the measured *S*-parameters on VLSI-standard Si substrates and 50 μm Si substrates on SiC AMOSFET device. The thinned-down AMOSFET maintained a higher G_{max} than the VLSI-standard Si substrate AMOSFET device as shown in Fig. 5. Therefore the higher f_{max} is obtained by extrapolation for the thinned-down AMOSFET device. However, this method cannot be used to determine the f_{max}. This is because the G_{max} slope changes from -10 dB/decade

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Table I. Comparison of RF g_m and R_{sub} for 0.18 µm AMOSFETs on VLSI-standard Si substrate and 50 µm Si substrate on SiC.

AMOSFET	VLSI-standard Si substrate	50 µm Si Substrate on SiC substrate	Improvement (%)
g_m (RF) (S)	0.097	0.103	6
R_{sub} (Ω)	54	64	18.5

to higher values at higher frequencies, where the G_{max} decreases from the MSG to the maximum available gain (MAG). The f_{max} value is above our measurement capability.

For further analysis of the substrate materials, it is necessary to extract the small-signal device parameters RF g_m and R_{sub}. The device parameters are de-embedded from the open pad. The RF g_m vaule is derived from[14)]

$$g_m = |Y_{21} - Y_{12}|.$$

The bias of an AMOSFET whose body is tied to the source is $V_g = 1.2$ V, $V_d = 1.8$ V. The extracted RF g_m value in Table I shows the 6% improvement, which is the same trend observed for DC characteristics. A simple extraction method of extracting R_{sub} from the Y-parameters of the MOSFET is proposed. The R_{sub} is derived from[15)]

$$R_{sub} \approx \frac{\mathrm{Re}[Y_{22}]}{(\mathrm{Im}[Y_{22}] + \mathrm{Im}[Y_{12}])^2}.$$

The bias of an AMOSFET whose body is tied to the source is $V_g = V_d = 0$ V. The 18.5% enhancement in the extracted R_{sub} is obtained from the thinned-down device to the VLSI-standard device in Table I. The higher R_{sub} shows lower substrate loss. Therefore, the thinned-down AMOSFET on a SiC substrate shows better RF performance due to lower substrate loss and better DC characteristics.

3.3 RF power characteristics

The substrate loss can be reduced by a CMP procedure after the IC processes. In this study the substrate was thinned-down to 50 µm. The substrate loss can be reduced to improve the RF power performance. The RF power characteristics have been measured at 2.4 GHz by ATN load pull system under the DC bias point, $V_{gs} = 1.2$ V and $V_{ds} = 2.5$ V, for the AMOSFETs before and after thinned-down procedure in Fig. 6. The DC drain breakdown voltage (BV_{dss}) of the AMOSFETs was 6.9 V for asymmetric-LDD transistors.[5)] This better BV_{dss} is due to the wider depletion region designed at drain side to allow higher applied voltages, which is vital for RF power applications with large voltage swing. Therefore, the AMOSFET devices are biased at $V_{ds} = 2.5$ V with a 2× drain voltage swing in this study. The RF saturation output power (P_{sat}) at 2.4 GHz is 0.45 and 0.48 W/mm for the AMOSFET devices on VLSI-standard Si substrate and 50 µm Si substrate on SiC, respectively. This is equivalent to a 6.6% enhancement. The higher improvement percentage is benefit from the reduced substrate loss by thinned down substrate to 50 µm and transfer to the semi-insulating SiC substrate. The power gain is also increased from 19.88 to 20.12 dB, which is nearly a 0.3 dB improvement. In an RF power amplifier, power-added efficiency (PAE) is defined as the ratio of the difference between the

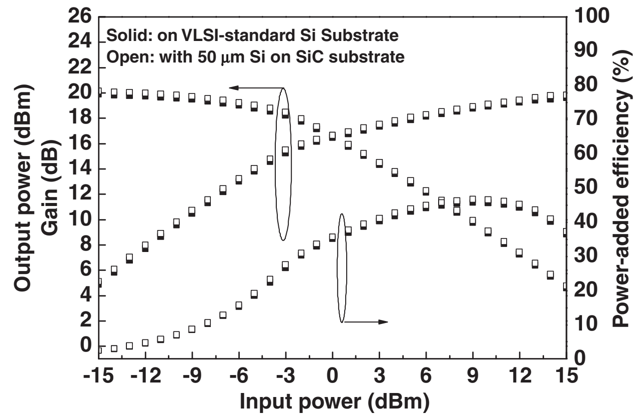

Fig. 6. Measured RF output power, gain and PAE of 0.18 µm AMOSFETs on VLSI-standard Si substrate and 50 µm Si substrate on SiC at 2.4 GHz.

output and input signal power to the DC power consumed, as given by

$$\mathrm{PAE} = \frac{\mathrm{RF_{out}} - \mathrm{RF_{in}}}{P_{DC}}.$$

The peak PAE of AMOSFET devices on VLSI-standard Si substrates and 50 µm Si substrates on SiC are 45.6 and 46.6%, respectively. The enhancement of the trend in the measured large signal RF P_{out} and PAE characteristics as a function of P_{in} is in good agreement with the improvement in DC measurement results. The improvement in DC I–V and RF characteristics is due to the reduction in the self-heating and substrate loss effect.

4. Conclusions

We have successfully demonstrated the improved DC characteristics and RF performance of AMOSFETs on 50 µm Si substrates mounted on SiC substrates. These are future candidates for heat sink applications in high-power devices. The trend in the enhancement is also observed in the milli watt power range. The combination of a thinned Si substrate on a SiC substrate also shows better RF performance owing to the reduction of self-heating and the substrate loss effect.

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