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Improved Radio Frequency Power Characteristics of Complementary Metal–Oxide–Semiconductor-Compatible Asymmetric-Lightly-Doped-Drain Metal–Oxide–Semiconductor Transistor

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We have characterized and modeled the radio frequency (RF) power performance of a 0.18 μm asymmetric-lightly-doped-drain metal–oxide–semiconductor field-effect transistor (LDD MOSFET). In comparison with the conventional 0.18 μm MOSFET, this asymmetric-LDD device shows a larger power density of 0.54 W/mm, and 8 dB better adjacent channel power ratio (ACPR) linearity at 2.4 GHz from the improved twice DC breakdown voltage of 6.9 V. These significant improvements of RF power performance in the asymmetric-LDD transistor are important for the medium RF power amplifier application. © 2010 The Japan Society of Applied Physics

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1. Introduction

Silicon radio frequency (RF) metal–oxide–semiconductor field-effect transistors (MOSFETs) are now widely-used for wireless communications owing to the improvements of larger RF gain, higher current-gain ($|H_{21}|^2$) cut-off frequency (f_T), and power-gain (G_{max}) maximum oscillation frequency of (f_{max}) with transistor down-scaling and technology evolution.[1–9] This has led MOSFETs to be the prime choice for wireless communication and RF system-on-chip (SoC) application such as WiMAX, W-LAN, and ultrawide band (UWB). However, one fundamental challenge for MOS transistors is the relatively poor RF power performance, which is due to the lower drain breakdown voltage for RF power delivery. The breakdown voltage becomes even worse with down-scaling of MOSFETs, even though the higher f_T and f_{max} allow a higher frequency operation with higher gain. Nevertheless, the MOSFET is still desirable for RF power applications because of the low cost and high-density circuit integration. To improve the breakdown voltage, lateral-diffused MOS (LDMOS) transistors[10–14] have been proposed. However, the issues are the lower f_T and f_{max} difficult for higher RF frequency application and the non-standard process with extra process steps and masks beyond IC foundry. To address above issues, we proposed a new asymmetric lightly-doped-drain (LDD) MOS transistor.[15] Using the 0.25 μm technology, this device showed high drain breakdown voltage and preserved a high f_T and f_{max} for high frequency operation at the same time. The realization of both the high power density and low ACRP is difficult when scaling the gate length (L_g). A long L_g and long drain side region have been used to improve breakdown voltage (V_{BD}).[16] However, the long gate length degrades gain and the long drain side region increases parasitic resistance and impacts the output power (P_{out}). In this paper, we further studied the scalability of this asymmetric-LDD MOSFET[17] to 0.18 μm which increases V_{BD} and power density as well as improving the linearity of ACPR due to a higher bias point. In this paper, we further studied the scalability of this asymmetric-LDD MOSFET[17] to 0.18 μm. A device model of DC, RF small signal and large signal RF power was developed to design the RF power amplifier. In comparison with a conventional 0.18 μm device, the asymmetric-LDD MOSFET had twice the DC breakdown voltage to 6.9 V, a higher output power of 64%, and 8 dB better linearity of adjacent channel power ratio (ACPR) at 2.4 GHz. The good accuracy of the device model is evident from the good agreement of simulated data with measured RF output power characteristics of a power amplifier circuit.

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2. Experimental Methods

A foundry standard 0.18 μm 1-poly-6-metals (1P6M) logic process was used in this study. To increase the breakdown voltage of an asymmetric-LDD MOSFET, the drain LDD region was removed by an n^+ ion-implantation blocking mask.[15] Conventional MOSFETs were also fabricated for comparison. The p-type region underneath the drain spacer forms a wider depletion region to allow a larger applied drain voltage. A multiple gate finger layout has been used, which has 10-gate-fingers in these MOS transistors with 0.18 μm gate length and 5 μm width. A standard coplanar-waveguide (CPW) RF layout was used for on-wafer probing.[5–9] The small signal *S*-parameters are measured from 45 MHz to 20 GHz by CASCADE probe station and SOLT standard calibration procedure using an HP8510C network analyzer. The intrinsic device characteristics were obtained by a de-embedding procedure.[5–9] The RF power characterization was carried out by on-wafer measurements at 2.4 GHz using an ATN load-pull system, where the input and output impedance matching conditions were selected to optimize the output power.

3. Results and Discussion

3.1 DC characteristics

Figure 1 shows a comparison of DC drain breakdown voltage at a gate voltage (V_g) of 0 V (BV_{dss}) for conventional and asymmetric-LDD MOS transistors. A BV_{dss} of 3.5 V is measured for a conventional MOSFET at an I_{ds} of 0.1 μA/μm, which is increased to 6.9 V for the asymmetric-LDD transistor under the same criteria. The increased BV_{dss} is due to the wider depletion region at the drain side designed to permit higher applied voltage. The larger DC breakdown voltage is important for RF power applications with a large voltage swing.

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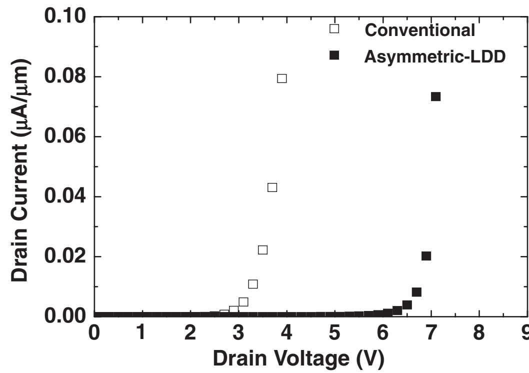
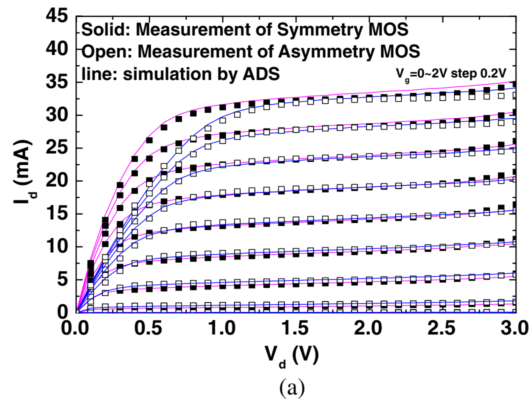
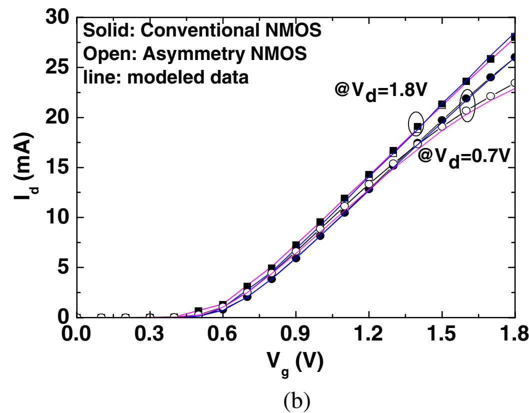


Fig. 1. I_d–V_d characteristics at a V_g of 0 V for conventional and asymmetric-LDD n-MOSFETs with the same gate length of 0.18 μm.



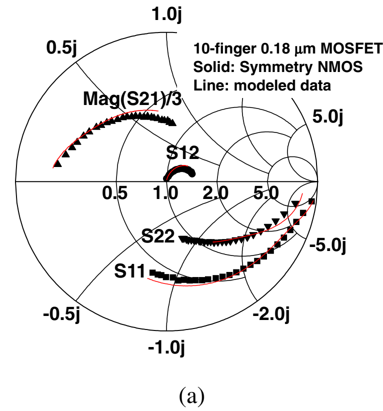
(a)



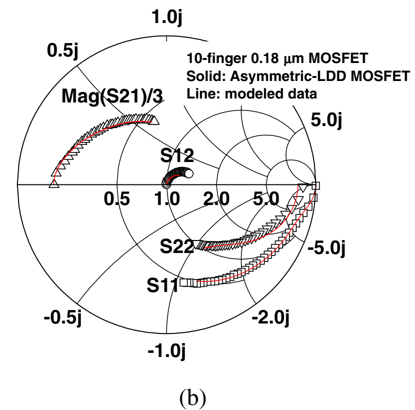
(b)

Fig. 2. (Color online) Measured and simulated (a) I_d–V_d and (b) I_d–V_g characteristics for 10-gate-finger conventional and asymmetric-LDD 0.18 μm RF MOSFETs.

In addition to the high breakdown voltage, the high drain current is also important for RF power applications. The drive current of conventional and asymmetric-LDD 0.18 μm MOSFETs are shown in the DC drain current–drain voltage (I_d–V_d) and drain current–gate voltage (I_d–V_g) characteristics of Figs. 2(a) and 2(b), respectively for comparison. The discrepancy between these two 0.18 μm devices is the slightly degraded knee voltage and turn on resistance (R_{on}) at low V_d. However, the saturation drain current ($I_{d,sat}$) of these two devices is almost the same at high V_d. The close $I_{d,sat}$ values are due to the injected electrons from the source that are transient over the wide drain depletion region at fast saturation velocity. The nearly identical I_d–V_g curves at high V_d led to close transconductance (g_m) values which are important for the



(a)



(b)

Fig. 3. (Color online) Measured (solid symbols) and simulated (line) *S*-parameters for (a) conventional and (b) asymmetric-LDD 0.18 μm RF MOSFETs from 45 MHz to 20 GHz.

small signal RF gain of $|H_{21}|^2$ and G_{max}, f_T [$g_m/2\pi(C_{gd+}C_{gs})$] and f_{max} discussed in the following sections.

The RF *S*-parameters are shown in Figs. 3(a) and 3(b) for conventional and asymmetric-LDD 0.18 μm MOSFETs, respectively. The forward S_{21} is divided by 3 to fit into the Smith charts. One significant difference between these two devices is the smaller reverse S_{12} in asymmetric-LDD MOSFET, which is due to the smaller gate–drain coupling capacitance with a wide depletion region at the drain without an n^+ drain extension region.

To further analyze the small signal RF characteristics, we have plotted the frequency dependence on $|H_{21}|^2$ and G_{max}, as shown in Figs. 4(a) and 4(b), for conventional and asymmetric-LDD 0.18 μm MOSFETs, respectively. The $|H_{21}|^2$ follows the typical −20 dB/decade slope with increasing frequency and G_{max} follows a −10 dB/decade slope in the maximum stale gain (MSG) frequency region. The f_T was obtained by extrapolating the $|H_{21}|^2$ to 0 dB by the same slope of −20 dB/decade. The asymmetric device maintained a high f_T of 52 GHz, which is close to the 55 GHz value obtained for the conventional device. This is due to nearly the same g_m obtained in the I_d–V_g characteristics shown in Fig. 2(b) at large V_d bias. However, this method cannot be used to determine the f_{max}. This is because the G_{max} slope changes from −10 dB/decade to a higher value at higher frequencies, where the G_{max} decreases from the MSG to maximum available gain (MAG). A device model is required to analyze the MAG and f_{max} at higher frequency, beyond the maximum frequency provided by the network analyzer. Such a device model, with simulation

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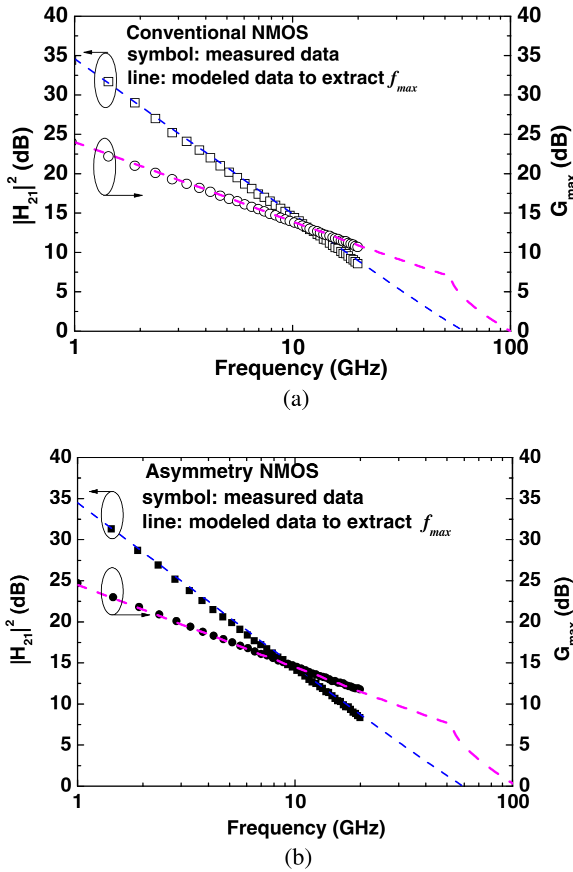

Fig. 4. (Color online) Measured and simulated $|H_{21}|^2$, G_{max}, f_T, and f_{max} characteristics for (a) conventional and (b) asymmetric-LDD 0.18 μm RF MOSFETs. The f_T was obtained by extrapolating $|H_{21}|^2$ in the MAG region.

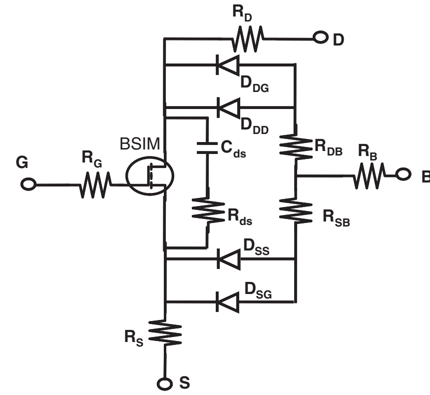

Fig. 5. Self-consistent device model of asymmetric-LDD 0.18 μm RF MOSFETs used to simulate the DC, small signal S-parameters and large signal RF power characteristics.

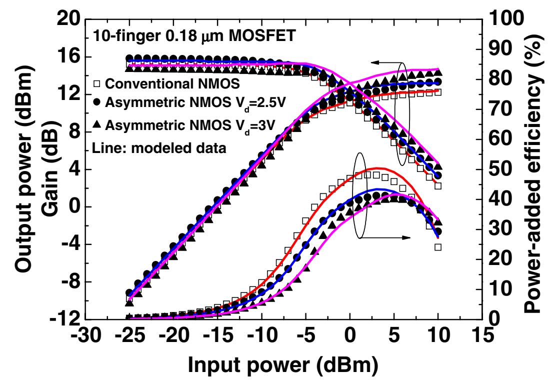

Fig. 6. (Color online) Measured and simulated RF output power and PAE of conventional and asymmetric-LDD 0.18 μm RF MOSFETs at 2.4 GHz.

data in good agreement with measured DC, small signal *S*-parameters, and large signal RF characteristics, is also indispensable for power amplifier circuit design.

3.2 Device modeling of asymmetric-LDD MOSFET

Figure 5 shows the device model for the asymmetric-LDD MOSFET. A Berkeley short-channel IGFET model (BSIM3) core is used to simulate the DC to RF characteristics, and additional subcircuits were added for parasitic effects.[8,9,18] This asymmetric-LDD device model has a smaller C_{gd} and larger drain series resistance (R_D) to simulate the slightly larger R_{on} and smaller S_{12}, owing to the wide depletion region without n^+ doping at the drain side. The typical value of R_D is 11.33 Ω with a smaller gate–drain feedback capacitance (C_{gd}) of 1.9×10^{-10} F/m. The good accuracy of this equivalent circuit model has been verified by the close agreements of simulated and modeled DC, *S*-parameters, and RF gains ($|H_{21}|^2$ and MSG) shown in Figs. 2–4, respectively.

On the basis of this well-calibrated model shown in Fig. 4, we have further simulated the G_{max} at higher frequencies, where the G_{max} degradation slope changes to ~25 to 40 dB/decade in the MAG region. Note that an f_{max} of 115 GHz was obtained in asymmetric-LDD device, which is higher than the 97 GHz value obtained in the conventional device by extrapolation. This is due to the smaller reverse S_{12} shown in Fig. 3(b), which originated from the lack of n^+ drain LDD extension underneath the drain spacer to give a lower C_{gd}. Therefore, no degradation was found in small signal RF performance of the asymmetric-LDD 0.18 μm MOSFET compared with its conventional counterpart.

Note that the transit frequency f_T [$= g_m/2\pi(C_{gd}+C_{gs})$] and the maximum oscillation frequency f_{max} are useful figures of merit to evaluate the dynamic performances of a device dedicated to RF PA applications. The f_{max} of the MOS transistor can be estimated using[10)]

$$f_{max} = \sqrt{\frac{f_T}{8\pi \cdot R_g \cdot C_{gd}}}. \qquad (1)$$

The smaller C_{gd} increases f_T and f_{max}. The g_m of asymmetric-LDD device and the conventional device are almost the same in the saturation region. Therefore, the asymmetric device shows a high f_T and f_{max} which are almost the same as those of the conventional type.

3.3 RF power performance

We further measured the RF power characteristics. Figure 6 shows the output power and power-added efficiency (PAE) for conventional and asymmetric-LDD 0.18 μm devices measured at 2.4 GHz. The DC bias for these devices during measurements are at peak g_m for V_g. The V_d bias for conventional devices was at 1.8 V allowing a two times drain voltage swing close to BV_{dss} that is higher at 2.5 and 3 V for the asymmetric-LDD MOSFET because of the higher BV_{dss}. Good match between harmonic balance simulation and

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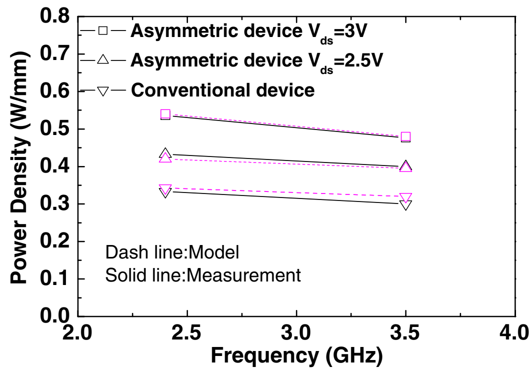

Fig. 7. (Color online) Measured and simulated power density as functions of operation frequency and V_d bias for conventional and asymmetric-LDD 0.18 μm RF devices.

measured data are also shown in Fig. 6. The RF output power at 2.4 GHz increased from 0.33 W/mm in conventional MOSFET to 0.43 and 0.54 W/mm in the asymmetric-LDD device, which is equivalent to 30 and 64% improvements. The peak PAE's for the asymmetric-LDD 0.18 μm device are 42 and 40% at V_d biases of 2.5 and 3 V, respectively, which are slightly lower than the 48% value for the conventional device. However, the peak PAE for the asymmetric-LDD device exists at a higher RF power output than that of conventional ones with as much as 3 dB better output power.

Figure 7 further depicts the measured output power as functions of V_d bias and frequency. The output power decreases with increasing frequency from 2.4 to 3.5 GHz, which is due to the decreased gain at higher frequency. However, significantly larger RF output power is still obtained in the asymmetric-LDD 0.18 μm devices than in conventional ones, which is simply due to the larger applied V_d bias permitting larger RF voltage swing. The higher RF power density of the asymmetric-LDD MOSFET is especially important for Si-based power amplifier design using power-combining techniques.[19] The higher power density in the unit cell allows shorter transmission lines for RF power combination, where the RF loss to the substrate for transmission line is one of the key issues for Si-based RF ICs.[20–22]

The load-pull measurement offers no information of the actual voltage and current waveforms in terms of time domain. We have performed the harmonic balance simulation on our well-calibrated large signal nonlinear model shown in Figs. 6 and 7. Figures 8(a), 8(b), and 8(c) show the voltage and current swings as a function of time for 0.18 μm conventional and asymmetric-LDD MOSFETs biased at V_d's of 1.8, 2.5, and 3 V, respectively, with the same 10 dBm input power at 2.4 GHz.

The peak-to-peak drain output voltage and current swings increase monotonically with increasing V_d bias from 3.8 V and 35.3 mA for $V_d = 1.8$ V, 4.9 V and 37.2 mA for $V_d = 2.5$ V, and 6.2 V and 43.2 mA for $V_d = 3$ V. Therefore, the improved RF power performance in asymmetric-LDD MOSFETs is due to both the larger voltage and current swings, which is in good agreement with the load-pull measurements shown in Fig. 6.

3.4 Linearity in saturation

One of the key factors for a power amplifier is to have a good linearity. We have measured the ACPR of both conventional and asymmetric-LDD MOSFETs to examine the linearity characteristics. The ACPR measurement was standard W-CDMA with QPSK modulation from a ROHDE & SCHWARZ SMIQ06B signal generator. The calibration was carried at using an ATN on-wafer load pull system. As shown in Fig. 9, the ACPR degrades with increasing output power, which is typical for RF power transistors. However, the asymmetric-LDD device shows improved ACPR with increasing V_d bias; the improvement is as high as 8 dB at peak PAE compared with conventional devices. This is due to the decreased reverse feedback coupling between gate and drain nodes from smaller C_g that decreases the interference from adjacent channels. The much-improved ACPR in the asymmetric-LDD device is essential for linear power amplifiers.

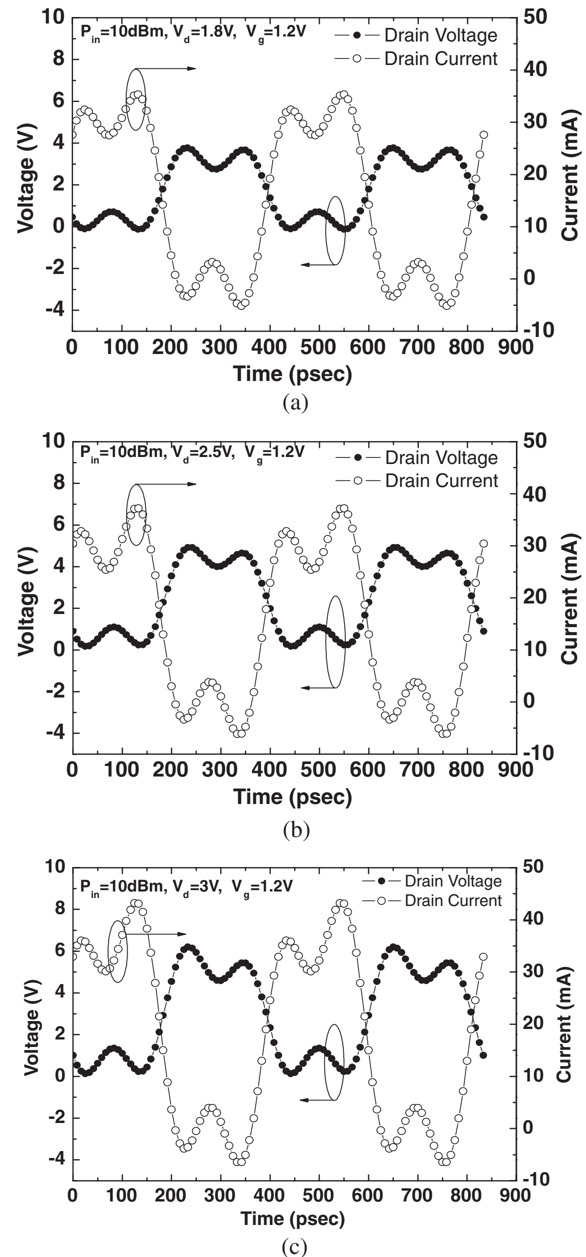

Fig. 8. Input and output voltage and current swing of the devices at the 10 dBm RF input power for (a) conventional ($Z_S = 195 + j168.8$, $Z_L = 95.1 + j20.9$), (b) asymmetrical-LDD at $V_d = 2.5$ V ($Z_S = 195 + j168.8$, $Z_L = 121.2 + j29.8$) and (c) at $V_d = 3.0$ V ($Z_S = 195 + j168.8$, $Z_L = 120.5 + j40$) 0.18 μm RF MOSFETs.

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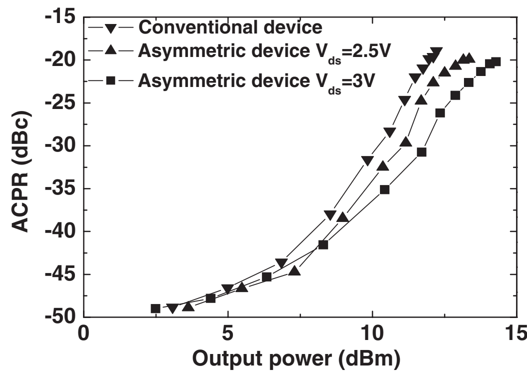

Fig. 9. ACPR vs output power of conventional and asymmetric-LDD 0.18 μm RF MOSFETs at 2.4 GHz.

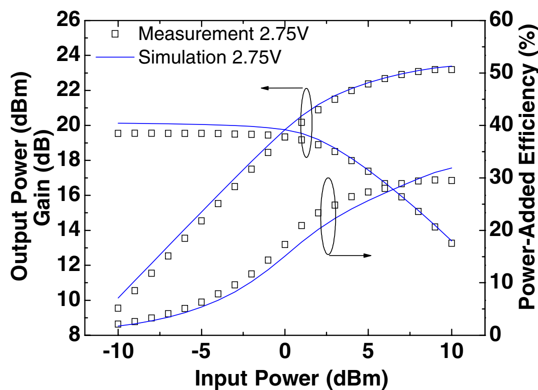

Fig. 10. (Color online) Measured and simulated RF output power, gain and PAE of designed PA using high breakdown voltage asymmetric-LDD MOSFETs.

3.5 Two-stage PA chip

On the basis of the well-matched device model, we have designed a two-stage power amplifier. The two-stage power amplifier adopts a class A operation for the driver stage and a class AB operation for the power stage. The circuit is designed with on-chip matching to decrease the complexity of wire bonding. The impedances of input, inter-stage, and output matching are designed to achieve a compromise between power and efficiency from load and source pull simulation.

The fabricated power amplifier using high breakdown voltage asymmetric-LDD MOSFETs showed an excellent ACPR of −36 dBc at 18 dBm and a large 23.3 dBm output power, 19.6 dB power gain, and good 29.6% at 2.4 GHz (Fig. 10). This result is competitive for off-chip power amplifiers with a specially designed linearizer.[23] The good matching of measured and simulated output–input power characteristics also confirms the good accuracy of our large signal nonlinear device model.

4. Conclusions

We have designed an asymmetric-LDD MOS transistor to increase the BV_{dss} from 3.5 V to 6.9 for larger output voltage and current swing and higher RF power delivery. In addition, good ACPR and PAE are obtained. This asymmetric-LDD MOSFET is fully embedded in the standard CMOS logic process provided by foundries without any process modification.

Acknowledgments

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