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DC and RF Performance Improvement of 70 nm Quantum Well Field Effect Transistor by Narrowing Source–Drain Spacing Technology

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Received September 30, 2009; accepted October 27, 2009; published online January 6, 2010

A 70 nm InAs channel quantum well field effect transistor (QWFET) fabricated by a narrowing source–drain (S/D) spacing technique was realized for future high-speed and logic applications. The S/D spacing was decreased from 3 to 0.65 μm through a simple fabrication process, which is an ameliorative redeposition ohmic technique. The drain-source current density and transconductance of the device were increased from 391 to 517 mA/mm and from 946 to 1348 mS/mm after the scaling of the S/D spacing, respectively. In addition, the current gain cutoff frequency (f_T) was also increased from 185 to 205 GHz. These results show that the easy method can effectively improve the III–V QWFET device performance for high-frequency and high-speed applications. © 2010 The Japan Society of Applied Physics

DOI: 10.1143/JJAP.49.010212

For advanced wireless communications, InP-based quantum well field effect transistors (QWFETs) have attracted considerable attention in sub-millimeter-wave semiconductor technologies and demonstrated an excellent high-frequency performance because of their superior electronic transport properties and high saturation velocity.[1)] Moreover, it is also a potential candidate FET for next-generation low-power digital logic applications to extend Moore's law beyond the 22-nm-node era.[2,3)] Generally, reductions in gate length and device pitch are the key driving force behind future millimeter wave or digital applications. Additionally, the associated parasitic resistances are no longer negligible and become a decisive factor in the performance enhancement of such ultrahigh-speed QWFETs. However, the state-of-the-art QWFETs typically have a source–drain ohmic contact separation on the order of 1.5 to 3 μm.[4)]

This problem may be solved through the adjustment of the self-aligned gate (SAG) process to attain low parasitic elements by reducing the physical separation between the metallized ohmic contacts and the intrinsic gate region.[5)] The source resistance (R_S) is the most critical component for achieving a high transconductance and a high RF performance. Previous effort in the SAG process was complex, and ion implantation for source–drain (S/D) doping[6,7)] was often adopted, which is not suitable for the fabrication of III–V FETs since active ions may damage the wafer structure. Furthermore, the activation annealing after ion implantation is always performed at high temperatures (such as 800–1000 °C), which are close to the growth temperature of the III–V epitaxial structure.[8)] It may result in grain regrowth or form numerous hot carriers that make the devices easier to break down.

In this study, 70 nm InAs channel QWFETs were fabricated by a modified self-aligned gate technology. This technology was developed simply with ohmic metal redeposition, which effectively reduced the source/drain spacing from 3 to 0.65 μm, and was also considered suitable for mass production. The measurement results in this work clearly evidenced that superior device performance can be easily achieved through a few added simple fabrication processes.

The InAs QWFET structure was grown by molecular beam epitaxy (MBE) on a 2-in.-diameter InP substrate. The epitaxial layer structure is as follows. It has a 50 Å InAs main channel layer with a 20 Å $In_{0.53}Ga_{0.47}As$ upper subchannel and a 30 Å $In_{0.53}Ga_{0.47}As$ lower subchannel grown on top of a 500-nm-thick InAlAs buffer layer. A 30-Å-thick InAlAs spacer with 4×10^{12} cm^{-2} Si-δ-doping, a 5-nm-thick InAlAs schottky barrier, a 4-nm-thick InP etch-stop layer, and a 40-nm-thick n-$In_{0.53}Ga_{0.47}As$ cap layer with 2×10^{19} cm^{-3} Si doping were grown on top of the composite channel layers.

For the device fabrication, the mesa was formed by wet chemical etching, and the ohmic contacts were formed with a 3 μm S/D spacing by evaporating Au/Ge/Ni/Au on the heavily doped cap layer. After the 70 nm T-shaped gate process, the 1500-Å-thick SiO_2 film was deposited as a hard mask at 200 °C by plasma-enhanced chemical vapor deposition to protect the 70 nm T-shaped gate, and then, the SiO_2 film between the source and drain region was removed by diluted HF (1 : 100). To reduce the effect of side etching, the etching time should be controlled accurately. Subsequently, a thin Au layer (around 500 Å) was redeposited by e-gun evaporation, covered from the source area to the drain area, forming a 0.65 μm S/D spacing as an ohmic metal after the lift-off technique. Finally, the devices were passivated with 600 Å SiN_x by PECVD at 200 °C. Figure 1(a) shows the schematic description of the QWFET process flow with the newly proposed method. The cross-sectional SEM images of the 70 nm T-shaped gate with a 0.65 μm S/D spacing are shown in Figs. 1(b) and 1(c), respectively. The specific contact resistance was measured to be 0.07 Ω·mm measured by a transmission line method (TLM).

The device with a 0.65 μm S/D spacing exhibited very good pinch-off characteristics, and a saturation current density (I_{DS}) of 517 mA/mm was achieved at $V_{DS} = 0.5$ V and $V_{GS} = 0$ V, as shown in Fig. 2, as compared with the drain current of 391 mA/mm for the device with a 3 μm S/D spacing. This drain current density increase was mainly due to the ameliorative ohmic technique that greatly reduced the access resistance. In addition, the highly doped cap layer structure with high doping promoted the formation of nonalloy ohmic contacts with a low specific contact resistance. In this study, the extracted source resistance R_S was 5 Ω for the device with a 3 μm S/D spacing compared with 1.1 Ω for the device with a 0.65 μm S/D spacing. As

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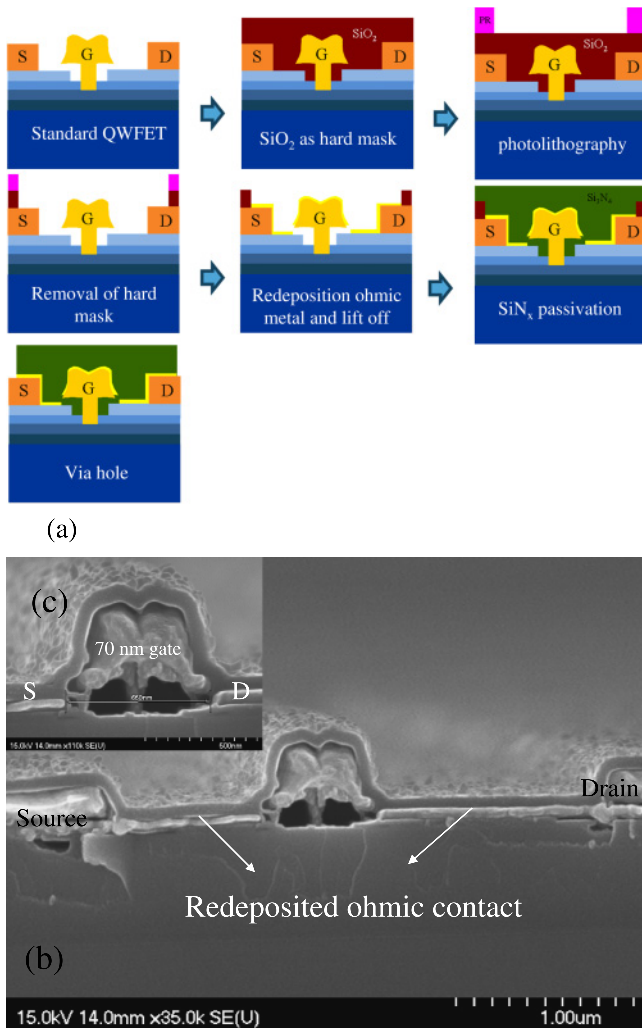

Fig. 1. (Color online) (a) Schematic of the QWFET process flow with newly proposed method. Cross-sectional SEM images of (b) redeposition ohmic metal and (c) 70 nm T-shaped gate with 0.65 μm S/D spacing.

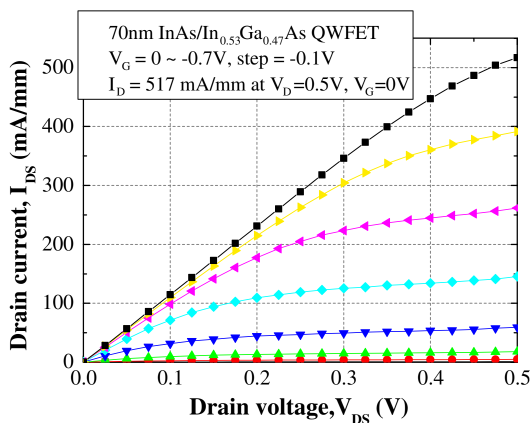

Fig. 2. (Color online) Drain-source current vs drain-source voltage curve of the 70 nm QWFET with 0.65 μm S/D spacing.

a result, it is concluded that the reduction in parasitic resistance by reducing the access resistance between the source (drain) and the gate is the main reason for the performance enhancement of the device.

The transconductance g_m and the drain source current plotted as functions of V_{GS} for controlled devices with a

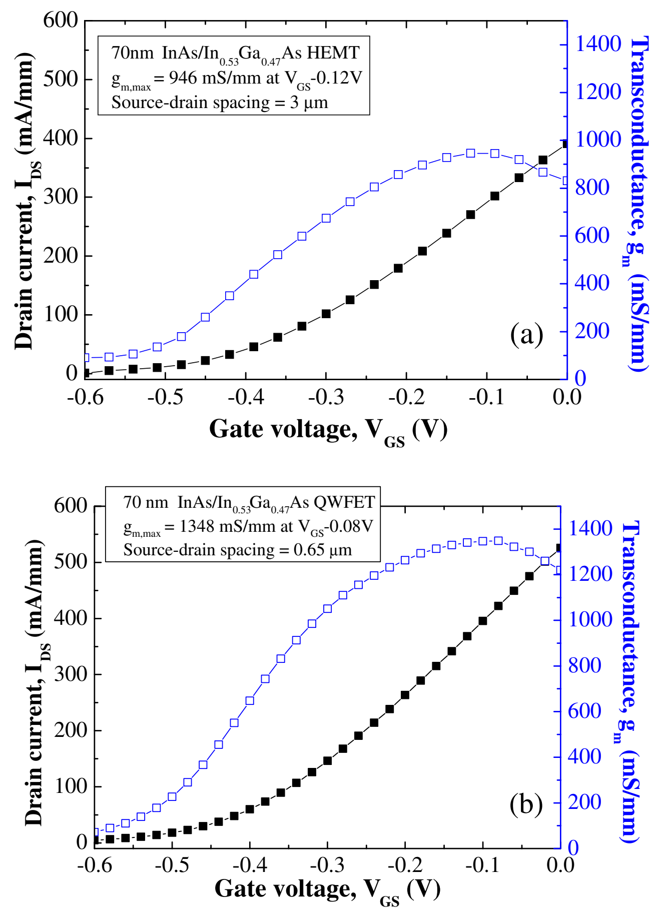

Fig. 3. (Color online) DC transconductance and drain-current characteristics of the (a) conventional QWFET with 3 μm S/D spacing and (b) device with newly proposed ohmic process with 0.65 μm S/D spacing.

redeposited ohmic process are shown in Figs. 3(a) and 3(b). The peak g_m value increased from 946 mS/mm for the controlled device to 1348 mS/mm for that with a 0.65 μm S/D spacing, both measured at $V_{DS} = 0.5$ V. This increase is mainly attributed to increase in I_{DS}. Moreover, the threshold voltage (V_{th}) slightly shifted from −0.58 V (without a redeposition ohmic metal) to −0.6 V (with a redeposition ohmic metal) when biased at $V_{DS} = 0.5$ V. The threshold voltage is defined as V_{GS} when I_{DS} reaches 1 mA/mm. It is probably due to the scaling of the gate–drain distance that increases the electric field between the gate and the drain, and modifies the threshold voltage.

As for the gate–drain breakdown voltage ($V_{DG,BR}$), the value decreased from 3.6 V for the standard device to 3.4 V for that with a redeposited ohmic process, mainly as a result of the increase in the electric field between the gate and the drain that reduces the device breakdown voltage. However, the diminution of the gate–drain breakdown voltage is still acceptable for low-voltage applications.

Figures 4(a) and 4(b) show the dependence of current gain and Mason's unilateral gain on frequency in 0.07 × 100 μm^2 QWFETs with 3 and 0.65 μm S/D spacings biased at a V_{DS} of 0.6 V, respectively. The parasitic capacitances due to the probing pads were carefully subtracted from the measured *S*-parameters of the QWFETs. A current gain cutoff frequency f_T of 205 GHz and a maximum oscillation frequency f_{max} of 170 GHz were obtained for the device with a 0.65 μm

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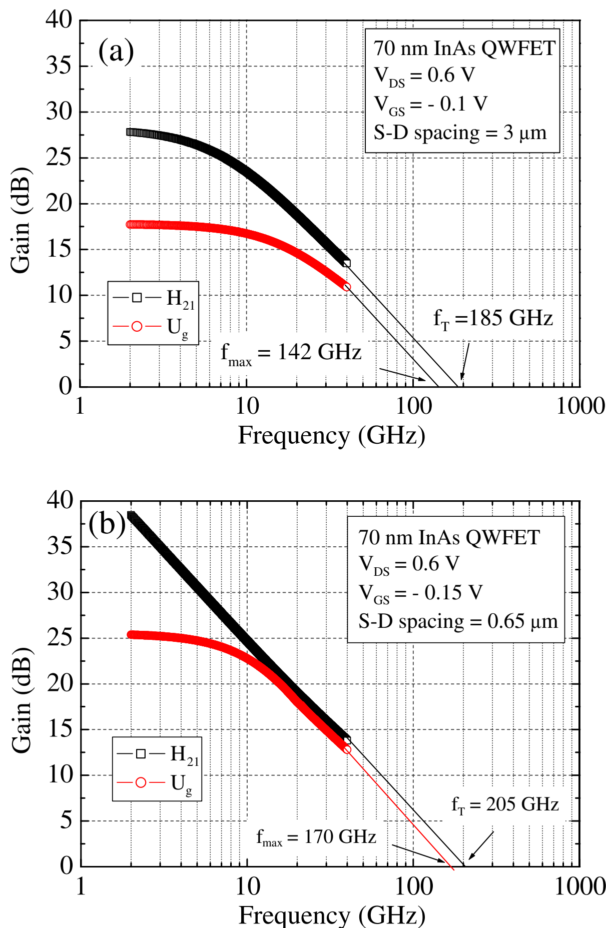

Fig. 4. (Color online) Frequency dependence of current gain H_{21} and Mason's unilateral gain of InAs channel QWFETs with (a) 3 µm and (b) 0.65 µm S/D spacings. The frequency range was from 2 to 40 GHz, and the devices were biased at $V_{DS} = 0.6$ V.

spacing by extrapolating H_{21} and U_g using least-squares fitting with a -20 dB/dec slope as compared with the case of $f_T = 185$ GHz and $f_{max} = 142$ GHz for the controlled device. This RF performance improvement was due to the decrease in source resistance (R_S) and the increase in g_m in the applied gate bias range. In addition, the H_{21} curve becomes straighter in at a lower frequency in Fig. 4(b), which is further evidence of the reduced R_S for a weak feedback effect. However, the fringing capacitance shows a small increase because of the close spacing between the electrodes. The capacitance at the gate-source end was extracted by high-frequency S-parameter measurement and observed to increase from 36.76 fF for the controlled device to 44.47 fF for the device with a 0.65 µm S/D spacing. It is believed that the DC and RF performances can be improved if we can design the optimal device layout with a low fringing capacitance.

In this study, the use of a new proposed redeposition ohmic technology to improve the DC and RF performances of the QWFETs has been demonstrated. The InAs-channel QWFETs exhibit $I_{DS} = 517$ mA/mm, $g_m = 1348$ mS/mm, and an f_T (f_{max}) of 205 GHz (170 GHz) after the redeposition ohmic metal process. It is believed that the novel and straightforward technology can markedly improve the DC and RF performances of the QWFETs. The device with the scaling of S/D spacing also maintains the well gate–drain breakdown voltage. The results demonstrated that a superior QWFET device performance enhancement for high-frequency, high-speed and low-power logic applications can be achieved through the adoption of a very simple ameliorated redeposition ohmic process with an optimal epitaxy. The parasitic source and drain resistances were significantly reduced from 5.0 to 1.1 Ω, as evidenced from the values extracted through S-parameter measurement.

Acknowledgements The authors would like to acknowledge the assistance and support from the National Science Council, R.O.C., under contract NSC 97-2221-E-155-070. This study was particularly supported by the "Aim for the Top University Plan" of the National Chiao Tung University and the Ministry of Education, Taiwan, R.O.C. Part of this study was supported by the "Nanotechnology Network Project" of the Ministry of Education, Culture, Sports, Science and Technology of Japan (MEXT).

1) W. Ha, K. Shinohara, and B. Brar: IEEE Electron Device Lett. **29** (2008) 419.
2) C.-I. Kuo, H.-T. Hsu, and E. Y. Chang: Electrochem. Solid-State Lett. **11** (2008) H193.
3) J. A. del Alamo and D. H. Kim: Proc. 19th Int. Conf. InP and Related Materials, 2007, p. 51.
4) B. O. Lim, M. K. Lee, T. J. Bake, M. Han, S. C. Kim, and J. K Rhee: IEEE Electron Device Lett. **28** (2007) 546.
5) D. A. J. Moran, E. Boyd, K. Elgaid, F. Mcewan, H. Mclelland, C. R. Stanley, and I. G. Thayne: Microelectron. Eng. **73** (2004) 814.
6) T. W. Kim, S. J. Jo, and J. I. Song: IEEE Electron Device Lett. **27** (2006) 722.
7) J. H. Huang, J. K. Abrokwah, and W. J. Ooms: Appl. Phys. Lett. **61** (1992) 2455.
8) D. A. Allan: IEE Proc., Part I **133** (1986) 18.

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