Modeling and Small-Signal Analysis of a Switch-Mode Rectifier With Single-Loop Current Sensorless Control

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***Abstract*—The conventional multiloop control with one inner current loop and one outer voltage loop is often applied to a single-phase boost-type switch-mode rectifier where the output of the voltage loop is a current amplitude signal. In the duty phase control (DPC) proposed recently, the output of the voltage loop is a phase signal used to generate the switching signals without current loop and sensing current. To improve the clamped current waveform of DPC, a single-loop current sensorless control (SLCSC) with some nominal parameters had also been proposed to compensate for the voltage drops across the switch, diodes, and inductor resistance. In this paper, the effect of the differences between nominal and real circuit parameters on the input current waveforms of SLCSC are addressed in detail. The results are helpful in the design of SLCSC. From the simulated and experimental results, we can find that the output voltage is well regulated by the only voltage loop and the input current harmonics are significantly improved.**

***Index Terms*—AC–DC power conversion.**

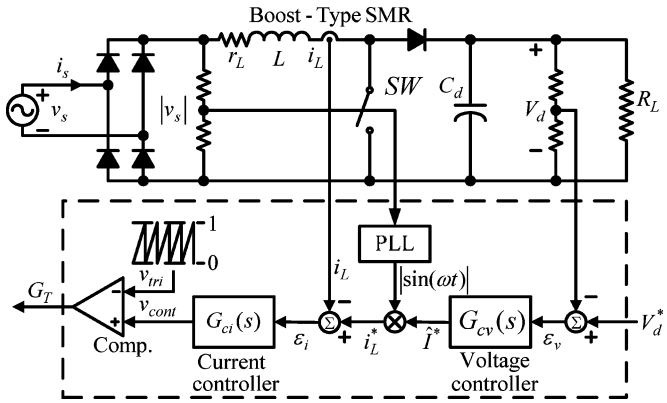

Fig. 1. Boost-type SMR with multiloop control.

I. Introduction

THE USE of ac/dc conversion has increased in a wide diversity of applications: power supplies for microelectronics, household electric appliances, electronics ballasts, battery charging, motor drives, power conversion, etc., which also results in the increase of input harmonic currents. Current harmonics have a negative effect on the electrical system and several standards have introduced important and stringent limits on harmonics.

Switching-mode rectifiers (SMRs) are an effective means to perform the qualified ac/dc conversion [1], [2], including input current shaping and output voltage regulation. Among all the power circuit topologies of SMR, the boost-type SMR, as shown in Fig. 1, is the most popular one for its continuous current in the boost inductors [2]. However, the qualified ac/dc functions must be met by adequately turning on and turning off the only controllable power switch in the boost-type SMR. According to the control structures, the SMR controls can be divided into two groups, where one is multiloop control [3]–[10] and the other single-loop control [11]–[17].

In the conventional multiloop control, as shown in Fig. 1, the inner current loop and the outer voltage loop work together to decide the conduction ratio of the only controllable switch. The former loop shapes input current waveform and the latter loop regulates the output voltage, respectively. In [3] and [4], a robust voltage control loop had been proposed to remove the effect of voltage ripple on the current command. Several intelligent current sampling algorithms proposed in [5] and [6] can sense current correctly, and many feedforward current controllers [3], [7], [8] had been used to help the current loop to obtain the large-variation control signal. Some sensorless multiloop controls for boost-type SMRs had been proposed in [9] and [10].

Furthermore, we can find that the output voltage loop is the only loop in the group of single-loop control [11]–[17] and all of them can be seen as sensorless controls, where [11]–[14] eliminate the senses of input voltage and [14]–[17] exclude the sensing of current. It is noted that the inductor currents in [11]–[14] are sensed and used in their single voltage loops. However, an essential zero-current detector is necessary to ensure the inductor current flowing at the boundary condition, which contributes to the variable switching frequency in [11]. On the contrary, fixed switching periods can be found in [12]–[17]. Additionally, all the outputs of the voltage loops in [12]–[15] adjust the amplitudes of the fixed-frequency carrier signals. Only a fixed-frequency fixed-amplitude carrier signal is used in [16] and [17]. It is noted that due to the digital resolution, implementing a fixed-amplitude carrier signal is easier than a variable–amplitude in digital signal processor (DSP)/field-programmable gate array (FPGA) based systems.

The duty phase control (DPC) with the single voltage loop is plotted in Fig. 2 [16], where the switching signal is obtained from the comparison of a control signal at "–" terminal and

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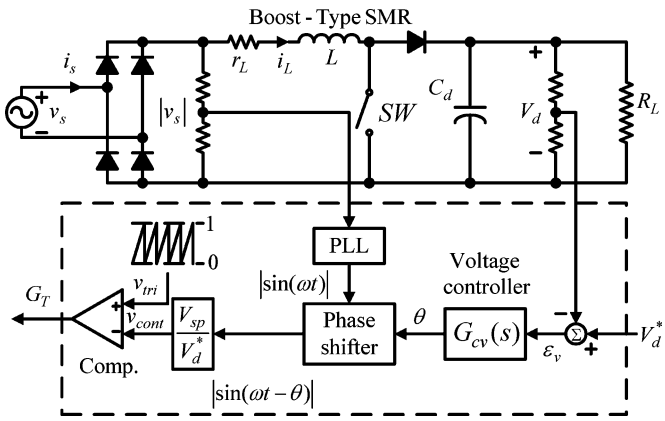

Fig. 2. Boost-type SMR with DPC [16].

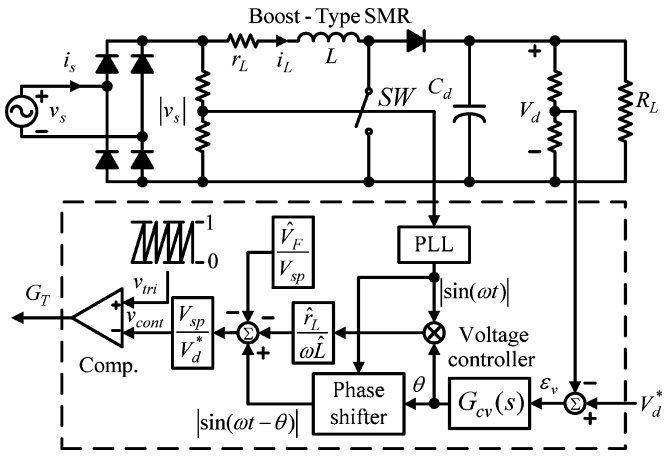

Fig. 3. Boost-type SMR with SLCSC [17].

a fixed-amplitude carrier signal at "+" terminal. The output of voltage controller is a phase signal, instead of the current amplitude in conventional multiloop control in Fig. 1. The performance of the proposed DPC had been evaluated and demonstrated from the simulated and experimental results in [16].

However, due to the real circuit elements, the resulting input current returns to zero early before the zero-crossing points of input voltage (i.e., clamped current). In order to improve the clamped input current waveform, a single-loop current sensorless control (SLCSC), plotted in Fig. 3, had also been proposed in [17] by adding two additional loops with nominal parameters to compensate for the voltage drops across the circuit elements. All the single-loop control methods can be summarized in Table I.

In [17], the sensitivity of the inductance parameter had even been studied by some simulation results. However, the following works here show that the input current waveform can be represented in terms of the circuit parameter and the parameter error. Consequently, the effect of parameter error on input current and the small-signal transfer function of output voltage response can be modeled, which also leads to this paper.

In this paper, the effect of the differences between nominal and real circuit parameters on the input current waveforms, and the modeling and small-signal analysis of SLCSC are addressed

TABLE I
SUMMARIZED RESULT FOR VARIOUS SINGLE-LOOP CONTROLS [11]–[17]

	[11]	[12]	[13]	[14]	[15]	[16]	[17]
Without sensing input voltage	√	√	√				
Without sensing current				√	√	√	√
Without sensing output voltage				√			
Variable switching frequency	√						
Fixed switching frequency		√	√	√	√	√	√
Variable-amplitude carrier		√	√	√	√		
Fixed-amplitude carrier						√	√
Without nominal circuit parameters	√	√	√	√	√	√	
With nominal circuit parameters							√

in detail. The result shows that the input current waveform of SLCSC is highly dependent on the circuit parameter error, not on the control parameters, whereas in multiloop control, the control parameters dominate the input current waveforms. Additionally, we understand that the parameter error would contribute to not only a clamped current but also a nonzero current at the zero-crossing points of input voltage (i.e., a hard-commutation current), which are helpful in the design of SLCSC.

Simply speaking, [17] is focused on the design and development of single-loop current control, and this paper has emphasized on the effect of parameter error and the small-signal transfer function between output voltage and control signal.

The paper is organized as follows. Initially, the input current of SLCSC is analyzed. The input current waveforms of SLCSC can be divided into three groups: sinusoidal currents, clamped currents, and hard-commutation currents. The model and small-signal analysis of the case of sinusoidal currents are derived. Finally, some simulated and experimental results have been given to illustrate the performances of the proposed SLCSC.

II. SINGLE-LOOP CURRENT SENSORLESS CONTROL (SLCSC)

A. Boost-Type SMR

As shown in Fig. 1, the power circuit of the boost-type SMR mainly consists of a diode bridge rectifier and a boost-type dc/dc converter. When the switch SW is turned on, the input current flows through two rectifier diodes and the inductor *L,* and returns to the source. Similarly, the input current flows through two rectifier diodes, inductor *L* and diode *D*, and returns to the source when the power switch SW is turned off.

Due to the boost-type topology, the inductor current must be either positive or clamped to zero (i.e., no negative current). In steady state, the inductor current must be periodic with each half line cycle, and can be expressed as a sum of infinite base current waveform $i_{Ln}(t-nT/2)$

$$i_L(t)=\sum_{n=-\infty}^{n=+\infty} i_{Ln}\left(t-n\frac{T}{2}\right) \tag{1}$$

where T is the period of input line cycle and

$$i_{Ln}(T/2)=i_{Ln}(0). \tag{2}$$

From the circuit topology shown in Fig. 1, the input current i_s is equal to positive inductor current i_L and negative inductor current $-i_L$, when the input voltage $v_s=V_{sp}\sin(\omega t)$ is positive and negative, respectively. Therefore, the input current can be

represented [10] by

$$i_s(t) = \text{sign}(v_s(t))i_L(t) = \text{sign}(\sin\omega t)i_L(t) \tag{3}$$

where $\text{sign}(\bullet)$ is the sign operator and is defined as

$$\text{sign}(X) = \begin{cases} +1, & \text{when } X \geq 0 \\ -1, & \text{when } X < 0. \end{cases} \tag{4}$$

In order to model the behavior of a boost-type SMR in a simplified way, the following assumptions are initially made.

1) Power switch SW is assumed to operate at a switching frequency approaching infinity.
2) The small phase signal $\theta \approx 0$ in radians is assumed and it follows that the approximations $\sin\theta \approx \theta$ and $\cos\theta \approx 1$ can be used.
3) A bulk capacitor C_d is assumed in the power circuit, which contributes to the steady-state output voltage V_d equal to voltage command V_d^*.
4) Both nominal sums of the conduction voltages in the loop of "switch SW ON" and "switch SW OFF" are assumed to be equal to V_F.

B. SLCSC

The configuration of the proposed SLCSC with the only voltage loop is plotted in Fig. 3. Like DPC in Fig. 2, the duty signal G_T is also generated from the comparison between a fixed triangle signal v_{tri} at "+" (the inverted commas have been retained for consistency) terminal and a control signal v_{cont} at "−" terminal and the output of voltage controller is a phase signal θ. To compensate for the effect of inductor resistance and conducting voltages on the input current waveform, the control signal v_{cont} in SLCSC is obtained by

$$v_{\text{cont}} = \frac{V_{sp}}{V_d^*}\left[|\sin(\omega t - \theta)| - \theta\frac{\hat{r}_L}{\omega\hat{L}}|\sin(\omega t)| - \frac{\hat{V}_F}{V_{sp}}\right] \tag{5}$$

where $\hat{r}_L$ and $\hat{L}$ represent the nominal circuit values, and $\hat{V}_F$ is the sum of all the nominal conduction voltages.

The differences between nominal values and real values can be represented as

$$\Delta r_L = \hat{r}_L - r_L \tag{6}$$

$$\Delta L = \hat{L} - L \tag{7}$$

$$\Delta V_F = \hat{V}_F - V_F \tag{8}$$

where r_L and L are the real values in the boost-type SMR and V_F is the sum of the real conduction voltages. With assumed infinite switching frequency, the average duty ratio signal $\bar{d}$ over one switching period can be represented in terms of the control signal v_{cont}

$$\bar{d} = 1 - v_{\text{cont}}. \tag{9}$$

Replacing v_{cont} in (9) by (5), the average duty ratio signal $\bar{d}$ can be obtained as

$$\bar{d} = 1 - \frac{V_{sp}}{V_d^*}|\sin(\omega t - \theta)| + \theta\frac{V_{sp}}{V_d^*}\frac{\hat{r}_L}{\omega\hat{L}}|\sin(\omega t)| + \frac{\hat{V}_F}{V_d^*}. \tag{10}$$

Then, we can write two Kirchhoff's voltage law (KVL) equations according to the conduction state of the power switch SW

$$L\frac{di_L}{dt} = V_{sp}|\sin(\omega t)| - i_L r_L - V_F \text{ when SW is "ON"} \tag{11}$$

$$L\frac{di_L}{dt} = V_{sp}|\sin(\omega t)| - V_d^* - i_L r_L - V_F \text{ when SW is "OFF"} \tag{12}$$

Multiplying (11) and (12) by the turn-ON time $\bar{d}T_s$ and the turn-OFF time $(1-\bar{d})T_s$, respectively, yields the following averaged equation:

$$L\frac{di_L}{dt} = V_{sp}|\sin(\omega t)| - (1-\bar{d})V_d^* - i_L r_L - V_F \tag{13}$$

where T_s is the switching period. Therefore, by substituting $\bar{d}$ in (10) into (13) and rearranging the other terms, we can obtain the following time-differential equations for inductor current i_L:

$$L\frac{di_L}{dt} = V_{sp}\left[|\sin(\omega t)| - |\sin(\omega t - \theta)| + \theta\frac{\hat{r}_L}{\omega\hat{L}}|\sin(\omega t)|\right] - r_L i_L + (\hat{V}_F - V_F). \tag{14}$$

Then, using the assumed $\sin\theta \approx \theta$, $\cos\theta \approx 1$ and the common trigonometric identity $\sin(A-B) = \sin A\cos B - \sin B\cos A$, we obtain the following approximation of (14):

$$L\frac{di_L}{dt} + r_L i_L \approx V_{sp}\left[|\sin(\omega t)| - |\sin(\omega t) - \theta\cos(\omega t)| + \theta\frac{r_L + \Delta r_L}{\omega(L+\Delta L)}|\sin(\omega t)|\right] + \Delta V_F. \tag{15}$$

Due to the assumption of small phase signal $\theta \approx 0$, the term $|\sin(\omega t)| - |\sin(\omega t) - \theta\cos(\omega t)|$ in (15) can be replaced by $\theta\text{sign}(\sin(\omega t))\cos(\omega t)$

$$L\frac{di_L}{dt} + r_L i_L \approx V_{sp}\theta\left[\text{sign}\,\sin(\omega t)\,\cos(\omega t) + \frac{r_L + \Delta r_L}{\omega(L+\Delta L)}|\sin(\omega t)|\right] + \Delta V_F \tag{16}$$

where the function of $\text{sign}(X)$ had been defined in (4).

C. Input Current Waveforms

As shown in (1), the steady-state inductor current is repeated with each half line cycle and can be represented by the sum of base currents $i_{Ln}(t - nT/2)$. Thus, only considering the first half line cycle ($0 \sim T/2$) contributes to the following equalities $\text{sign}(\sin(\omega t)) = 1$, $|\sin(\omega t)| = \sin(\omega t)$, and

$$L\frac{di_{Ln}}{dt} + r_L i_{Ln} \approx V_{sp}\theta\left[\cos(\omega t) + \frac{r_L + \Delta r_L}{\omega(L+\Delta L)}\sin(\omega t)\right] + \Delta V_F. \tag{17}$$

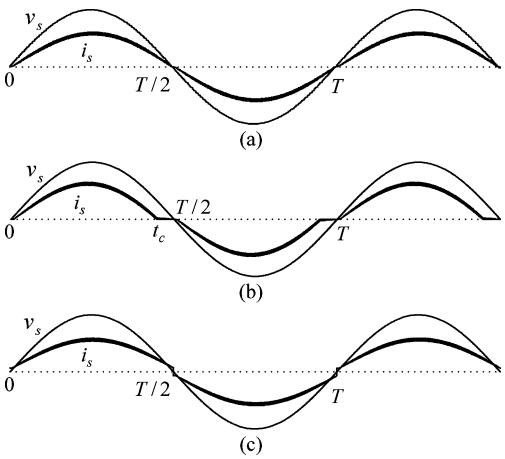

Fig. 4. Illustrated waveforms for: (a) sinusoidal input current, (b) clamped input current, and (c) hard-commutation input current.

Then, solving (17) yields the base current $i_{Ln}(t)$ during the first half line cycle $0 \sim T/2$

$$i_{Ln}(t) \approx \left\{ \begin{array}{l} \dfrac{V_{sp}\theta}{\omega L}\sin(\omega t) + i_{Ln}(0)e^{-\frac{\omega}{Q_L}t} + \dfrac{\Delta V_F}{r_L}(1 - e^{-\frac{\omega}{Q_L}t}) \\ \quad + k\dfrac{V_{sp}\theta}{\omega L}\sin\alpha_L[-\cos(\omega t + \alpha_L) + \cos\alpha_L e^{-\frac{\omega}{Q_L}t})] \end{array} \right\} \times \left[u(t) - u\left(t - \frac{T}{2}\right)\right] \tag{18}$$

where $\omega(T/2) = \pi$, Q_L denotes the quality factor of inductor *L*

$$Q_L = \frac{\omega L}{r_L} = \cot(\alpha_L) \tag{19}$$

and the factor *k* represents the equivalent parameter error

$$k = \frac{L\Delta r_L - r_L \Delta L}{r_L(L + \Delta L)}. \tag{20}$$

It is noted that the zero equivalent parameter error $k = 0$ implies

$$\frac{\Delta r_L}{r_L} = \frac{\Delta L}{L}. \tag{21}$$

Due to the effects of parameter errors Δr_L, ΔL, and ΔV_F on (18), the operation of SMR with SLCSC can be divided into three cases according to the input current waveforms plotted in Fig. 4.

III. Small-Signal Model

A. Sinusoidal Input Current

With the condition of zero equivalent parameter error $k = 0$ and zero conduction voltage $\Delta V_F = 0$, the base current in (18) becomes

$$i_{Ln}(t) \approx \left[\frac{V_{sp}\theta}{\omega L}\sin(\omega t) + i_{Ln}(0)e^{-\frac{\omega}{Q_L}t}\right]\left[u(t) - u\left(t - \frac{T}{2}\right)\right] \tag{22}$$

and from (2), obviously, the initial value $i_{Ln}(0)$ in this case must be zero. From (1), the inductor current i_L becomes a rectified sinusoidal waveform

$$i_L(t) \approx \sum_{n=-\infty}^{n=+\infty} \frac{V_{sp}\theta}{\omega L}\sin(\omega t - n\pi) \times \left[u\left(t - n\frac{T}{2}\right) - u\left(t - n\frac{T}{2} - \frac{T}{2}\right)\right] = \frac{V_{sp}\theta}{\omega L}|\sin\omega t|. \tag{23}$$

From (3), the input current $i_s(t)$ can be expressed as

$$i_s(t) \approx \frac{V_{sp}\theta}{\omega L}\sin(\omega t) = I_{sp}\sin(\omega t). \tag{24}$$

We can find that the input current i_s is automatically shaped to a sinusoidal waveform in phase with the input voltage v_s, as shown in Fig. 4(a). The current amplitude I_{sp} is proportional to the controllable phase θ. Obviously, the input power P_s is controllable by the only voltage controller in SLCSC.

The transfer function between the output voltage perturbation ΔV_d and the phase perturbation $\Delta\theta$ can be obtained from the power balance between input power P_s, output power P_d, and capacitor power P_C. The input power P_s with small perturbation ΔP_s becomes

$$P_s + \Delta P_s = \frac{V_{sp}^2(\theta + \Delta\theta)}{2\omega L} = \frac{V_{sp}^2\theta}{2\omega L} + \frac{V_{sp}^2\Delta\theta}{2\omega L}. \tag{25}$$

The output power P_d with small perturbation ΔP_d can be represented by the load perturbation ΔR_L and the output voltage perturbation ΔV_d

$$P_d + \Delta P_d = \frac{(V_d^* + \Delta V_d)^2}{R_L + \Delta R_L} \approx \frac{(V_d^*)^2}{R_L} + \frac{(V_d^*)^2}{R_L}\left(-\frac{\Delta R_L}{R_L}\right) + \frac{2V_d^*\Delta V_d}{R_L}. \tag{26}$$

The small perturbation ΔP_C of capacitor power can be represented by the output voltage perturbation ΔV_d

$$\Delta P_C = \frac{d\left(\frac{C}{2}(V_d^* + \Delta V_d)^2\right)}{dt} \approx CV_d^*\frac{d\Delta V_d}{dt}. \tag{27}$$

The balance between the power perturbations $\Delta P_s = \Delta P_C + \Delta P_d$ can yield the following two small-signal transfer functions for the sinusoidal current case

$$G_s(s) = \frac{\Delta V_d}{\Delta\theta} = \frac{V_{sp}^2}{2CV_d^*\omega L}\frac{1}{s + 2/(CR_L)} \tag{28}$$

$$G_d(s) = \frac{\Delta V_d}{\Delta R_L} = \frac{V_d^*}{CR_L^2}\frac{1}{s + 2/(CR_L)}. \tag{29}$$

Obviously, the behavior of output voltage can be seen as a first-order model, and thus, the desired output voltage can be well regulated by using simple plus integral (PI) type controller. The equivalent small-signal model of SLCSC with sinusoidal input current is plotted in Fig. 5.

B. Clamped Input Current

In a boost-type SMR, the inductor current must be either positive value or zero value. Thus, when the values ΔV_F, Δr_L, and ΔL make the calculated base current value in (18) turning

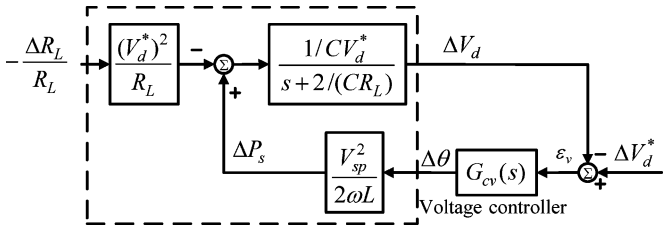

Fig. 5. Equivalent small-signal model of SLCSC with sinusoidal input current.

TABLE II
GENERAL TRENDS OF INPUT CURRENT WAVEFORMS IN TERMS OF k AND ΔV_F

	$k=\frac{L\Delta r_L - r_L\Delta L}{r_L(L+\Delta L)}<0$	$k=\frac{L\Delta r_L - r_L\Delta L}{r_L(L+\Delta L)}=0$	$k=\frac{L\Delta r_L - r_L\Delta L}{r_L(L+\Delta L)}>0$
$\Delta V_F<0$	*Clamped input current*	*Clamped current*	*either Hard-commutation or Clamped input current*
$\Delta V_F=0$		*Sinusoidal current*	*Hard-commutation input current*
$\Delta V_F>0$	*either Hard-commutation or Clamped input current*	*Hard-commutation current*	

from a positive value to a negative value, the real inductor current must be clamped to zero until the arrival of the next half line cycle, as shown in Fig. 4(b).

Due to the clamped current, the initial value of current is also zero $i_{Ln}(0)=0$. Obviously, the current in (18) will be clamped to zero when equivalent parameter error $k\le 0$ and $\Delta V_F \le 0$ because the functions $1-e^{-\frac{\omega}{Q_L}t}$ and $\cos\alpha_L e^{-\frac{\omega}{Q_L}t} - \cos(\omega t+\alpha_L)$ are positive at the end of each half line period. The general trends of input current waveforms in terms of *k* and ΔV_F are tabulated in Table II.

Applying zero initial current $i_{Ln}(0)=0$, and substituting $\sin\alpha_L = 1/\sqrt{(1+Q_L^2)}$ and $\cos\alpha_L = Q_L/\sqrt{(1+Q_L^2)}$ into (19), the clamped base current $i_{Ln}(t)$ can be rewritten as

$$i_{Ln}(t)\approx\left\{\begin{array}{l}\frac{V_{sp}\theta}{\omega L}\left[\left(1+k\frac{1}{1+Q_L^2}\right)\sin\omega t - k\frac{Q_L}{1+Q_L^2}\cos\omega t\right.\\ \quad\left.+k\frac{Q_L}{1+Q_L^2}e^{-\frac{\omega}{Q_L}t}\right][u(t)-u(t-t_c)]\\ \quad+\frac{\Delta V_F}{r_L}(1-e^{-\frac{\omega}{Q_L}t})[u(t)-u(t-t_c)]\end{array}\right\} \tag{30}$$

where t_c denotes the current clamping instant smaller than the half line period $0<t_c\le T/2$.

Because the last term $(1-e^{-\frac{\omega}{Q_L}t})[u(t)-u(t-t_c)]$ is not a function of control signal θ, error ΔV_F has no effect on the small-signal transfer function $\Delta V_d/\Delta\theta$. In order to simplify the analysis, zero parameter error ΔV_F is assumed here in the derivation of small-signal transfer function. It follows that from (1) and (3), the simplified clamped input current $i_{s,c}(t)$ can be expressed as shown (31), at the bottom of this page.

By expressing $i_{s,c}(t)$ as fourier series, the component $I_{s,c}$ of fundamental current in phase with the input voltage $V_{sp}\sin(\omega t)$ can be expressed as

$$I_{s,c}=\frac{V_{sp}\theta}{\omega L}F_c(k,Q_L) \tag{32}$$

where (33), as shown at the bottom of this page.

Then, the small perturbation ΔP_s resulting from phase perturbation $\Delta\theta$ now becomes

$$\Delta P_s = F_c(k,Q_L)\frac{V_{sp}^2}{2\omega L}\Delta\theta. \tag{34}$$

By following the steps in (26)–(28), we can obtain the small-signal transfer function $G_c(s)$ for clamped input current case in terms of $G_s(s)$ in (28)

$$\begin{aligned}G_c(s) &= F_c(k,Q_L)\frac{V_{sp}^2}{2CV_d^*\omega L}\frac{1}{s+2/(CR_L)}\\ &= F_c(k,Q_L)G_s(s).\end{aligned} \tag{35}$$

Obviously, small-signal transfer function $G_c(s)$ for clamped current can be seen as $G_s(s)$ with a modified factor $F_c(k,Q_L)$. In addition, the response ΔV_d due to the load perturbation ΔR_L is the same as (29) because the equivalent parameter error only contributes to the input power perturbation.

However, in the former two cases of sinusoidal input current and clamped input current, both the initial values of repeated current are zero, and thus, the current commutation operates at zero current and can be regarded as soft-commutation operations. However, in the following case, the current commutation operates at nonzero current and must be seen as a hard-commutation operation.

$$i_{s,c}(t)=\frac{V_{sp}\theta}{\omega L}\sum_{n=-\infty}^{n=+\infty}\left[\begin{array}{l}\left(1+k\frac{1}{1+Q_L^2}\right)\sin\omega t\left[u\left(t-n\frac{T}{2}\right)-u\left(t-t_c-n\frac{T}{2}\right)\right]\\ -k\frac{Q_L}{1+Q_L^2}\cos\omega t\left[u\left(t-n\frac{T}{2}\right)-u\left(t-t_c-n\frac{T}{2}\right)\right]\\ +k\frac{Q_L}{1+Q_L^2}\mathrm{sign}(\sin\omega t)e^{-\frac{\omega t-nT/2}{Q_L}}\left[u\left(t-n\frac{T}{2}\right)-u\left(t-t_c-n\frac{T}{2}\right)\right]\end{array}\right] \tag{31}$$

$$F_c(k,Q_L)=\left[\begin{array}{l}\left(1+k\frac{1}{1+Q_L^2}\right)\left(\frac{2t_c}{T}-\frac{1}{2\pi}\sin 2\omega t_c\right)-k\frac{Q_L}{1+Q_L^2}\frac{1-\cos 2\omega t_c}{2\pi}\\ +\frac{2}{\pi}k\frac{Q_L^2}{(1+Q_L^2)^2}(Q_L-Q_L\cos\omega t_c e^{-\frac{\omega t_c}{Q_L}}-\sin\omega t_c e^{-\frac{\omega t_c}{Q_L}})\end{array}\right]. \tag{33}$$

C. Hard-Commutation Input Current

Alternatively, the values ΔV_F, Δr_L, and ΔL may result in a positive inductor current at the end of each half line cycle, which would force the current commutating from two bridge diodes to the other ones at the zero-crossing points of the input voltage. Substituting (18) into (2) and solving the equation yields the initial current value of hard-commutation input current

$$i_{Ln}(0) = \frac{\Delta V_F}{r_L} + k\frac{V_{sp}\theta}{\omega L}\frac{Q_L}{1+Q_L^2}\frac{1+e^{-\frac{\pi}{Q_L}}}{1-e^{-\frac{\pi}{Q_L}}}. \quad (36)$$

Substituting (36) into (18), the base current for hard-commutation current becomes

$$i_{Ln}(t) \approx \left\{ \begin{array}{l} \dfrac{V_{sp}\theta}{\omega L}\left(1+k\dfrac{1}{1+Q_L^2}\right)\sin\omega t - k\dfrac{V_{sp}\theta}{\omega L}\dfrac{Q_L}{1+Q_L^2}\cos\omega t \\ \quad +k\dfrac{V_{sp}\theta}{\omega L}\dfrac{Q_L}{1+Q_L^2}\dfrac{2}{1-e^{-\frac{\pi}{Q_L}}}e^{-\frac{\omega}{Q_L}t} + \dfrac{\Delta V_F}{r_L} \end{array} \right\} \times \left[u(t) - u\left(t-\frac{T}{2}\right)\right]. \quad (37)$$

Because the constant $\Delta V_F/r_L$ in (37) is not a function of control signal θ, the parameter error ΔV_F has no effect on the small-signal transfer function. In order to simply the analysis, the parameter error ΔV_F is assumed to be zero here in the following derivation for hard-commutation current case. From (1) and (3), the simplified hard-commutation input current $i_{s,h}(t)$ can be expressed as shown (38), at the bottom of this page.

By expressing $i_{s,h}(t)$ as a fourier series, the component $I_{s,h}$ of fundamental current in phase with the input voltage $V_{sp}\sin(\omega t)$ can be obtained as

$$I_{s,h} = \frac{V_{sp}\theta}{\omega L}F_h(k,Q_L) \quad (39)$$

where

$$F_h(k,Q_L) = \left[\left(1+k\frac{1}{1+Q_L^2}\right) + k\frac{4}{\pi}\frac{Q_L^3}{(1+Q_L^2)^2}\frac{1+e^{-\frac{\pi}{Q_L}}}{1-e^{-\frac{\pi}{Q_L}}}\right]. \quad (40)$$

Then, the input power perturbation ΔP_s resulting from $\Delta\theta$ now becomes

$$\Delta P_s = F_h(k,Q_L)\frac{V_{sp}^2\Delta\theta}{2\omega L}. \quad (41)$$

By following the steps in (26)–(28), we can obtain the small-signal transfer function for hard-commutation input current

$$G_h(s) = F_h(k,Q_L)\frac{V_{sp}^2}{2CV_d^*\omega L}\frac{1}{s+2/(CR_L)} = F_h(k,Q_L)G_s(s). \quad (42)$$

Obviously, small-signal transfer function $G_h(s)$ for clamped current can be seen as $G_s(s)$ with a modified factor $F_h(k,Q_L)$. However, we can find that in the former two cases, all the bridge diodes turn off with zero current switching (ZCS), but in this case, the bridge diodes turn off with a nonzero current, which would contribute to excess loss and reduce the overall efficiency. In addition, the sudden current change would also result in larger current harmonics than in the former two cases.

TABLE III
SIMULATED CIRCUIT PARAMETERS

Input line voltage (peak)	$\hat{V}_s = 155V$ ($110V_{rms}$)
Output voltage command	$V_d^* = 300V$
Input line frequency	$f = 60Hz$
Smoothing inductance	$L = 2.056mH$
Smoothing capacitance	$C_d = 470\mu F$
ESR of boost inductance	$r_L = 0.1773\Omega$
Conduction voltage	$V_F = 3V$
Carrier frequency	$f_{tri} = 50\,kHz$
Rated power	$P_s = 675W$ ($R_L = 133.333\Omega$)

IV. SIMULATIONS

In this section, we begin with a series of computer simulations to demonstrate the results of analysis. All simulated circuit elements are listed in Table III, and a simple PI controller is used as the only voltage controller to adjust the phase signal.

A. Sinusoidal Input Current

By choosing the nominal parameters equal to the real ones (i.e., $\Delta V_F = \Delta r_L = \Delta L = 0$), the simulated input currents and output voltages under various output power are shown in Fig. 6, respectively. We can find that the output voltage is well regulated to the voltage command $V_d^* = 300$ V and the sinusoidal input currents are in phase with the input voltage. Therefore, the proposed SLCSC can obtain high-quality ac/dc performance with only one voltage loop.

Additionally, substituting the simulated parameters in Table II into the equivalent model (28) yields the following s-domain

$$i_{s,h}(t) = \frac{V_{sp}\theta}{\omega L}\sum_{n=-\infty}^{n=+\infty}\left[\begin{array}{l} \left(1+k\dfrac{1}{1+Q_L^2}\right)\sin\omega t\left[u\left(t-n\dfrac{T}{2}\right) - u\left(t-\dfrac{T}{2}-n\dfrac{T}{2}\right)\right] \\ \quad -k\dfrac{Q_L}{1+Q_L^2}\cos\omega t\left[u\left(t-n\dfrac{T}{2}\right) - u\left(t-\dfrac{T}{2}-n\dfrac{T}{2}\right)\right] \\ \quad +\mathrm{sign}(\sin\omega t)k\dfrac{Q_L}{1+Q_L^2}\dfrac{2}{1-e^{-\frac{\pi}{Q_L}}}e^{-\frac{\omega t - nT/2}{Q_L}}\left[u\left(t-n\dfrac{T}{2}\right) - u\left(t-\dfrac{T}{2}-n\dfrac{T}{2}\right)\right] \end{array}\right]. \quad (38)$$

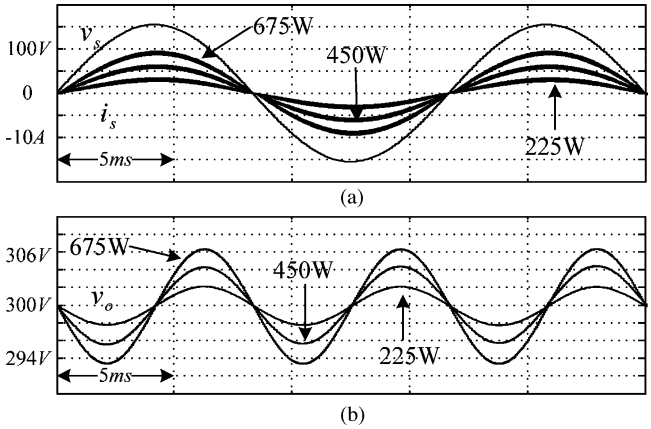

Fig. 6. (a) Simulated input voltage and input current. (b) Output voltage under various load conditions.

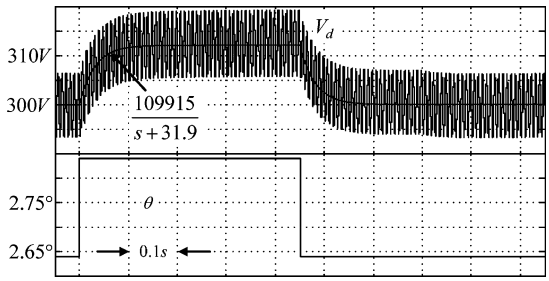

Fig. 7. Output voltage response due to the step change of phase signal.

transfer function where the phase signal is in radians

$$G_s(s) = \frac{109915}{s + 31.9}. \tag{43}$$

The response of the output voltage V_d due to the step change of phase signal $\Delta\theta = 0.2^\circ$ is plotted in Fig. 7, where the transfer function in (43) is also included for comparison. We can find that the behavior of (43) is close to the average value response of the simulated output voltage V_d, which also demonstrates the developed equivalent model in Fig. 5.

B. Clamped and Hard-Switching Input Currents

In order to understand the effect of parameter error, several current waveforms are plotted in Fig. 8, where the used nominal values are tabulated in Table IV. Cases (i) and (ii) yield the same value $k = -0.5$ from (19), and thus, contribute to the same clamped current waveforms shown in Fig. 8(a). Likewise, cases (iii) and (iv) have the same value $k = 0.25$ from (19), and thus, they contribute to the same hard-commutation current waveforms in Fig. 8(b). Fig. 8(c) and (d) plots the input current waveforms corresponding to the overcompensation $\Delta V_F > 0$ and undercompensation $\Delta V_F < 0$ of conduction voltages, respectively.

Case (vii) is a special case where zero nominal values $\hat{r}_L = 0$, $\hat{V}_F = 0$ (i.e., $k = -1$) are used and longer time of clamped current can be found in Fig. 8(e). In fact, SLCSC with zero nominal values in Fig. 3 can be seen as DPC in Fig. 2. However,

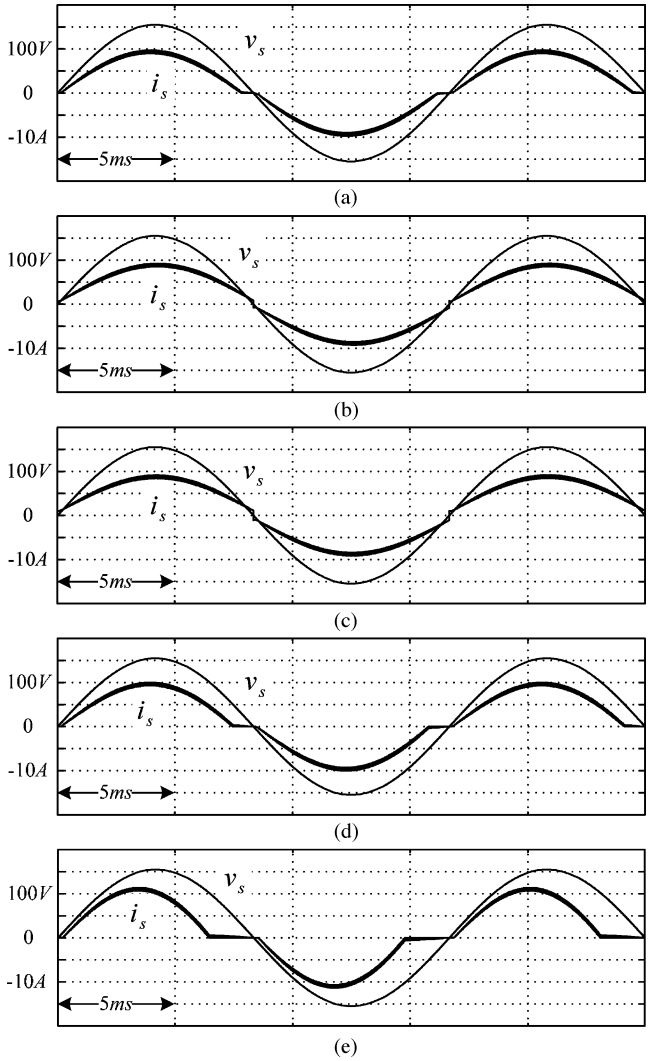

Fig. 8. Simulated input currents with various nominal values tabulated in Table IV.

TABLE IV
SIMULATED CASES FOR VARIOUS NOMINAL VALUES

		Simulation	Experiment
(i) $\hat{r}_L = 0.5r_L$, $\hat{L} = L$, $\hat{V}_F = V_F$ (ii) $\hat{L} = 2L$, $\hat{r}_L = r_L$, $\hat{V}_F = V_F$	$k = -0.5$, $\Delta V_F = 0$	**Fig. 8(a)**	
(iii) $\hat{r}_L = 1.25r_L$, $\hat{V}_F = V_F$, $\hat{L} = L$ (iv) $\hat{L} = 0.8L$, $\hat{r}_L = r_L$, $\hat{V}_F = V_F$	$k = 0.25$, $\Delta V_F = 0$	Fig. 8(b)	
(v) $\hat{L} = L$, $\hat{r}_L = r_L$, $\hat{V}_F = 1.1V_F$	$k = 0$, $\Delta V_F > 0$	Fig. 8(c)	
(vi) $\hat{L} = L$, $\hat{r}_L = r_L$, $\hat{V}_F = 0.5V_F$	$k = 0$, $\Delta V_F < 0$	Fig. 8(d)	
(vii) DPC case $\hat{r}_L = 0$, $\hat{V}_F = 0$	$k = -1$, $\Delta V_F < 0$	Fig. 8(e)	Fig. 10(c)

all the input currents in Fig. 8 can be found stable, and SLCSC is able to operate stably.

C. Transient Response

In order to understand the transient response of the proposed SLCSC, the simulated waveforms of sudden load change without parameter error and with parameter error are plotted in Fig. 9(a) and (b), respectively. To meet the change of load, the input current magnitude increases from about 6 to about 10 A by SLCSC.

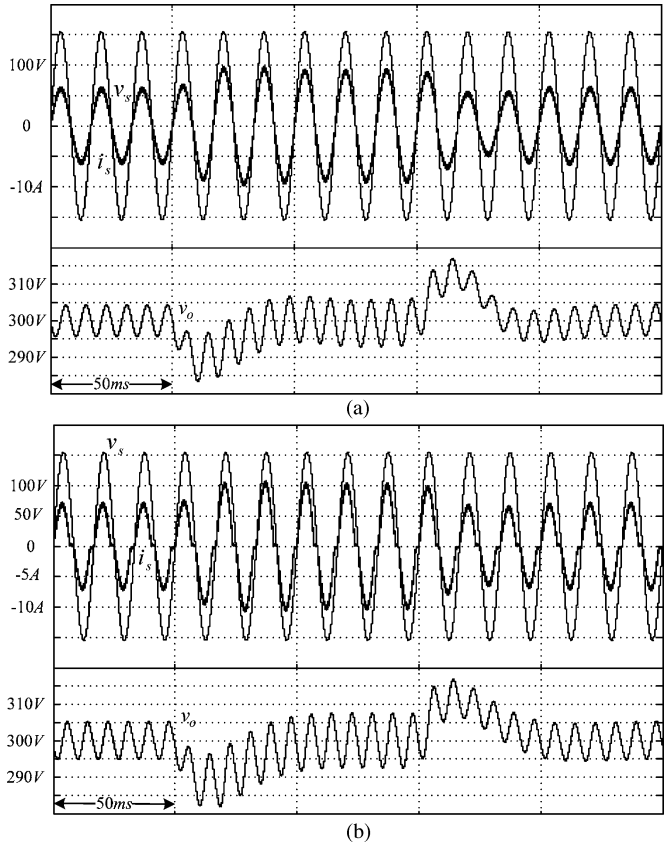

Fig. 9. Simulated waveforms during load regulation: (a) $\Delta r_L = 0, \Delta L = 0, \Delta V_F = 0$. (b) $\Delta r_L = 0.5 r_L, \Delta L = -0.5L, \Delta V_F = 0.5 V_F$.

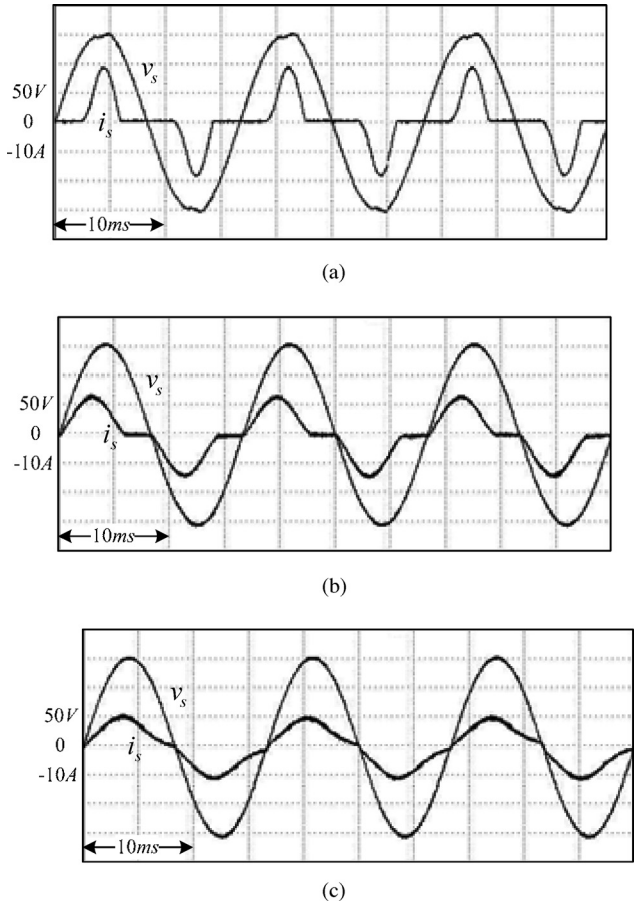

Fig. 10. Experimental input voltages and currents at 675 W. (a) For an SMR without turning on the power switch. (b) For a DPC-controlled SMR. (c) For an SLCSC-controlled SMR with nearly exact parameter.

In Fig. 9(a), we can find that the sinusoidal current is in phase with the input voltage during the transient period. Although the input current in Fig. 9(b) is clamped to zero due to the parameter error, the output voltage is still well regulated.

D. Comments

The sinusoidal input current case is not practical because we cannot determine the real values exactly. However, it is better to keep in clamped current than hard-commutation current. That is, it is preferred to select a larger nominal value of inductance ($\hat{L} > L$), smaller nominal values of resistance ($\hat{r}_L < r_L$), and nominal conduction voltage ($\hat{V}_F < V_F$) to operate SMR efficiently with clamped input current during the design of SLCSC.

V. Experimental Results

In this paper, SLCSC had been digitally implemented in an FPGA-based system using Xilinx XC3S200, where the DPC and SLCSC in [16] and [17] were implemented in DSP TMS320F240. Due to the measurement uncertainty, it is not easy to obtain the real values. In practice, some circuit parameters, such as inductance, resistance, and conduction voltages, may have small fluctuation with the instantaneous input current. However, we measure the parameters as exact as we can. All the measured circuit parameters have been listed in Table III and can be regarded as the nearly exact parameters.

Turning off the single power switch in a boost-type SMR obtains the pulse current waveform plotted in Fig. 10(a). The input current harmonics are tabulated in Table V, where the load resistance is decreased to about $30\,\Omega$ to yield the rated power 675 W. The input current is highly discontinuous and the peak current is high up to 20 A.

Fig. 10(b) plots the input current, where SLCSC with zero nominal values (i.e., DPC case in Table IV) is used to turn on and turn off the power switch to regulate the output voltage with the rated power of 675 W. We can find that the peak value of the clamped current decreases from 20 to about 12 A, and the total harmonic distortion factor (THD) decreases to the half of Fig. 10(a). However, due to the larger phase between the input voltage and input fundamental current in Fig. 10(b) than that in Fig. 10(a), the displacement power factor (DPF) decreases from 0.978 lagging to 0.908 leading.

Fig. 10(c) plots the input current where SLCSC with nearly exact parameters are used to regulate the output voltage. Due to the fluctuation of the circuit parameter with temperature and current, the input current is not a pure sinusoidal waveform, but is continuous. Due to the increase of DPF in Fig. 10(c), the peak current decreases to about 10 A, the power factor increases from 0.758 to 0.982, and THD decreases from 76.4% to 12.4%.

TABLE V
INPUT CURRENT HARMONICS AND THE LIMITS OF IEC-61000-3-2

Harmonics	Class A(A)	Fig.10(a)	Fig.10(b)	Fig.10(c)
1	X	6.55	7.016	6.514
3	2.300	4.49	2.571	0.702
5	1.140	1.789	0.218	0.190
7	0.770	0.403	0.097	0.138
9	0.400	0.605	0.155	0.111
11	0.330	0.330	0.093	0.076
13	0.210	0.322	0.014	0.058
15	0.150	0.222	0.045	0.039
17	0.132	0.163	0.036	0.033
19	0.118	0.160	0.005	0.032
21	0.107	0.098	0.017	0.027
Total Harmonic Distortion Factor		76.4%	36.4%	12.4%
Power Factor		0.758	0.853	0.982
Displacement Power Factor		0.978 lagging	0.908 leading	0.985 leading

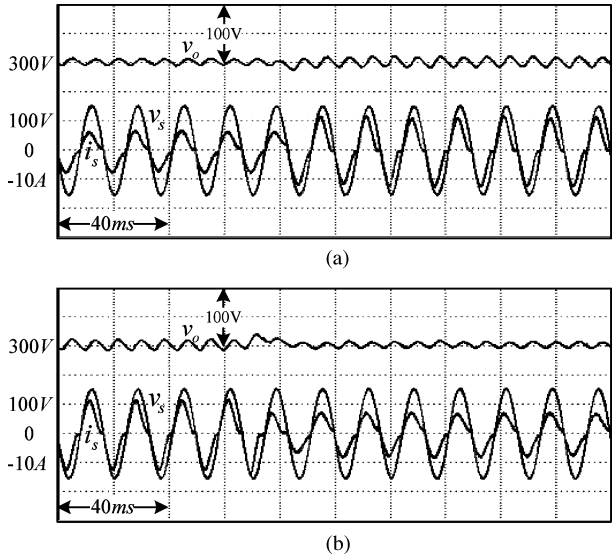

Fig. 11. Experimental waveforms when the load is suddenly changed. (a) From 450 to 675 W. (b) From 675 to 450 W.

Because of the continuous current, less current harmonics are found in Fig. 10(c) than those in Fig. 10(b).

All the current harmonics are tabulated in Table V, where the harmonic limits of IEC-61000-3-2 class A are also listed for comparison. It is noted that the input current waveform in (18) is highly dependent on the parameter errors and the quality factor Q_L in (19), especially when zero nominal values are included in DPC. The PI parameter of voltage loop can improve the response, but does not dominate the compliance of the IEC-61000-3-2 class A. Due to the absence of design optimization in the experiment, the input current harmonics in Fig. 10(c) are compliant to the limit of class A, but those in Fig. 10(b) are not.

To verify the dynamic performance of the proposed SLCSC with nearly exact parameters, some waveforms are plotted in Fig. 11 where the load condition is suddenly changed between 450 and 675 W. During the regulation, the input current is in phase with the input voltage, thus clearly showing that the proposed SLCSC also possesses good performance of regulation.

VI. CONCLUSION

In this paper, the effects of nominal parameter error on the input current waveforms and the small-signal model for a boost-type SMR with SLCSC have been addressed. The results also show that the parameter errors and the quality factor of inductor have a great effect on the input current waveform, and therefore, dominate the compliance of harmonic limits, not the control parameters. Due to the concerns of efficiency and current harmonics, it is better to keep SMR operating with clamped current than with hard-commutation current.

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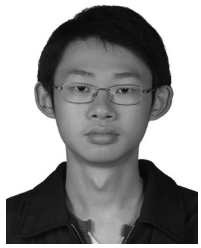

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