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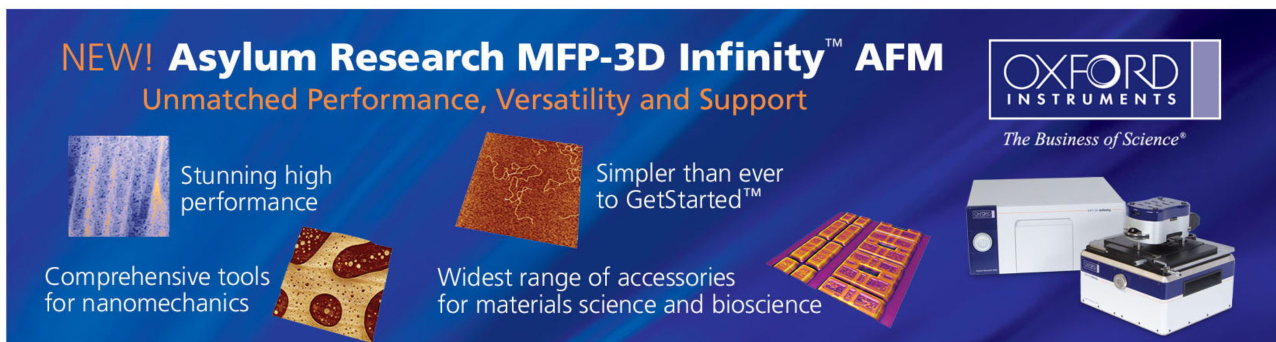

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Gate-to-drain capacitance verifying the continuous-wave green laser crystallization n-TFT trapped charges distribution under dc voltage stress

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In this work, a metrology was proposed to realize the distribution of fixed oxide trapped charges and grain boundary trapped states. The (continuous-wave green laser crystallization) n-channel thin-film transistors (TFTs) were forced by dc voltage stress, $V_G = V_D$. The gate-to-drain capacitance, $C_{GD} - V_G$, with varying frequency of applied small signal was developed. To probe the distribution of these defects, the difference (initial capacitance values minus stressed capacitance values) of $C_{GD} - V_G$ with different frequencies was precisely studied. © *2009 American Institute of Physics*. [doi:10.1063/1.3275728]

The continuous-wave green laser crystallization (CGLC) n-TFT had been manufactured successfully with its excellent output characteristic and high mobility.[1,2] The high carrier mobility of LTPS-TFTs is one of candidate for fabricating driver integrated circuit in TFT process. However, most of TFTs were made on quartz or glass substrate with no substrate (or bulk) terminal, and hence, there is seldom measurement techniques, such as charge-pumping or gated-diode methods, can be used to realize the shift in threshold voltage. In this study, as CGLC n-TFT was forced by the dc voltage stress, $V_G = V_D$, electrons injected into gate insulator and break the Si–H bond on the interface between channel and gate insulator. Moreover, there are a large number of Si–H bonds at the grain boundary of channel layer, and hence, after stressed, traps will be produced. The $C_{GD} - V_G$ curve, which was reported in several literatures,[3–5] was adopted instead of *I-V* curves to analyze the characteristic of CGLC n-TFT after dc voltage stressed. The stress voltage was gate voltage was equal to drain voltage and can be referred to some lectures.[6–8] The stretched and shifted $C_{GD} - V_G$ curve was attributed to the increased of oxide trapped charges, interface states, and deep trap states as TFT devices were stressed by the dc voltage. The TCAD tool was performed to simulate the vertical and lateral electrical field while stressing, and the result of TCAD assisted in verifying the location of oxide trapped charges and deep trap states.

A transparent quartz glass was employed as a substrate. Nitride layer (SiN_x), buffer silicon dioxide (SiO_2), and amorphous silicon (a-Si) films were sequentially deposited on this substrate. The nitride layer is used to form a barrier layer between substrate and buffer oxide and gather the mobile ions, not to influence the electrical characteristics of TFTs. The buffer SiO_2 may reduce the stress effect between a-Si and SiN_x. Then, the continuous-wave green laser, diode pumped solid state CW laser (l=532 nm [second harmonics (2ω) of Nd:YVO_4], irradiated on a-Si film to produce a numbers of grain in channel as a gate channel. Next, the gate dielectric TEOS-SiO_2 (tetraethoxysilane) was deposited with 100 nm thickness by plasma-enhanced chemical vapor deposition technology at 300 °C. Furthermore, the active region of a TFT transistor on the CGLC poly-Si was fabricated.

The dc voltage stress condition was $V_G = V_D = 16$ V. The stress and measurement instruments are Keithley 4200 semiconductor parameter analyzer and Agilent 4284A LCR meter. A simple illustration of the CGLC n-TFT is presented in Fig. 1. High lateral voltage (V_D) will accelerate the flowing electrons in the channel and cause impact ionization, and hence damage which is near drain side have been raised from these hot electrons. In addition, high vertical voltage (V_G) will attract the flowing electrons and move toward the interface of silicon channel and gate oxide insulator. Therefore, the interface and insulator may be damaged during stressing.

The impact ionization in Fig. 1 was led by hot carrier effect (HCE) which causes a formation of electron-hole-pairs, EHPs.[9,10] The generation electrons injected into gate oxide layer, which can be referred to lucky current model, to form oxide trapped charges and interface states.[11] Otherwise, the generation holes reflowed to source terminal causing grain boundary states. The path of hole reflowing is described in Fig. 1.[12] Therefore, a shift of threshold voltage

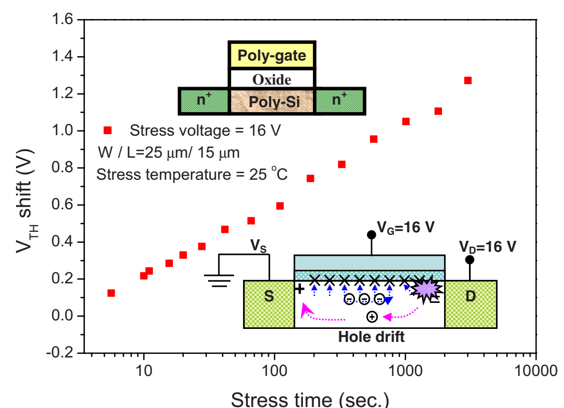

FIG. 1. (Color online) An illustration of cross-section view of CGLC n-TFT, hot carrier effect on CGLC n-TFT, and shift in threshold voltage on CGLC n-TFT under dc voltage stress.

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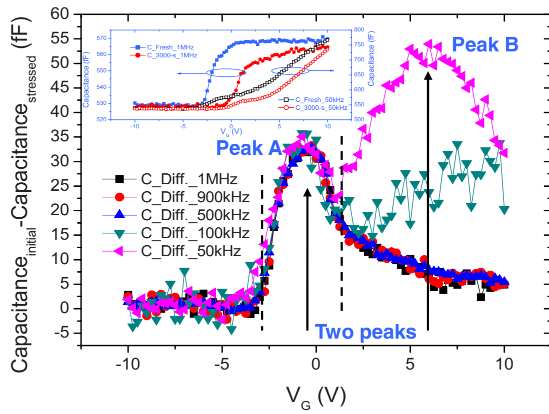

FIG. 2. (Color online) The difference of before and after stressed $C_{GD}-V_G$ curve (initial capacitance curve minus stressed capacitance curve) clearly represented the feature trend. The abbreviated graph presented the gate-to-drain capacitance (C_{GD}) vs gate voltage. $C_{GD}-V_G$ curve.

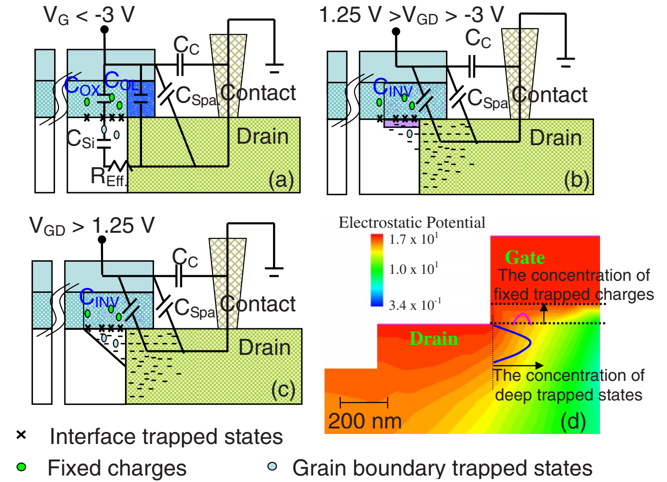

FIG. 3. (Color online) The capacitor model as (a) gate voltage is less than −3 V ($V_G<-3$ V), (b) gate voltage is between −3 and 1.25 V (-3 V $<V_G<1.25$ V), and (c) gate voltage is greater than 1.25 V ($V_G>1.25$ V). (d) The simulation of vertical and lateral electrical field from TCAD tool.

was observed in Fig. 1. The threshold voltage shift in this work was attributed to the dangling bonds and fixed oxide trapped charges. The flowing electrons in the channel were attracted by gate voltage, at this moment in time; silicon-hydrogen (Si–H) bonds were easily broken due to the collision from flowing electrons. The broken bonds became dangling bonds then degrading the drain current of device. In a word, as CGLC n-TFT was forced by dc voltage stress, it may induce oxide trapped charges, deep trapped states, and few of interface states since HCE.

An abbreviated graph in Fig. 2 presented the gate-to-drain capacitance (C_{GD}) versus gate voltage. $C_{GD}-V_G$ curve was reported to analyze device characteristic after stressed.[7] In order to verify grain boundary trapped states or fixed gate trapped charges effect on device, the frequency modulation of applied small signal, which were from 1 MHz to 50 kHz, was given. From the experimental data, a horizontal shift on $C_{GD}-V_G$ curve was observed before and after stressed and a distortion at the tail of 50 kHz had been discovered. However, the difference of before and after stressed $C_{GD}-V_G$ curve (initial capacitance curve minus stressed capacitance curve) in Fig. 2 clearly represented the feature trend which can be divided into three region, including $V_G<-3$ V, -3 V$<V_G<1.25$ V, and $V_G>1.25$ V.

For $V_G<-3$ V, the TFT device was accumulation mode that C_{GD} can be consider as $(C_{OL}\|C_{Spa})$.[13] The capacitor model was illustrated in Fig. 3(a). Supposing the overlap capacitor was damaged, the $C_{GD}-V_G$ curve should be shifted or depends on the applied frequency. However, the difference of capacitance approached to zero showed that the TFT device exhibited no damage except channel region after stressed.

The region of -3 V$<V_G<1.25$ V showed frequency independence, but gate bias dependence. Gate bias determined the inversion charges (electrons) which below the gate oxide. The inversion charges came from the drain terminal due to this terminal was connected to ground. The inversion layer was initially formed near the drain site at the channel region. As gate voltage increased, the inversion layer extended into the channel which can be seen in Fig. 3(b). The extended inversion layer was considered as a conductor which was modulated by gate voltage. Therefore, as gate voltage induced the inversion charges, the gate oxide trapped charges had been revealed in $C_{GD}-V_G$ curve. Most of the gate oxide trapped charges were resulted from the generation electrons of EHPs. Typically, EHPs was strongly relative to electrical field while stressing, and hence, Fig. 3(d) displayed the electrical field simulation of device with the stress condition. The peak of vertical electrical field in Fig. 3(d) had led the peak value of oxide trapped charges which described in Fig. 2.

The gate-to-drain capacitance started to be frequency-dependent while gate voltage was much than 1.25 V which was around threshold voltage. The frequency-dependent C_{GD} in Fig. 2 was attributed to the interface trapped states and grain boundary trapped states which were enhanced revealed by vertical and lateral electrical field, respectively. However, the amount of interface trapped charge was not greater than grain boundary trapped state,[14] and hence, the frequency-dependent C_{GD} was dominated by boundary trapped states. The frequency-dependent C_{GD} was appeared at large gate voltage. As gate voltage was above threshold voltage, electrons (for n-TFT) were accumulated under gate oxide layer. In the meantime, the interface trapped states and grain boundary trapped states easily caught the electrons, and then, decreased source-to-drain current. The peak A in Fig. 2 is resulted from the horizontal shift which can be observed in abbreviated graph of Fig. 2. For the peak B, this phenomenon speculated induces from the distribution of deep trapped states.[6]

For $C_{GD}-V_G$ measurement, the source terminal was floated so that most of electrons were provided from drain terminal. An illustration of the gradient of electron concentration was shown in Figs. 3(a)–3(c). Electrons filled in vertical were rapider than in lateral. Therefore, the C_{GD} revealed frequency- and gate voltage-dependent in this work. Moreover, the grain boundary trapped states depended on impact ionization which was determined by lateral electrical field. Consequently, from the TCAD simulation result, the most damaged region occurred in deep region labeled on Fig. 3(d).

In this study, gate-to-drain capacitance had been investigated to analyze the CGLC n-TFT under dc voltage stress, $V_G=V_D=16$ V. From the experimental data, the $C_{GD}-V_G$ curve can be divided into three regions. The first region ($V_G<-3$ V) showed no damage while stressing. The second

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region (-3 V $< V_G <$ 1.25 V) revealed the oxide trapped charge influencing C_{GD}. The third region ($V_G >$ 1.25 V) described a frequency-dependent C_{GD}. As gate voltage increased, the inversion layer which was considered by inversion charges determined the C_{GD} component. Therefore, combining the TCAD electrical field simulation, the distribution of oxide trapped charge and grain boundary trapped charge can be realized.

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